PARITY GENERATION AND CHECKING WITH THE 162511T

APPLICATION NOTE AN-121

By Stanley Hronik

INTRODUCTION

The 162511T has been designed to perform high-speed parity generation and checking. The device is a bus transceiver capable of bidirectional parity checking, or generation in one direction and checking in the other. Parity generation and checking are done at the byte level with individual parity bits for each byte. There is a separate parity error flag for each direction allowing easier failure isolation. The parity error flags are open drain outputs which will allow tying several parity error outputs together to generate a common error flag.

The 162511T contains a registered transceiver which is identical in function to the 162501T function. This transceiver is capable of acting as a bidirectional buffer, latch, register or any combination of the three, making the part universally adaptable to almost any parity situation. The parity functions are not affected by the mode and the parity and parity errors will appear at the device output simultaneously (except for variations in propagation delay) with the data. Because the part contains multiple functions in one package, the performance is superior to combinations of individual components.

The part is packaged in IDT's 25 mil pitch SSOP and Cerpack packages and 19.6 mil pitch TSSOP packages which have multiple grounds and V_{CCS}. The packages are designed for low noise, providing clean output waveforms and excellent noise immunity on the device inputs.

The output structure of the device is configured to provide a balanced output drive with equal current levels for high going and low going signals. The output static current levels are set at ±24mA commercial and ±16mA military for quiet operation similar to series current limiting resistors. The balanced output drivers will maintain lower noise levels and higher signal integrity than standard output drivers in most applications.

The power dissipation levels of the FCT162511T are characteristic of IDT's Double-Density™ product families. The power dissipation levels are lower over the entire operating frequency range than can be obtained with any bipolar, BiCMOS or standard CMOS components. The single component solution further reduces power dissipation by limiting the part count and number of devices switching.

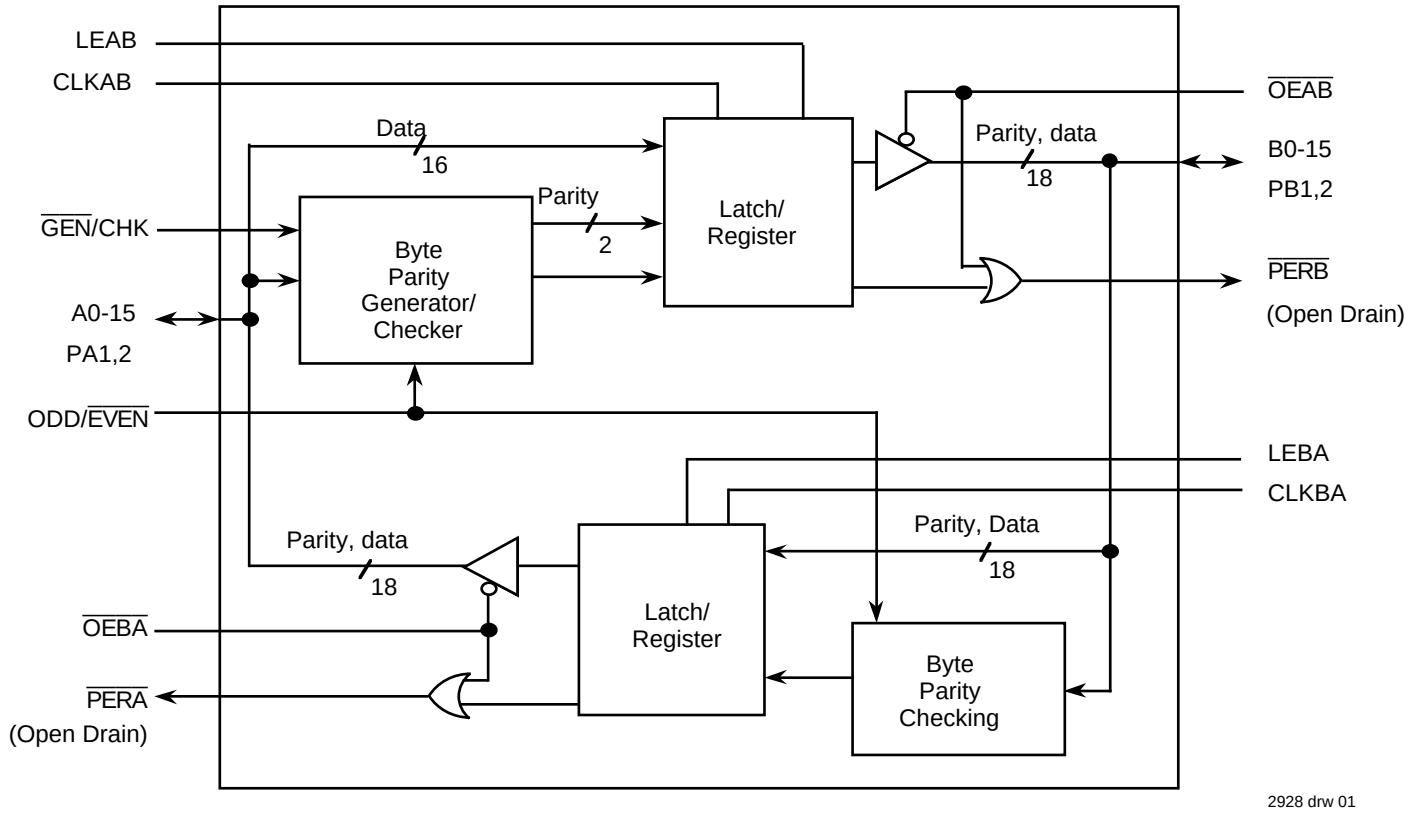

Figure 1. Simplified Block Diagram of 162511T

USAGE EXAMPLES

As a simple parity checker, the 162511T will perform unidirectional parity checking the same as a combination of two ‘280 parity trees as shown in Figures 2a and 2b. When generating a single parity error for both bytes of a 16 bit word, the ‘280 requires that the parity errors be combined by using a two input gate (similar to the ’08). In this simple application of parity, the use of a 162511T will provide superior performance to the combination of two ‘280s and a ’08 because of the accumulation of propagation delays with the multiple component solution.

Adding a buffer, latch, or register to the path of the multiple component configuration as shown in Figure 3a further increases the overall propagation delay, making the single component FCT162511T configuration of Figure 3b very attractive for high speed applications. The single component

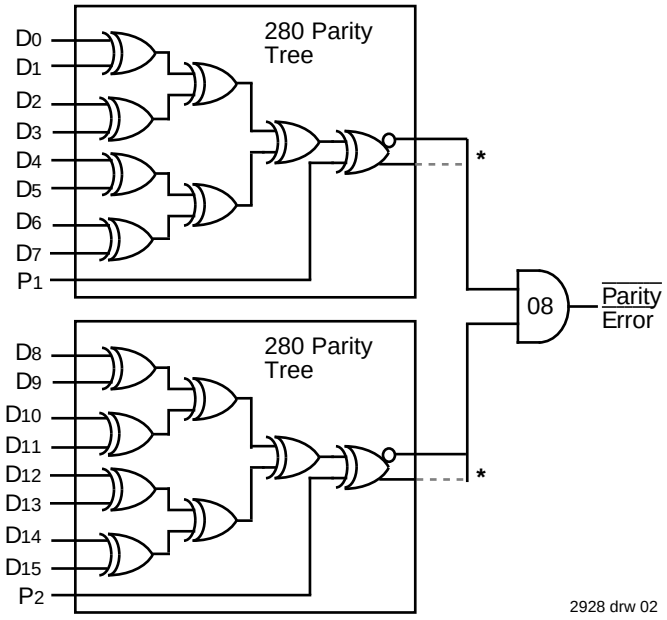

Figure 2a. An Example of 16-bit Parity Checking

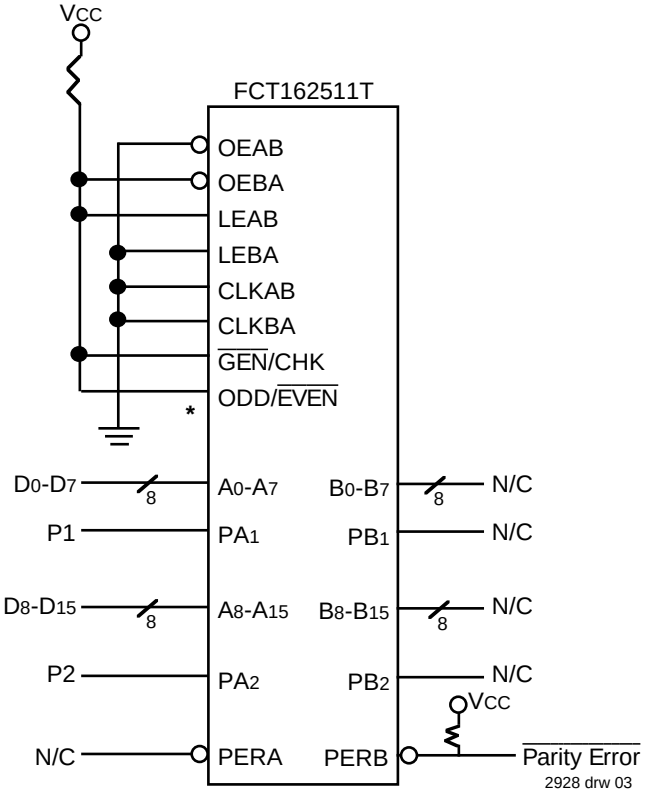

Figure 2b. The FCT162511T Implementation of Figure 2a.

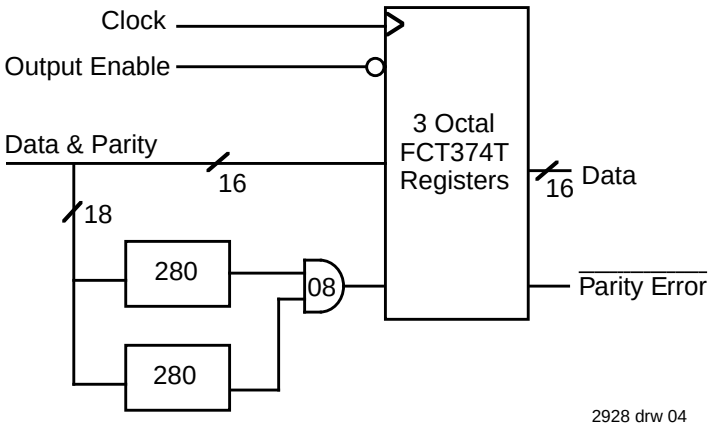

Figure 3a. A Registered Parity Applicaation

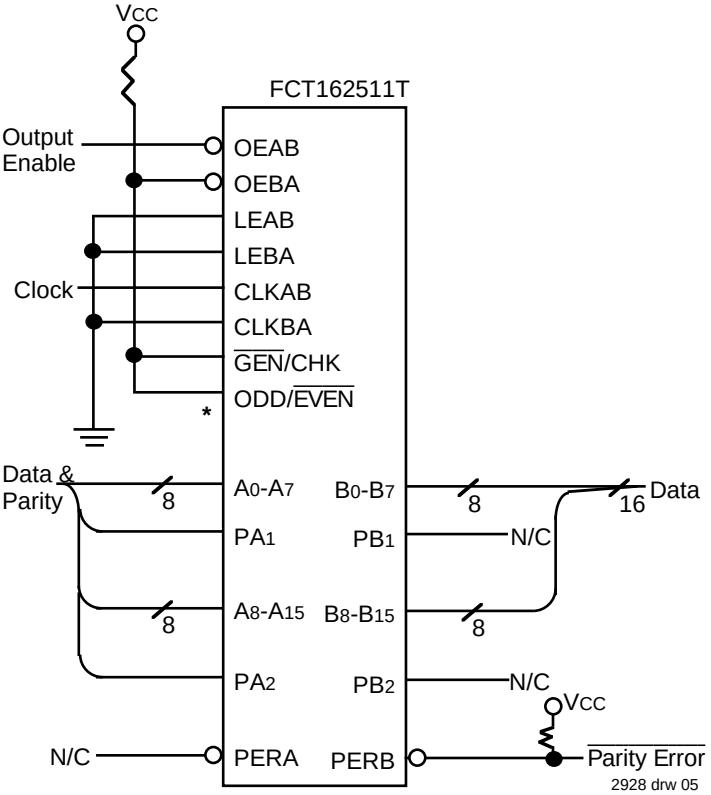

Figure 3b. The FCT162511T Implementation of Figure 3a

*Determines EVEN or ODD parity.

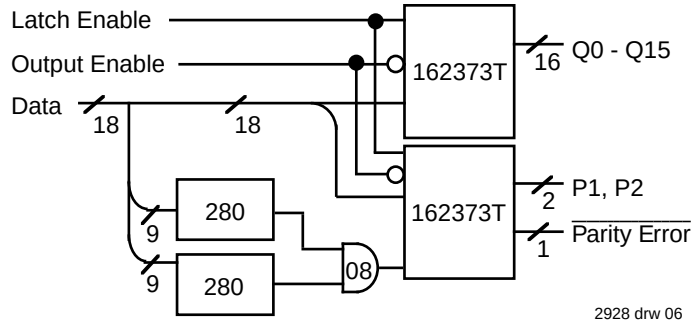

Figure 4a. A Parity Application using Latches

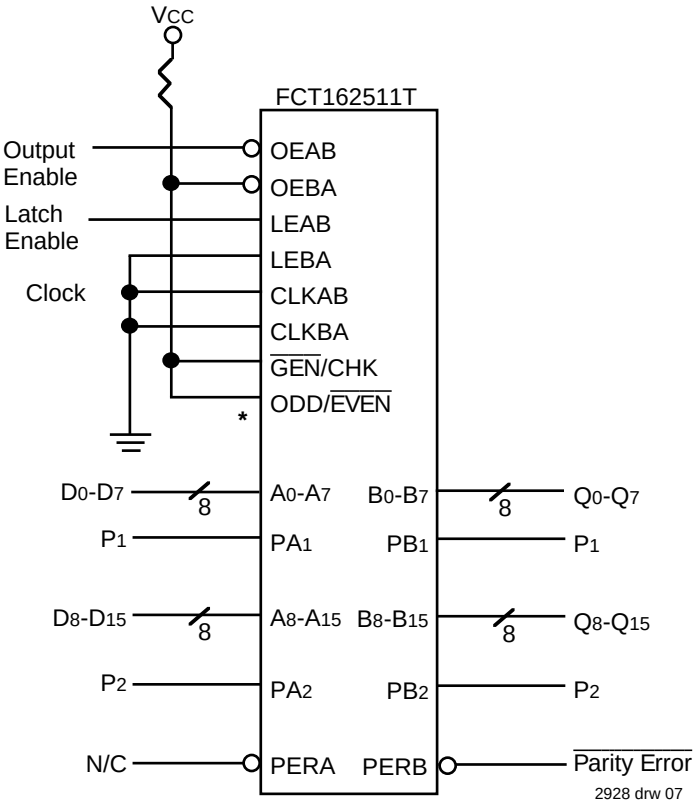

Figure 4b. The FCT162511T Implementation of Figure 4a

will also ease board layout problems by reducing part count.

Figure 4a shows an application similar to Figure 3a but using latches instead of registers. The162511T latched configuration is shown in Figure 4b.

Extending the application example to a bidirectional, 18 bit bus begins to demonstrate how effective the FCT162511T is in controlling part count and propagation delay. An example of a transceiver application using individual parts is shown in Figure 5a with the FCT162511T implementation shown in Figure 5b. In this application, parity is generated in the A to B direction. If the application requires registers or latches, the FCT162511T can provide the needed configuration without additional components, whereas, the discrete implementa-

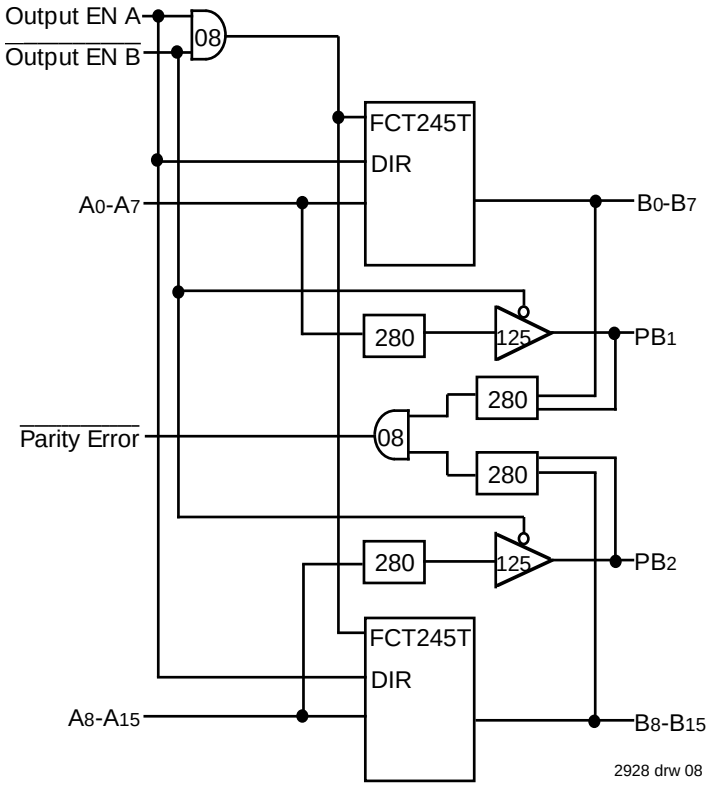

Figure 5a. Parity Generation from A to B, while checking from B to A

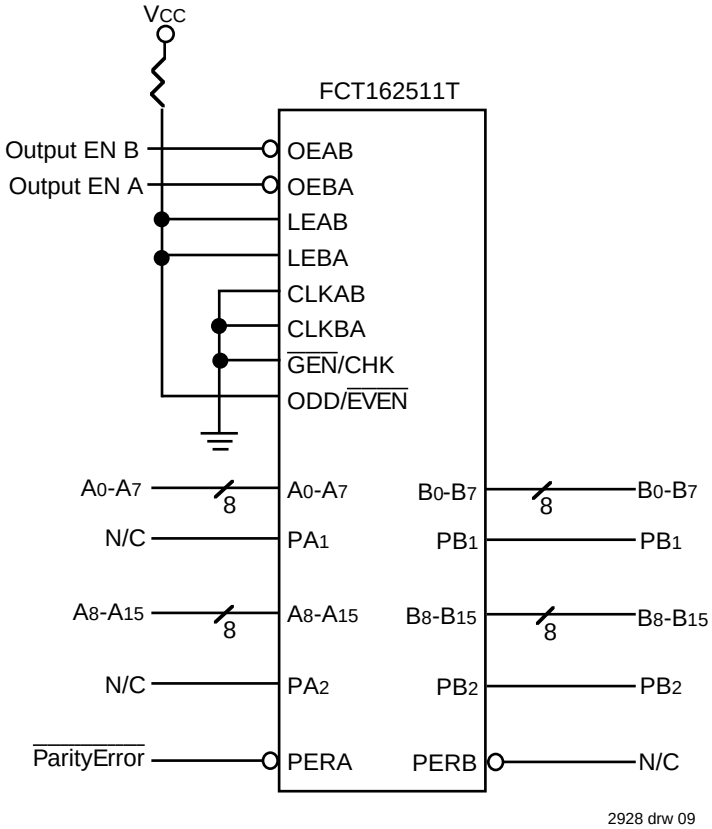

Figure 5b. The FCT162511T Implementation of Figure 5a.

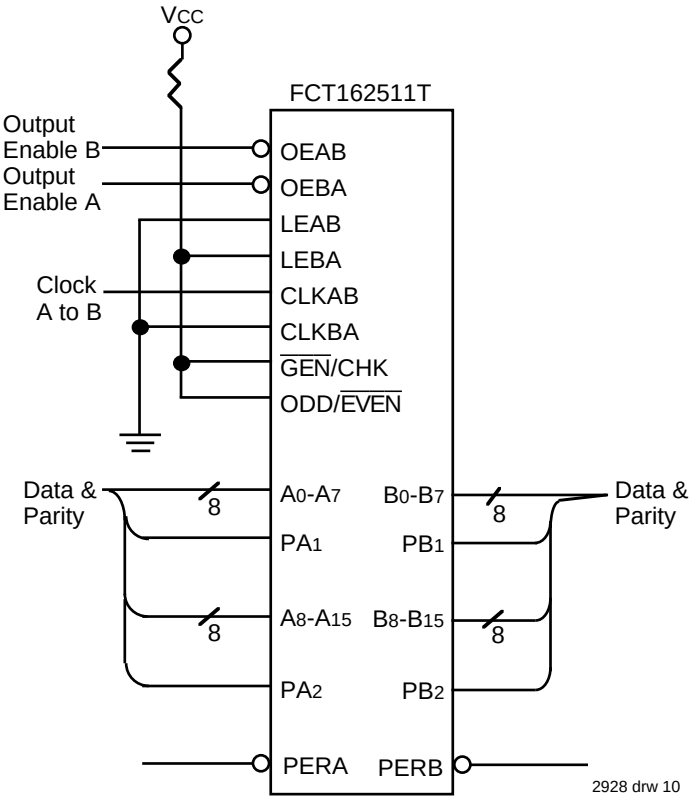

Figure 6. Mixed Mode Operation

tion of Figure 5a will require additional parts.

The 162511T is capable of operating in any unidirectional or bidirectional combination of buffers, latches, and registers. Because of this, the device can be configured as a register in one direction and a latch in the other, as a buffer and a register or as any other bidirectional combination of the three. Figure 6 shows an example of the 162511T used as a 162374T type register in the "A" to "B" direction and a 162244T type buffer in the "B" to "A" direction while checking parity in both directions.

CONNECTING THE PARITY PINS PA1 AND PA2

The input structures of the PA1 and PA2 pins (parity pins on the "A" port) have been designed to automatically disable when the 162511T is in a Generate Mode ($\overline{GEN}$/CHK LOW). In this mode, the PA1 and PA2 pins will act as true output pins with 3-state capability. Since the input structure of these pins has been disabled, the pins may be left floating, meaning it is not necessary to pull the PA1 and PA2 pins to either a HIGH or LOW state when the "A" port is disabled ($\overline{OEBA}$ HIGH). No oscillation or power dissipation problems will occur if the voltage on these pins floats near the logic input threshold voltage. This is useful when the 162511T is transferring data from the "A" port to the "B" port in Generate Mode and there is nothing driving the PA1 and PA2 pins.

USE OF THE PARITY ERROR PIN ($\overline{PERR}$)

The FCT162511T has a separate parity error output pin for each direction. These outputs are open drain which will require a pull up resistor to achieve a logic high state. Since they are open drain, the two pins can be tied together to form a common parity error flag for the device. In addition, several flags from several devices can be tied together forming a single parity error flag as shown in Figure 7. This could be used in applications which are not concerned with isolating the error, but instead use the flag to indicate a general failure condition. An example of a usage of this type would be a common interrupt at a central processor to which all parity error flags are directed, indicating that the CPU needs to exercise a fault correction routine (such as a data retransmission).

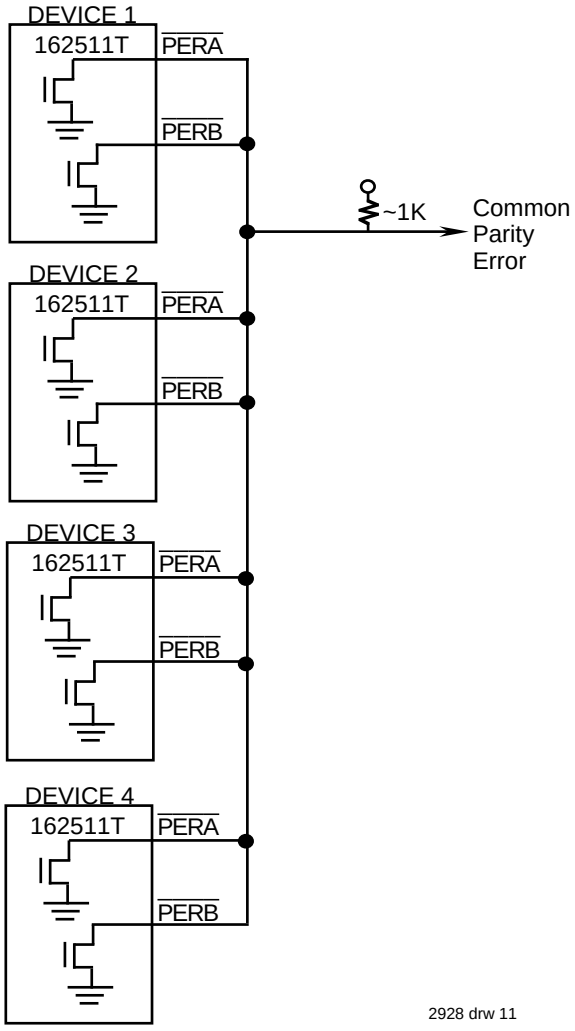

Figure 7. Combining Parity Errors

It should be noted that the $\overline{PERR}$ flag will give a very quick HIGH to LOW transition that is specified in the data sheet. Since there is no internal, active, pull up on the output, the rise time of the signal is dependent entirely upon external sources. The output needs an external pull up and the rise time of the signal will depend upon how quickly the external pull up can raise the signal.

APPLICATIONS OF THE FCT162511T

The 162511T adapts itself to most parity applications through its versatile, multifunctioned nature. Some of the

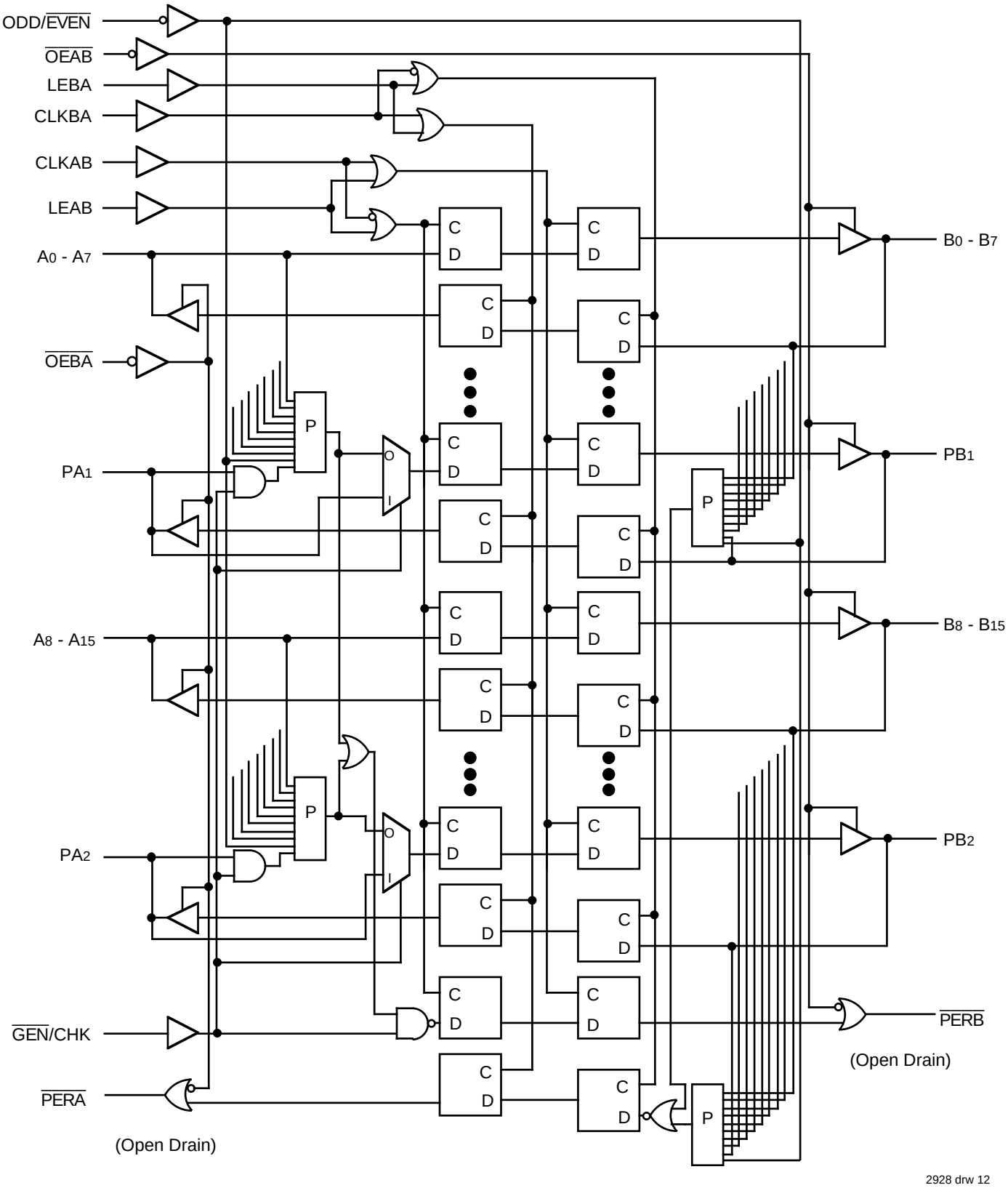

Figure 8. Full Schematic representation of the 162511

many applications which use parity and for which the 162511T is well suited include the following:

1) High-speed memory arrays which use parity generation and/or checking.

2) High-speed networking and communications applications which check data integrity through parity checking.

3) Disk drives or other peripheral applications which utilize parity. With the 162511T in this application it is possible to identify which side of the interface is causing parity errors.

4) Any high-speed application using parity and requiring a bidirectional buffer, register or latch.

SYSTEM TESTING USING THE FCT162511T

Performing system tests in a parity based system should include the testing of the parity error response. This testing usually involves injecting faulty data into the system and verifying that a parity error occurs. An easy way of accomplishing this with the FCT162511T is to toggle the $\overline{\text{EVEN}}$/ODD pin on the part. This can be done without adding a delay level or otherwise interfering with normal signal flow and operation. If the component is in a parity generation mode, toggling the $\overline{\text{EVEN}}$/ODD pin will cause the parity bit to be reversed from its proper state which should be detected by a later stage in the system. If the FCT162511T is in a checking mode when the $\overline{\text{EVEN}}$/ODD pin is toggled, a parity error flag will be generated. The proper handling of the parity error through subsequent stages of the system can then be verified.

SUMMARY

The FCT162511T is a highly integrated component with the flexibility to be dynamically configured to act as a bidirectional latch, buffer, register, parity tree, or any combinational pair of these. For most applications the FCT162511T will provide the fastest and lowest cost solution to parity generation/checking problems with a minimum of board space required. In design situations requiring the use of parity, the FCT162511T will typically provide performance levels, integration levels, low power levels and flexibility that are not achievable with other solutions. Usually the FCT162511T will provide these benefits at a cost savings.

A COMPARISON OF COMMON PARITY GENERATORS/CHECKERS

Part Type	Mfg	Configuration	#	Bidirection	Gen	Chk	Gen/Chk	Chk/Chk	Transpar	Register	Latch	Odd/Even
280	TI,Q,M,N	tree	1		x	x						either
480	P	tree	2		x	x						odd
481	P	tree	2		x	x						even
552	S	register	8	x	x	x	x			x		odd
11286	TI	tree	1		x	x						either
833/34	IDT,TI,P,Q	buffer	8	x	x	x	x		x			odd
853/54	TI,P,Q	buffer	8	x	x	x	x		x			odd
16657	TI	buffer	16	x	x	x	x		x			either
16833/34	TI	buffer	16	x	x	x	x		x			odd
16853/54	TI	buffer	16	x	x	x	x		x			odd
657	P,N	buffer	8	x	x	x	x		x			either
899	TI,N	latch	9	x	x	x		x	x		x	either
73210/11	IDT	register	9	x	x	x	x	x		x		even
162511	IDT	buf/reg/latch	18	x	x	x	x	x	x	x	x	either

NOTES:

1. The 833 has a registered Parity Error, The 853 has a latched Parity Error.
2. The 162511 has a separate parity error flag for each direction
3. The 833, 853, 16833, 16853, and 162511 have open collector parity error flags
4. The 73210/11 is capable of even parity generation or checking in either direction or odd generation in the A to B direction only
5. The 162511, 73210/11 and 899 will pass parity while checking
6. The 899 will generate in both directions or check in both directions
7. For trees, # is the number of parity trees contained within the part.
8. For Latches, Registers and Buffers, # is the number of bits that the part will pass without stripping (many parts strip or add the parity bit).

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