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SH7137 Group

12-Bit A/D Converter:
Example of Settings for Conversion in Single-Scan Mode

Introduction
This application note describes an example of settings for the 12-bit A/D converter in single-scan mode as an example of application of the A/D converter of the SH7137.

Target Device
SH7137

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1. Preface

1.1 Specifications

- A/D conversion in single-scan mode by the 12-bit A/D converter
- Three rounds of A/D conversion are performed on analog input channels 0 to 3 (AN0 to AN3), and the converted data are stored in RAM.

1.2 Module Used

- 12-bit A/D converter (12-bit A/D)

1.3 Applicable Conditions

- MCU: SH7137/SH7136
- Operating frequency:
  - Internal clock: 80 MHz
  - Bus clock: 40 MHz
  - Peripheral clock: 40 MHz
- Compiler:
  - SuperH RISC engine Family C/C++ Compiler Package Ver.9.01 Release01 from Renesas Technology
- Compiler options:
  -cpu = sh2a -include = "$(WORKSPDIR)/inc"
  -object = "$(CONFIGDIR)/FILELEAF.obj" -debug -gbr = auto -chgincpath -errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0
  -del_vacant_loop = 0 -struct_alloc = 1 -nologo

1.4 Related Application Note

None
2. Description of the Sample Application

The sample program employs the single-scan mode of the 12-bit A/D converter to perform three rounds of A/D conversion on input channels 0 to 3 (AN0 to AN3), and then stores converted data in RAM.

2.1 Operational Overview of Module Used

The operating modes of the 12-bit A/D converter are single-cycle scan mode and continuous scan mode. In single-cycle scan mode, A/D conversion is performed once on each of one or more specified channels and then ends. The ADST bit is automatically cleared to 0. In continuous scan mode, A/D conversion is performed sequentially on one or more specified channels until the ADST bit is cleared to 0.

Additionally, channels 0 to 2 and 8 to 10 have dedicated sample-and-hold circuits, so multiple channels are capable of simultaneous sampling.

Table 1 gives an overview of the module used in this sample application (i.e. the A/D converter) and figure 1 is a block diagram of 12-bit A/D converter. For details on the 12-bit A/D converter, see the section on the A/D converter in the SH7137 Group Hardware Manual.

Table 1 Overview of the Module (A/D Converter) Used in the Sample Application

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Resolution</td>
<td>12 bits</td>
</tr>
<tr>
<td>Minimum conversion time</td>
<td>1.25 μs per channel (Pφ = 40 MHz)</td>
</tr>
<tr>
<td>Number of modules</td>
<td>2</td>
</tr>
<tr>
<td>Input channels</td>
<td>16 (SH7137), 12 (SH7136)</td>
</tr>
<tr>
<td>Operating modes</td>
<td>Single-cycle scan mode&lt;br&gt;Continuous scan mode</td>
</tr>
<tr>
<td>Sample-and-hold function</td>
<td>Common to 0 to 7 channels: 1 circuit&lt;br&gt;Common to 8 to 15 channels: 1 circuit&lt;br&gt;Dedicated for individual channels: 1 circuit each for ch0 to 2 and 8 to 10 (6 in all)</td>
</tr>
<tr>
<td>Sources for activation of A/D conversion</td>
<td>Software: Setting of the ADST bit&lt;br&gt;Timer: TRGAN, TRG0N, TRG4AN, and TRG4BN signals from the MTU2 module&lt;br&gt;TRGAN, TRG4AN, and TRG4BN signals from the MTU2S module&lt;br&gt;External trigger: ADTRG</td>
</tr>
</tbody>
</table>
Figure 1  Block Diagram of the 12-Bit A/D Converter
2.2 Procedure for Setting Module Used

Figure 2 shows an example of the initialization sequence for A/D conversion in single-scan mode. For details on the settings of individual registers, see the *SH7137 Group Hardware Manual*.

```
START

Release A/D converter from module stop mode
STB.CR4.BIT._ADC0 = 0x00;

Set A/D control register_0 (ADCR_0)

Set A/D analog input channel select register_0
(ADANSR_0)

Set A/D status register_0 (ADSR_0)

END
```

- Setting of standby control register 4 (STBCR4)
  MSTP19 (module stop) bit is cleared to 0.
  [Function]
  The ADC0 converter is released from module standby mode.

- Setting of ADC control register (ADCR_0)
  ADST Clear the A/D Start bit to 0.
  [Function]
  A/D conversion is halted.
  ADCS Clear the A/D Continuous Scan bit to 0.
  [Function]
  Single-cycle scan mode is selected.
  ACE Set the Automatic Clear Enable bit.
  [Function]
  Automatic clearing of ADDR after ADDR has been read is disabled or enabled.
  ADIE Set the A/D Interrupt Enable bit.
  [Function]
  A/D conversion end interrupt is disabled or enabled.
  TRGE Set the Trigger Enable bit.
  [Function]
  Starting of A/D conversion by the external trigger or an A/D conversion start trigger from the MTU2 or MTU2S module is disabled or enabled.
  EXTRG Set the Trigger Select bit.
  [Function]
  A/D conversion start trigger is selected as a trigger from the MTU2/MTU2S modules or an external trigger from the external pin (ADTRG).

- Specification of analog input channel (ADANSR_0)
  Set ANS bits (ANS[7:0]):
  [Function]
  Channels are selected

- Clear of A/D end flag (ADSR_0)
  ADF Confirm the A/D End Flag bit is 1, then set it to 0 after the ADF bit has been read.
  [Function]
  A/D end flag is cleared.
  Note: Do not overwrite this bit with 0 when the value of this bit is 0.

---

**Figure 2  Initialization Sequence for 12-Bit A/D Conversion**


2.3 Operation of the Sample Program

In this sample program, A/D conversion in single-scan mode is performed on channels 0 to 3 (AN0 to AN3). The A/D converter is activated by software and converted data are stored in RAM. This processing is repeated three times.

Table 2 gives a description of RAM usage in this sample program.

Table 2 Variables Used in the Sample Program

<table>
<thead>
<tr>
<th>Variable Name</th>
<th>Description</th>
<th>Area</th>
<th>Name of Employing Module</th>
</tr>
</thead>
<tbody>
<tr>
<td>unsigned short</td>
<td>Array for storing A/D-converted data (2 bytes/datum)</td>
<td>On-chip RAM</td>
<td>io_ad_1cyc_scan (unsigned short*ad_buf)</td>
</tr>
</tbody>
</table>

2.4 Sequence of Processing by the Sample Program

Table 3 gives settings for registers used in the sample program and figure 3 shows the flow of handling the sample program.

Table 3 Register Settings Used in Sample Program

<table>
<thead>
<tr>
<th>Register Name</th>
<th>Address</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
</table>
| A/D control register_0 (ADCR_0) | H'FFFF D400 | H'00    | • ADST = 0: Halts A/D conversion  
• ADCS = 0: Single-cycle scan  
• ACE = 0: Disables automatic clearing of ADDR  
• ADIE = 0: Disables A/D conversion end interrupt  
• TRGE = 0: Disables starting of A/D conversion by an external trigger or by the MTU2 and MTU2S modules |
|                       | H'80       |         | • ADST = 1: Starts A/D conversion                                            |
Main (main)

START

Set the count variable to 0

Initialization of A/D converter
io_ad_init();

A/D conversion and storage of converted data (first round):
io_ad_1cyc_scan();

A/D conversion and storage of converted data (second round):
io_ad_1cyc_scan();

A/D conversion and storage of converted data (third round):
io_ad_1cyc_scan();

END

Release A/D converter from module stop mode
STB.CR4.BIT._ADC0 = 0x00;

Set A/D control register_0 (ADCR_0)

Set A/D analog input channel select register_0 (ADANSR_0)

Set A/D status register_0 (ADSR_0)

END

START

Initialization of A/D converter (io_ad_init)

A/D conversion (io_ad_1cyc_scan)

START

Set A/D control register_0 (ADCR_0)

Set A/D analog input channel select register_0 (ADANSR_0)

Set A/D status register_0 (ADSR_0)

End of A/D conversion?
ADC0.ADSR.BIT.ADF == 0?

Clear A/D end flag
ADC0.ADSR.BIT.ADF = 0;

Store result of conversion

END

Figure 3 Flow of Handling the Sample Program
3. Listing of Sample Program

1. Sample Program Listing: "main.c" (1)

1 /*"FILE COMMENT"*************************************************************************/
2 * System Name : SH7137 Sample Program
3 * File Name  : main.c
4 * Contents  : Sample program for A/D conversion in single-scan mode
5 * Version : 1.00.00
6 * Model : M3A-HS37
7 * CPU : SH7137
8 * Compiler : SHC9.1.1.0
9 * note : A/D conversion in single-scan mode is performed by the A/D converter.
10 *        Three rounds of A/D conversion on analog input channels 0 to 3
11 *        (AN0 to AN3) proceed, and the converted data are stored in RAM.
12 *
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18 * Copyright (C) 2008 Renesas Technology Corp. All Rights Reserved
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20 *
21 * history : 2008.02.26 ver.1.00.00
22 */"FILE COMMENT END"**************************************************************************/
23 #include <machine.h>
24 #include "iodefine.h" /* SH7137 iodefine */
25 void main(void);
26 void io_ad_init(void);
27 void io_ad_1cyc_scan(unsigned short *ad_buf);
28 /
29 /* ----- prototype declaration ----- */
30 #define AD 3
31 #define CH 4
32 /* ----- symbol definition ----- */
33 unsigned short Ad_data[AD][CH];
34 /* ----- RAM allocation variable declaration ----- */
2. Sample Program Listing: "main.c" (2)

```c
/*""FUNC COMMENT"**************************************************************
 * Outline  : main
 *-------------------------------------------------------------------------------
 * Include  : #include "iodefine.h"
 *              #include <machine.h>
 *-------------------------------------------------------------------------------
 * Declaration : void main(void);
 *-------------------------------------------------------------------------------
 * Function  : A/D conversion with 1 cycle scan mode
 *-------------------------------------------------------------------------------
 * Argument  : void
 *-------------------------------------------------------------------------------
 * Return Value : none
 *-------------------------------------------------------------------------------
 * Notice  :
 *""FUNC COMMENT END"***********************************************************/

void main(void)
{
    unsigned char count;
    count = 0;

    /* ==== Initial Setting of ADC ==== */
    io_ad_init();

    /* ==== A/D conversion ==== */
    io_ad_1cyc_scan(&Ad_data[count][0]);
    count++;
    io_ad_1cyc_scan(&Ad_data[count][0]);
    count++;
    io_ad_1cyc_scan(&Ad_data[count][0]);

    while(1){
        /* loop */
    }
}

/*""FUNC COMMENT"**************************************************************
 * Outline  : Initial setting of ADC
 *-------------------------------------------------------------------------------
 * Include  : #include "iodefine.h"
 *-------------------------------------------------------------------------------
 * Declaration : void io_ad_init(void);
 *-------------------------------------------------------------------------------
 * Function  : Initial setting of ADC
 *-------------------------------------------------------------------------------
 * Argument  : void
 *-------------------------------------------------------------------------------
 * Return Value : none
 *-------------------------------------------------------------------------------
 * Notice  :
 *""FUNC COMMENT END"***********************************************************/
```
void io_ad_init(void)
{
    /* ==== Release of power down mode (ADC0) ==== */
    STB.CR4.BIT._ADC0 = 0x00;
    /* ==== Setting of ADC ==== */
    /* ---- A/D Control Register (ADCR) ---- */
    ADC0.ADCR.BYTE = 0x00;
    /* 7 = b'0  : A/D conversion start flag*/
    /* 6 = b'0  : Single-cycle scan */
    /* 5 = b'0  : Automatic clearing of ADDR by its readout is disabled */
    /* 4 = b'0  : Generation of A/D conversion end interrupt is disabled */
    /* 3-2 = b'0  : Reserve */
    /* 1 = b'0  : A/D conversion start by the external trigger or an A/D conversion start trigger from the MTU2 or MTU2S is disabled */
    /* 0 = b'0  : A/D converter is started by the A/D conversion start trigger from the MTU2 or MTU2S */

    /* ---- A/D Analog Input Channel Select Register (ADANSR) ---- */
    ADC0.ADANSR.BYTE = 0x0f;         /* AN0-AN3 */

    /* ---- A/D Status Register (ADSR) ---- */
    if(ADC0.ADSR.BIT.ADF == 0x01){
        ADC0.ADSR.BIT.ADF = 0x00;  /* ADF clear */
    }
}

void io_ad_1cyc_scan(unsigned short *ad_buf)
{
    ADC0.ADCR.BIT.ADST = 1;  /* A/D conversion start */
    while(ADC0.ADSR.BIT.ADF == 0){
        /* A/D conversion completion waiting */
    }
    ADC0.ADSR.BIT.ADF = 0;   /* ADF clear */
    *ad_buf++ = ADC0.ADDR0;  /* AN0 */
    *ad_buf++ = ADC0.ADDR1;  /* AN1 */
    *ad_buf++ = ADC0.ADDR2;  /* AN2 */
    *ad_buf++ = ADC0.ADDR3;  /* AN3 */
}

/* End of File */
4. Documents for Reference

- Software Manual
  SH-1/SH2/SH-DSP Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.

- Hardware Manual
  SH7137 Group Hardware Manual
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