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SH7211 Group

12-Bit A/D Converter: Example of Settings for Conversion in Single-Scan Mode

Introduction

This application note describes an example of settings for the 12-bit A/D converter in single-scan mode as an example of application of the A/D converter of the SH7211.

Target Device

SH7211

Contents

1. Preface

1.1 Specifications

- A/D conversion in single-scan mode by the 12-bit A/D converter
- Three rounds of A/D conversion are performed on analog input channels 0 to 3 (AN0 to AN3), and the converted data are stored in RAM.

1.2 Module Used

- 12-bit A/D converter (12-bit A/D)

1.3 Applicable Conditions

• MCU	SH7211
• Operating frequency	Internal clock: 160 MHz Bus clock: 40 MHz Peripheral clock: 40 MHz
• C compiler	SuperH RISC Engine Family C/C++ Compiler Package Ver.9.0.1 Release01 from Renesas Technology
• Compiler options	-cpu = sh2a -include = "$(WORKSPDIR)\inc" -object = "$(CONFIGDIR)\$(FILELEAF).obj" -debug -gbr = auto -chgincpath -errorpath -global_volatile = 0 -opt_range = all -inifinte_loop = 0 -del_vacant_loop = 0 -struct_alloc = 1 -nologo

1.4 Related Application Note

None

2. Description of the Sample Application

The sample program employs the single-scan mode of the 12-bit A/D converter to perform three rounds of A/D conversion on input channels 0 to 3 (AN0 to AN3), and then stores converted data in RAM.

2.1 Operational Overview of Module Used

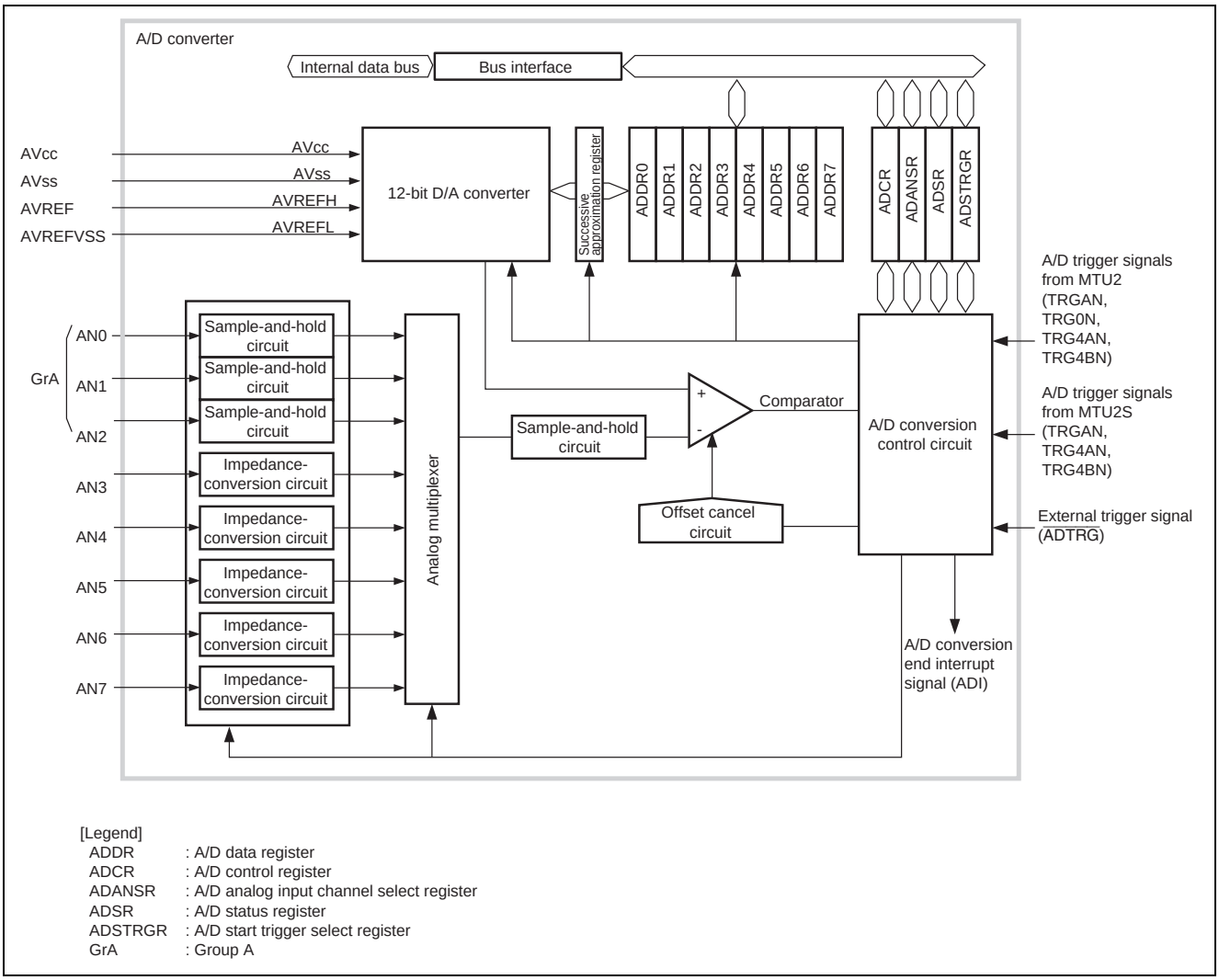
The operating modes of the 12-bit A/D converter are single-cycle scan mode and continuous scan mode. In single-cycle scan mode, A/D conversion is performed once on each of one or more specified channels and then ends. The ADST bit is automatically cleared to 0. In continuous scan mode, A/D conversion is performed sequentially on one or more specified channels until the ADST bit is cleared to 0.

Additionally, channels 0, 1, and 2 have dedicated sample-and-hold circuits, so multiple channels are capable of simultaneous sampling.

Table 1 gives an overview of the module used in this sample application (i.e. the A/D converter) and figure 1 is a block diagram of 12-bit A/D converter. For details on the 12-bit A/D converter, see the section on the A/D converter in the *SH7211 Group Hardware Manual*.

Table 1 Overview of the Module (A/D Converter) Used in the Sample Application

Item	Description
Resolution	12 bits
Minimum conversion time	1.25 μs per channel (Pϕ = 40 MHz)
Number of modules	1
Input channels	8
Operating modes	Single-cycle scan mode Continuous scan mode
Sample-and-hold function	Common to all channels: 1 circuit Dedicated for individual channels: 1 circuit each for ch0, ch1, and ch2 (3 in all)
Sources for activation of A/D conversion	Software: Setting of the ADST bit Timer: TRGAN, TRG0N, TRG4AN, and TRG4BN signals from the MTU2 module TRGAN, TRG4AN, and TRG4BN signals from the MTU2S module External trigger: $\overline{\text{ADTRG}}$



[Legend]
ADDR : A/D data register
ADCR : A/D control register
ADANSR : A/D analog input channel select register
ADSR : A/D status register
ADSTRGR : A/D start trigger select register
GrA : Group A

Figure 1 Block Diagram of the 12-Bit A/D Converter

2.2 Procedure for Setting Module Used

Figure 2 shows an example of the initialization sequence for A/D conversion in single-scan mode. For details on the settings of individual registers, see the *SH7211 Group Hardware Manual*.

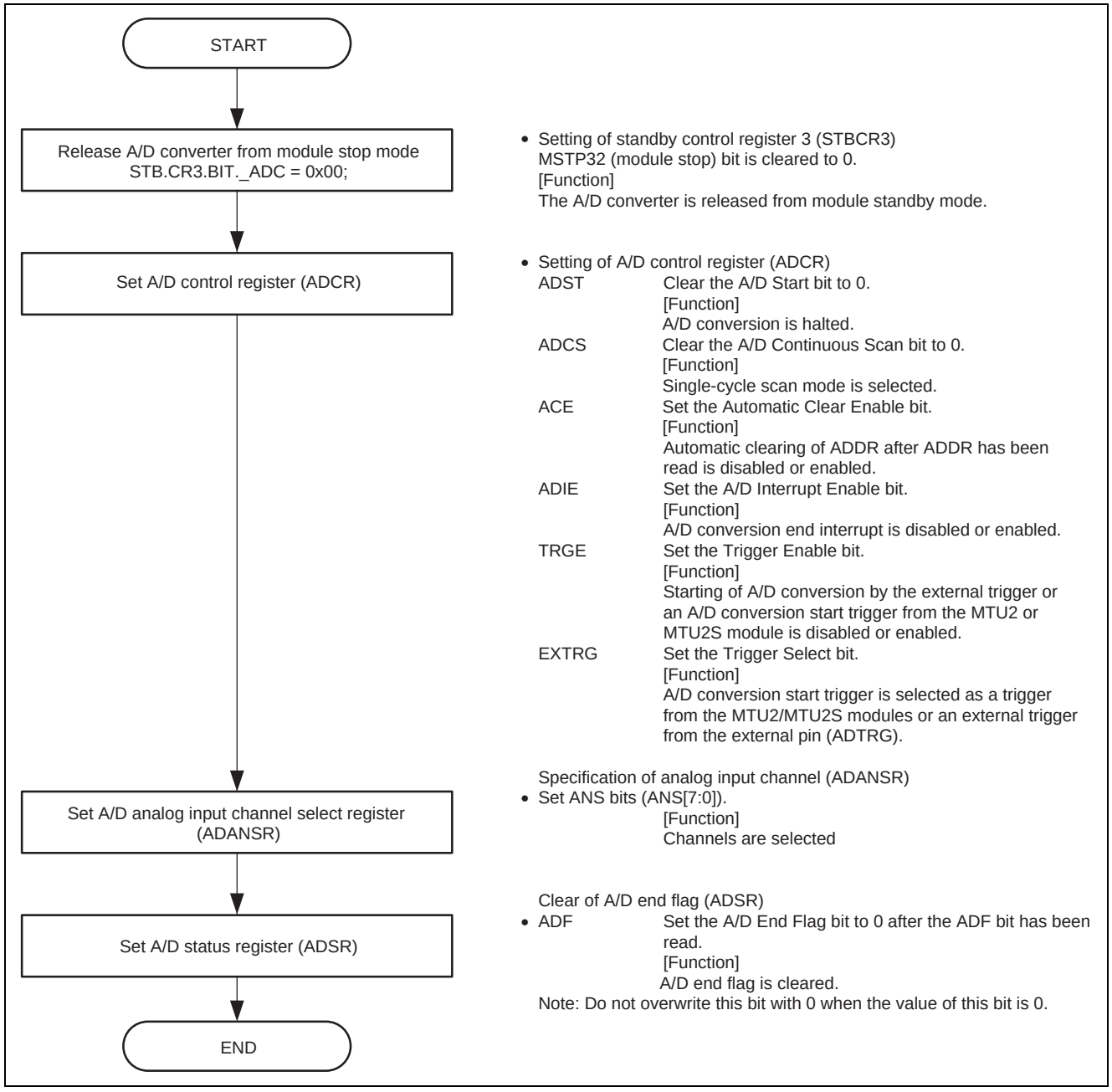


Figure 2 Initialization Sequence for 12-Bit A/D Conversion

2.3 Operation of the Sample Program

In this sample program, A/D conversion in single-scan mode is performed on channels 0 to 3 (AN0 to AN3). The A/D converter is activated by software and converted data are stored in RAM. This processing is repeated three times.

Table 2 gives a description of RAM usage in this sample program.

Table 2 Variables Used in the Sample Program

Variable Name	Description	Area	Name of Employing Module
unsigned short Ad_data[AD][CH]	Array for storing A/D-converted data (2 bytes/datum)	On-chip RAM	io_ad_1cyc_scan (unsigned short*ad_buf)

2.4 Sequence of Processing by the Sample Program

Table 3 gives settings for registers used in the sample program and figure 3 shows the flow of handling the sample program.

Table 3 Register Settings Used in Sample Program

Register Name	Address	Setting	Description
A/D control register (ADCR)	H'FFFFE800	H'00	• ADST = 0: Halts A/D conversion • ADCS = 0: Single-cycle scan • ACE = 0: Disables automatic clearing of ADDR • ADIE = 0: Disables A/D conversion end interrupt • TRGE = 0: Disables starting of A/D conversion by an external trigger or by the MTU2 and MTU2S modules
		H'80	• ADST = 1: Starts A/D conversion

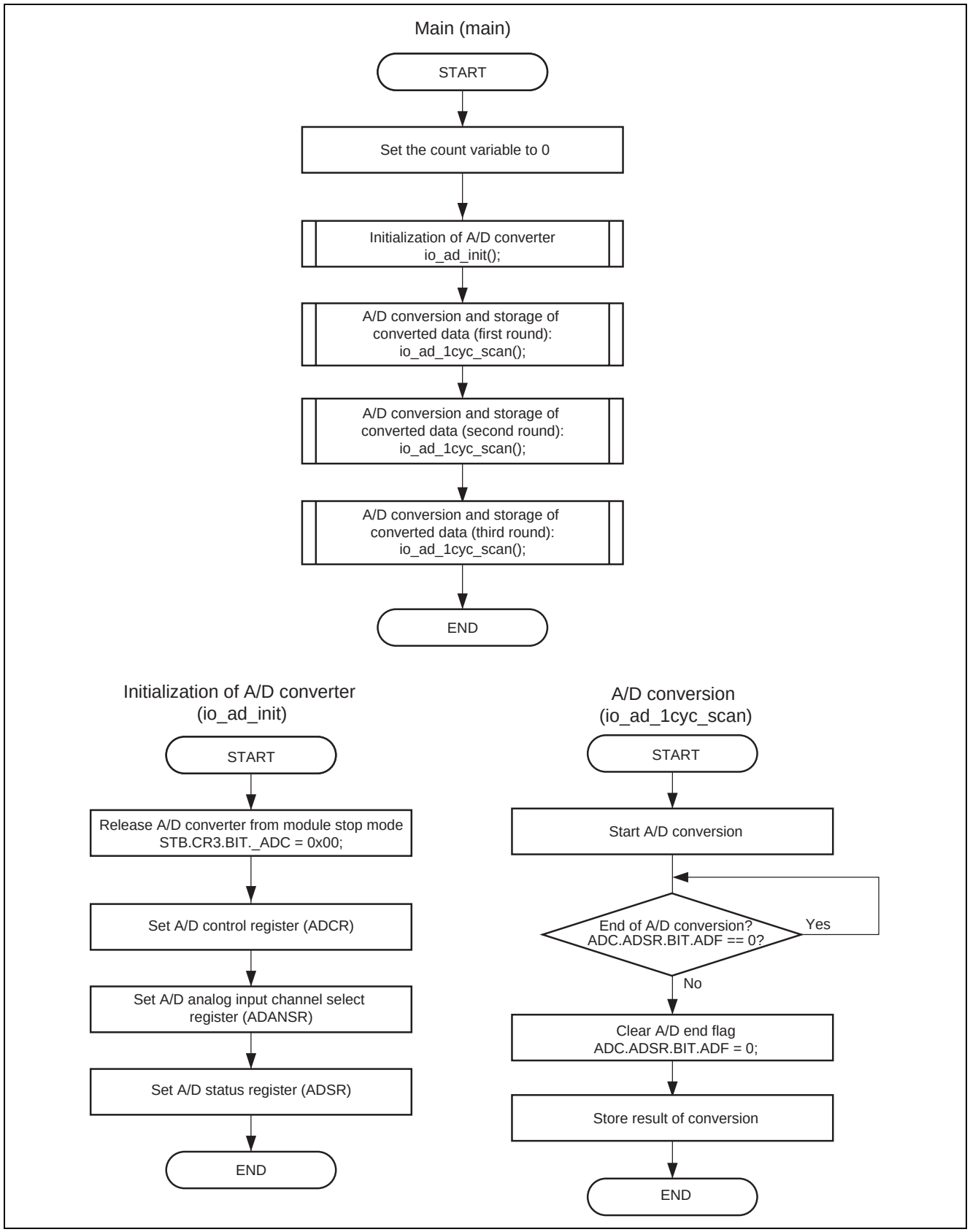


Figure 3 Flow of Handling the Sample Program

3. Listing of Sample Program

1. Sample Program Listing: "main.c" (1)

```
1  /*""FILE COMMENT""*******************************************************************************
2  *
3  *       System Name    : SH7211 Sample Program
4  *       File Name      : main.c
5  *       Contents       : Sample program for A/D conversion in single-scan mode
6  *       Version        : 1.00.00
7  *       Model          : M3A-HS11
8  *       CPU            : SH7211
9  *       Compiler       : SHC9.1.1.0
10 *       note           : A/D conversion in single-scan mode is performed by the A/D
11                          converter. Three rounds of A/D conversion on analog input channels
12                          0 to 3 (AN0 to AN3)proceed, and the converted data are stored in
13                          RAM.
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22 *
23 *       history        : 2008.02.26 ver.1.00.00
24 *""FILE COMMENT END""*******************************************************************************/
25 #include <machine.h>
26 #include "iodefine.h"         /* SH7211 iodefine  */
27
28
29 /* ==== prototype declaration ==== */
30 void main(void);
31 void io_ad_init(void);
32 void io_ad_1cyc_scan(unsigned short *ad_buf);
33
34 /* ==== symbol definition ==== */
35 #define AD 3
36 #define CH 4
37
38 /* ==== RAM allocation variable declaration ==== */
39 unsigned short Ad_data[AD][CH];
```

2. Sample Program Listing: "main.c" (2)

```
/*""FUNC COMMENT""*************************************************
* Outline      : main
*-----------------------------------------------------------------
* Include      : #include "iodefine.h"
*              : #include <machine.h>
*-----------------------------------------------------------------
* Declaration  : void main(void);
*-----------------------------------------------------------------
* Function     : AD translation with 1 cycle scan mode
*-----------------------------------------------------------------
* Argument     : void
*-----------------------------------------------------------------
* Return Value : void
*-----------------------------------------------------------------
* Notice       : non
*""FUNC COMMENT END""*********************************************/
void main(void)
{
    unsigned char count;
    count = 0;

    /* ==== Initial Setting of ADC ==== */
    io_ad_init();

    /* ==== A/D convert ==== */
    io_ad_1cyc_scan(&Ad_data[count][0]);
    count++;
    io_ad_1cyc_scan(&Ad_data[count][0]);
    count++;
    io_ad_1cyc_scan(&Ad_data[count][0]);

    while(1){
    /* loop */
    }
}

/*""FUNC COMMENT""*************************************************
* Outline      : Initial setting of ADC
*-----------------------------------------------------------------
* Include      : #include "iodefine.h"
*-----------------------------------------------------------------
* Declaration  : void io_ad_init(void);
*-----------------------------------------------------------------
* Function     : Initial setting of ADC
*-----------------------------------------------------------------
* Argument     : void
*-----------------------------------------------------------------
* Return Value : void
*-----------------------------------------------------------------
* Notice       : non
*""FUNC COMMENT END""*********************************************/
```

3. Sample Program Listing: "main.c" (3)

```
91  void io_ad_init(void)
92  {
93      /* ==== Release of power down mode(ADC) ==== */
94      STB.CR3.BIT._ADC = 0x00;
95
96      /* ==== Setting of ADC ==== */
97      /* ---- A/D Control Register(ADCR) ---- */
98      ADC.ADCR.BYTE = 0x00;
99          /* 7    = b'0      : A/D End Flag                                  */
100         /* 6    = b'0      : Single-cycle scan                             */
101         /* 5    = b'0      : Automatic clearing of ADDR
102                               after being read is disabled                 */
103         /* 4    = b'0      : Generation of A/D conversion end
104                               interrupt is disabled                        */
105         /* 3-2  = b'0      : reserve                                       */
106         /* 1    = b'0      : A/D conversion start by the external trigger
107                               or an A/D conversion start trigger from
108                               the MTU or MTU2S is disabled                 */
109         /* 0    = b'0      : A/D converter is started by the A/D conversion
110                               start trigger from the MTU2 or MTU2S         */
111
112     /* ---- A/D Analog Input Channel Select Register(ADANSR) ---- */
113     ADC.ADANSR.BYTE = 0x0F;       /* AN0-AN3 */
114
115     /* ---- A/D Status Register(ADSR) ---- */
116     if(ADC.ADSR.BIT.ADF == 0x01){
117     ADC.ADSR.BIT.ADF = 0x00;      /* ADF clear */
118     }
119 }
120
121 /*""FUNC COMMENT""************************************************************
122 * Outline      : A/D convert
123 *-----------------------------------------------------------------------------
124 * Include      : #include "iodefine.h"
125 *-----------------------------------------------------------------------------
126 * Declaration  : void io_ad_1cyc_scan(unsigned short *ad_buf);
127 *-----------------------------------------------------------------------------
128 * Function     : The clearance of an ADF flag, storing of conversion data
129 *-----------------------------------------------------------------------------
130 * Argument     : void
131 *-----------------------------------------------------------------------------
132 * Return Value : void
133 *-----------------------------------------------------------------------------
134 * Notice       : non
135 *""FUNC COMMENT END""*********************************************************/
136 void io_ad_1cyc_scan(unsigned short *ad_buf)
137 {
138     ADC.ADCR.BIT.ADST = 1;            /* A/D conversion start */
139
140     while(ADC.ADSR.BIT.ADF == 0){
141     /* A/D conversion completion waiting */
142     }
143
144     ADC.ADSR.BIT.ADF = 0;         /* ADF clear */
145     *ad_buf++ = ADC.ADDR0;        /* AN0 */
146     *ad_buf++ = ADC.ADDR1;        /* AN1 */
147     *ad_buf++ = ADC.ADDR2;        /* AN2 */
148     *ad_buf++ = ADC.ADDR3;        /* AN3 */
149 }
150 /* End of File */
```

4. Documents for Reference

- Software Manual
  SH-2A/SH2A-FPU Software Manual
  The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
  SH7211 Group Hardware Manual
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