Ultra-low Power Low Voltage Lock-in Amplifier for Embedded Applications

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Introduction

The phase-sensitive or lock-in amplifier is capable of extracting excessively low signals in the presence of relatively high noise. In the past several years there has been an increased interest in portable or embedded lock-in amplifiers for instrumentation and sensing purposes. The fundamental approach of a lock-in amplifier is to make the physical quantity to be measured periodic, shifting the DC signal in this way to a known frequency and thus avoiding a high level of low-frequency flicker noise. In this App Note we will present the possibility of ultra-low power, low voltage (single supply), lock-in amplifier for portable or embedded applications circuitry design based only on the SLG88104 Rail to Rail I/O 375 nA Quad OpAmp and passive components.

The Lock-In Amplifier Circuitry

The block schematic of the proposed lock-in amplifier circuitry is presented in figure 1. The *Quadrature Oscillator* generates two phase shifted pulsed voltage signals *P* (in phase) and *Q* (in quadrature). The in phase signal is also used to power up the *Sensor*. The signal from the *Sensor* is amplified by the *Differential Preamplifier* and then brought to the inputs of *Amplifier* and *Multiplier* where it has been amplified (the overall signal processing chain has three relatively low gain amplifiers in order to keep large bandwidth) and multiplied by the in phase and in quadrature signals. After the multiplications, the signals have been added by the *Adder* in order to eliminate the possible phase shift of the *Sensor*. After the filtration by the low-pass *Filter* and amplification by the *Amplifier* the output signal V_{out} is proportional to the measured physical quantity.

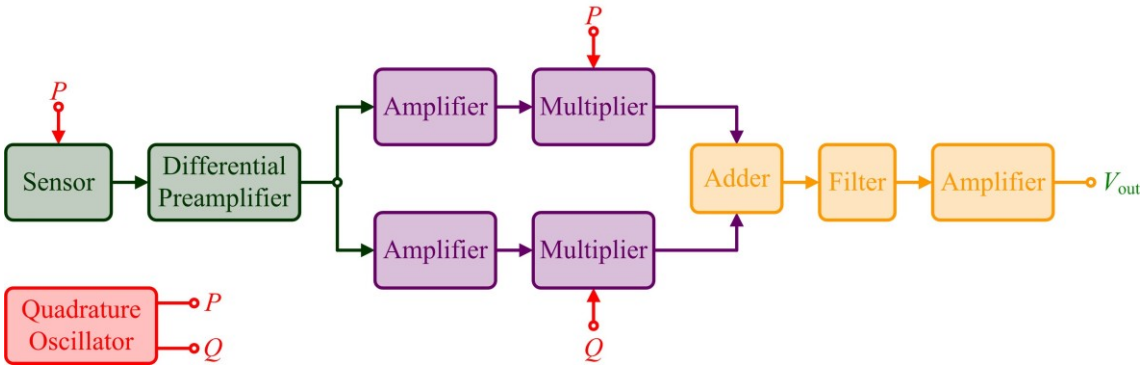


Figure 1. Block schematics of the proposed lock-in amplifier.

In order to fulfill all these requirements, the corresponding circuitry can be successfully produced based only on the SLG88104 Rail to Rail I/O 375 nA Quad OpAmp and passive components. For the complete circuitry, eight operational amplifiers (two SLG88104 chips) and a relatively low number of passive components (resistors and capacitors) are sufficient.

The corresponding signals of the presented lock-in amplifier block elements are depicted in figure 2. The first two time diagrams represent the output signals of the *Quadrature Oscillator*, which generates two phase shifted pulsed voltage signals with a phase shift of 90°. The voltage levels of these two signals are marked with logic levels “0” and “1”, since they serve to power up and down

(switch on and off) the corresponding operational amplifiers.

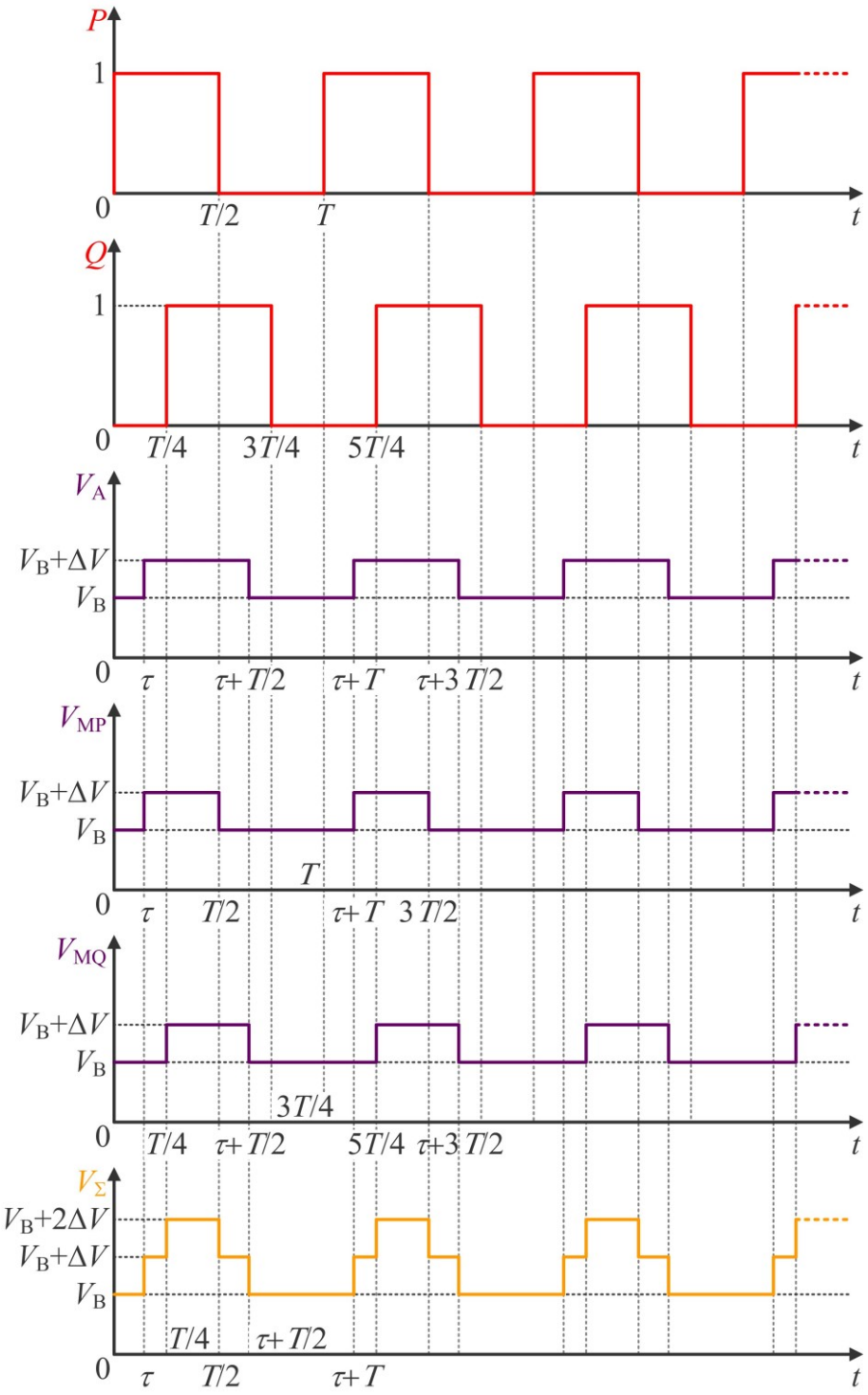


Figure 2. Time diagrams of the corresponding signals of the suggested lock-in amplifier.

The third diagram represents the time dependence of the voltage signals at the outputs of the second stage *Amplifier*s, which deliver the voltage signals to the *Multiplier*s inputs. These signals have the following value:

$$V_{\mathrm{A}}(t)=\begin{cases} V_{\mathrm{B}}, & \tau+\left(k+\frac{1}{2}\right)T<t\le\tau+(k+1)T \\ V_{\mathrm{B}}+\Delta V, & \tau+kT<t\le\tau+\left(k+\frac{1}{2}\right)T \end{cases}, \tag{1}$$

where $V_B = V_{DD}/2$ is the common mode voltage (virtual ground) of the circuitry and V_{DD} is the power supply voltage (we need virtual ground as we have single power supply), ΔV is the amplified *Sensor* signal with respect to the virtual ground, which is given by $\Delta V = GA_1V_S(t)$, where G is the *Differential Preamplifier* gain, A_1 is the second stage *Amplifier* amplification and $V_S(t)$ is the slow varying voltage signal at the *Sensor* output, τ is the time delay (or equivalently phase shift) of the *Sensor*, *Differential Preamplifier* and second stage *Amplifier*, T is the period of oscillation of the *Quadrature Oscillator*, and k is an arbitrary integer number.

After the multiplication that has been performed with the help of the *Multiplier*s, at their outputs we have voltage signals, which time dependences are depicted in the fourth and fifth diagrams of the figure 2. These signals have the following value:

$$\begin{aligned} V_{\mathrm{MP}}(t)&=\begin{cases} V_{\mathrm{B}}, & \left(k+\frac{1}{2}\right)T<t\le\tau+(k+1)T \\ V_{\mathrm{B}}+\Delta V, & \tau+kT<t\le\left(k+\frac{1}{2}\right)T \end{cases} \\ V_{\mathrm{MQ}}(t)&=\begin{cases} V_{\mathrm{B}}, & \tau+\left(k+\frac{1}{2}\right)T<t\le\left(k+\frac{5}{4}\right)T \\ V_{\mathrm{B}}+\Delta V, & \left(k+\frac{1}{4}\right)T<t\le\tau+\left(k+\frac{1}{2}\right)T \end{cases} \end{aligned}. \tag{2}$$

After the multiplication, the signals are added with the help of the *Adder* and at its output we have the following signal:

$$V_{\Sigma}(t)=\begin{cases} V_{\mathrm{B}}, & \tau+\left(k+\frac{1}{2}\right)T<t\le(k+1)T \\ V_{\mathrm{B}}+\Delta V, & \tau+kT<t\le\left(k+\frac{1}{4}\right)T\wedge\left(k+\frac{1}{2}\right)T<t\le\tau+\left(k+\frac{1}{2}\right)T \\ V_{\mathrm{B}}+2\Delta V, & \left(k+\frac{1}{4}\right)T<t\le\left(k+\frac{5}{4}\right)T \end{cases}. \tag{3}$$

The low-pass *Filter* at its output generates the average value of the input voltage signal, so the corresponding signal is given as:

$$V_{\mathrm{F}}=\frac{1}{T}\left\{V_{\mathrm{B}}\left[(\tau+T)-\left(\tau+\frac{T}{2}\right)\right]+(V_{\mathrm{B}}+\Delta V)\left[\left(\frac{T}{4}-\tau\right)+\left(\tau+\frac{T}{2}\right)-\frac{T}{2}\right]+(V_{\mathrm{B}}+2\Delta V)\left(\frac{T}{2}-\frac{T}{4}\right)\right\}. \tag{4}$$

The last equation reduces to:

$$V_{\mathrm{F}}=V_{\mathrm{B}}+\frac{3}{4}\Delta V, \tag{5}$$

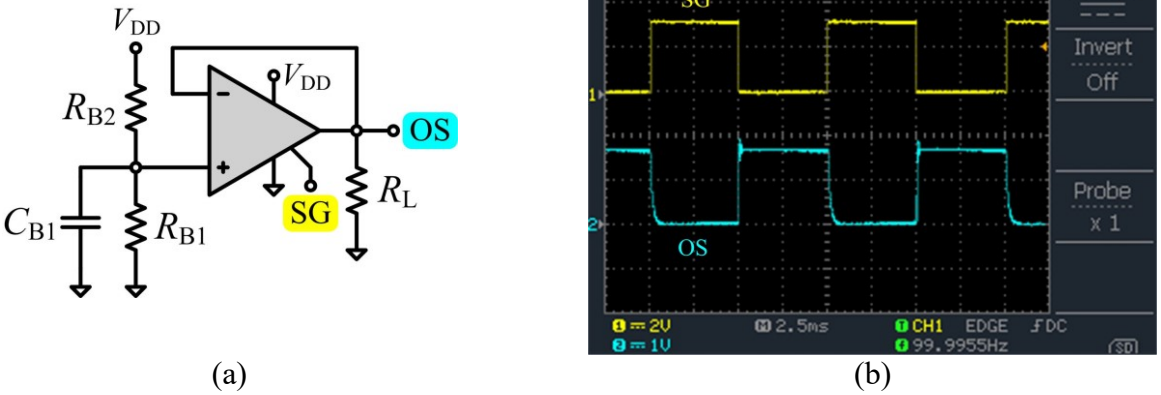
which gives the *Filter* output voltage signal that is independent on the time delay (phase shift) but only on the sensor signal. Finally, the output signal is amplified by the third stage *Amplifier*, where the output voltage is given by $V_{out} = A_2(V_F\text{-}V_B)$ and where A_2 is the third stage *Amplifier* amplification. Therefore, at the circuitry output we have the corresponding signal with respect to the virtual ground equal to:

$$V_F = \frac{3}{4} G A_1 A_2 V_S(t). \tag{6}$$

Realization with the SLG88104 Rail to Rail I/O 375 nA Quad OpAmp

The realization of the lock-in amplifier circuitry will be based on the unique characteristics of the SLG88104 Quad OpAmp. The use of these operational amplifiers will enable us to design low voltage, ultra-low power, low-noise circuitry that at its outputs will provide the voltage signal proportional to the measured physical value. Due to the unique characteristic of the phase-sensitive detection of the lock-in amplifier, the output voltage signal will provide very precise information about the measured physical value even if the high level of noise is present. It is worth mentioning that these operational amplifiers are sufficient for the complete design even in the case of multiplication where typically the analog multiplier or the analog switch have been used.

The design with the SLG88104 Quad OpAmp offers several advantages. First, it has a relatively low corner frequency of flicker noise. Based on the datasheet parameters, this corner frequency is estimated to be approximately 0.7 Hz. Therefore, we can use the quadrature oscillator frequency of only about 100 Hz (where the noise floor has been reached) that provides us the possibility of using large resistors in the design of the quadrature oscillator and thus ultra-low power consumption. This low oscillating frequency enables us also the possibility of designing the corresponding amplifiers with relatively large gains as the gain-bandwidth product of this operational amplifier is 10 kHz. Second, another important feature of the SLG88104 Quad OpAmp is the possibility of powering it down by the PD*i* (i = 1,2,3,4) inputs. This allows us to make a multiplication of the signal at the output of the *Differential Amplifier* and the corresponding in phase (P) and in quadrature (Q) signals from the pulsed *Quadrature Oscillator*. In order to prove this concept, we built a test circuit, as presented in figure 3. (a), where the corresponding signals of the signal generator (SG) and the output signal (OS) are depicted in figure 3. (b) The pulsed signal from the signal generator (SG) is brought to the PD input of the operational amplifier.



(a) (b)

Figure 3. Signal multiplication.

According to the captured oscilloscope image shown in figure 3 (b), one can notice that the signal multiplication is possible with the quadrature oscillator frequency of about 100 Hz. Therefore, there is no need of employing another analog voltage multiplier or analog switch since the SLG88104 has the possibility of such multiplication that can satisfy the needs of lock-in amplification.

Based on the analysis presented above and the block schematic, the suggested electrical schematic of the lock-in amplifier circuitry is given in figure 4.

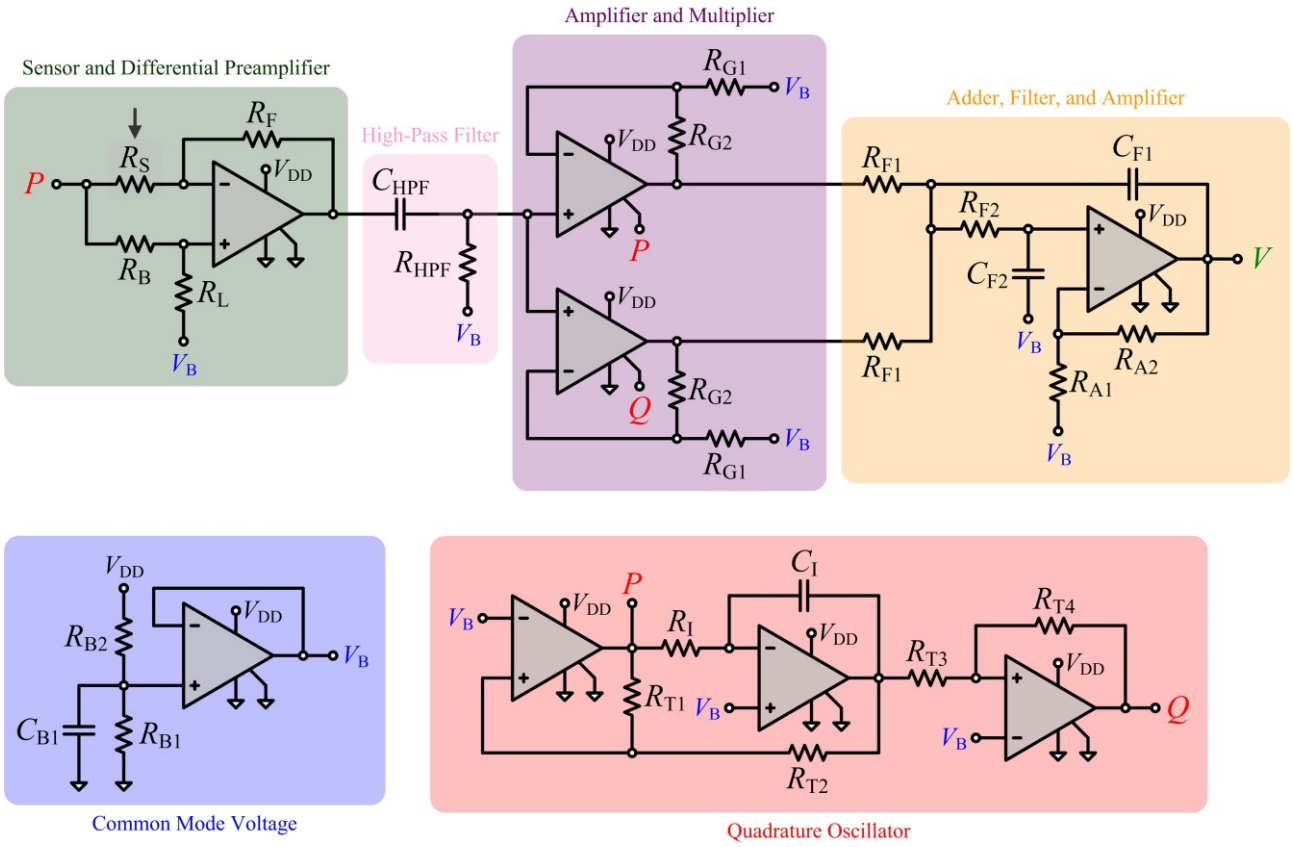


Figure 4. Electrical schematic of the proposed lock-in amplifier circuitry.

Regarding the input of the lock-in amplifier, it typically depends on the type of sensor used. For example, in figure 4., the resistive sensor R_S is used. This type of sensor changes its resistivity when some physical parameter such force, pressure, temperature, etc., acts on the sensor. The output of the lock-in amplifier is the voltage signal, which is proportional to the measured physical value. In order to describe in details the choices of the parameters of each part of the lock-in amplifier each of its segments will be separately analyzed in the following text.

Common Mode Voltage

The suggested circuitry has a single power supply that is made of a voltage source of V_{DD} = 3 V. This power supply can be made of two standard type batteries having 1.5 V each connected in series. In order to make a full span of the output voltage values, the common mode voltage (virtual ground) must have half of the value of the power supply voltage, or $V_B = V_{DD}/2$ = 1.5 V. Therefore, the resistor values R_{B1} and R_{B2} must be the same and must have large values in order to reduce power consumption. The chosen values of these resistors are: $\boldsymbol{R_{B1} = R_{B2} = 1\ M\Omega}$. Capacitor C_{B1} serves to

filter the noise and must also have a large value. In the suggested design the capacitor $\boldsymbol{C_{B1}}$ was realized as the parallel connection of two capacitors having the values **100 µF** and **220 nF**.

Quadrature Oscillator

As mentioned earlier, *Quadrature Oscillator* serves to generate two pulsed, phase shifted voltage signals for gating the corresponding operational amplifiers. In order to reduce the power consumption, the resistors R_I, R_{T1}, R_{T2} and R_{T4} must have large values. In the suggested design, based on the circuit testing, the following values have been chosen: $\boldsymbol{R_{T1} = R_{T2} = R_{T4} = 1\ M\Omega}$ and $\boldsymbol{R_I = 700\ k\Omega}$. In order to have oscillating frequency near to 100 Hz the capacitor value has been chosen to be $\boldsymbol{C_I = 2.2\ nF}$. In general case, the oscillating frequency can be estimated according to the following relation:

$$f_{QO} = \frac{1}{4R_I C_I}\frac{R_{T1}}{R_{T2}}, \tag{7}$$

which is equal to $f_{QO} \approx 162$ Hz for the suggested resistors and capacitor values. The resistor R_{T3} doesn't need to have large value. In order to reduce the hysteresis of the Schmitt trigger and thus to reduce the additional phase shift of the in quadrature signal, the resistor value must be low or as chosen $\boldsymbol{R_{T3} = 1\ k\Omega}$. Further, in order to prove the concept of the quadrature oscillator as presented in figure 4, a simulation has been performed with results presented in figure 5. Here we can easily see that in phase (*P*) and in quadrature (*Q*) signals are phase shifted for 90° and with the frequency of 135 Hz.

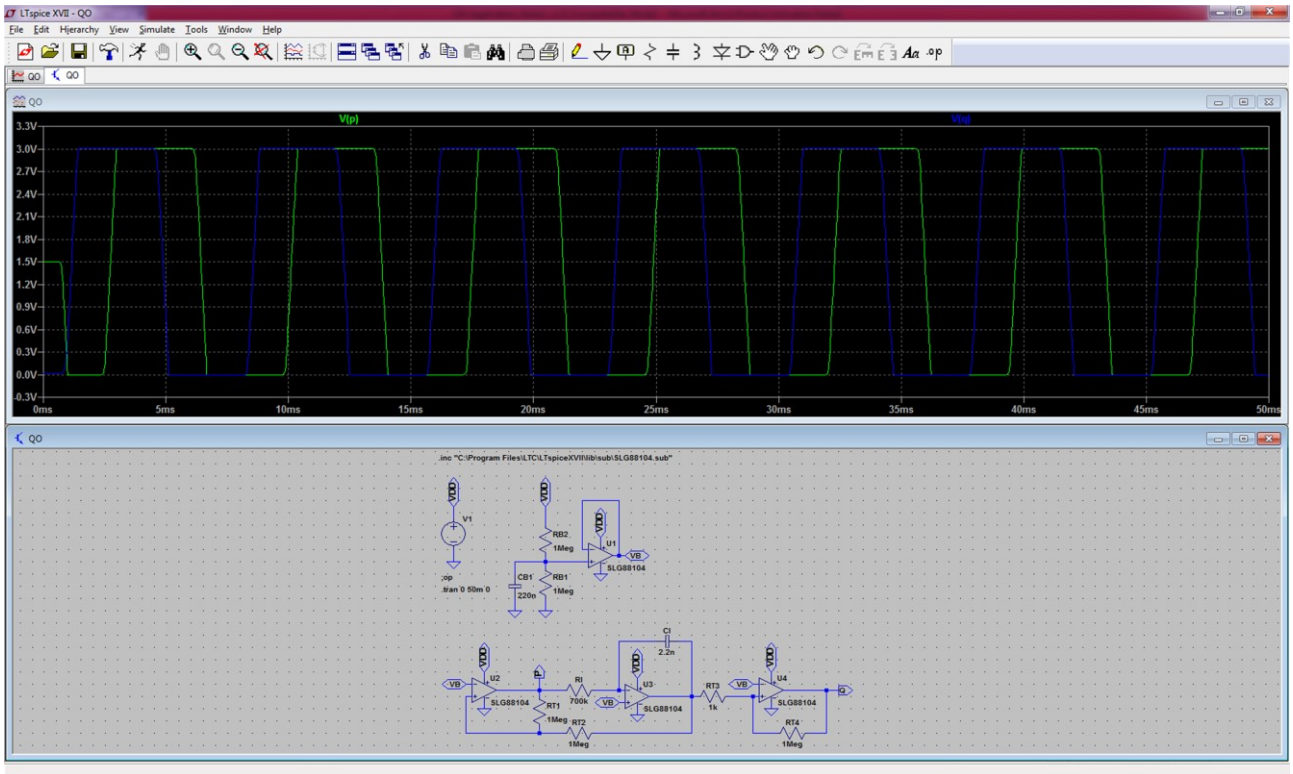


Figure 5. Quadrature oscillator simulation results.

Differential Preamplifier

The suggested *Differential Preamplifier* has the topology that the resistive sensor R_S is incorporated in it. As the power consumption of the circuitry is a major concern, the values of the resistors R_F and R_L have been chosen to be large enough, i.e. $\boldsymbol{R_F = R_L = 1\ M\Omega}$. The values of the resistors R_S (the sensor) and R_B must be chosen in a way that the *Differential Preamplifier* is capable of amplifying a pulsed signal with a frequency greater than 100 Hz without distorting it. Therefore, the optimal values of these resistors are $\boldsymbol{R_S = R_B \approx 100\ k\Omega}$. A bandwidth of approximately 1 kHz has been achieved in the case of the such designed *Differential Preamplifier*. The output signal of the *Differential Preamplifier* with respect to the power supply negative node is given by:

$$V_{DP} = \frac{R_B}{R_S}\frac{R_S + R_F}{R_B + R_L}V_B + \left(\frac{R_L}{R_S}\frac{R_S + R_F}{R_B + R_L} - \frac{R_F}{R_S}\right)P\,. \tag{8}$$

Typically, the sensor resistance R_S varies with respect to its nominal value as:

$$R_S = R_{S0} + \Delta R_S\,, \tag{9}$$

where R_{S0} is the sensor nominal resistance and ΔR_S is the resistance variation caused by some physical quantity to be measured. In the case where $\Delta R_S << R_{S0}$ and $R_{S0} = R_B$ is met, we have:

$$V_{DP} \approx \left[1 - \frac{R_F}{R_{S0}\left(R_{S0} + R_F\right)}\Delta R_S\right]V_B + \frac{R_F}{R_B + R_L}\frac{\Delta R_S}{R_{S0}}P\,. \tag{10}$$

High-Pass Filter

According to equation (10) the *Differential Preamplifier* output signal consists of two parts, the slow varying part proportional to the common mode voltage V_B and the fast varying part proportional to the in phase signal P. The role of the *High-Pass Filter* is to remove the slow varying signal and also the offset voltage as well as the low frequency flicker noise of the *Differential Amplifier*. Therefore the signal at the filter output is given by:

$$V_{HPF} \approx \frac{R_F}{R_B + R_L}\frac{\Delta R_S}{R_{S0}}P' + V_B\,. \tag{11}$$

where P' is the time delayed (i.e. phase shifted) version of the in phase signal P, i.e. $P'(t) = P(t\text{-}\tau)$, where τ is the time delay of the *Differential Preamplifier* and *High-Pass Filter* combined, which is in this case very small as compared to the period of the *Quadrature Oscillator* and V_B is the voltage that was added due to the virtual ground of the *High-Pass Filter*. In order to achieve cut-off frequency of about 1 Hz and low output current of the *Differential Preamplifier,* the following values were chosen: $\boldsymbol{C_{HPF} = 220\ nF}$ and $\boldsymbol{R_{HPF} = 1\ M\Omega}$.

Amplifier and Multiplier

The *Amplifier and Multiplier* has a dual role, i.e. to simultaneously amplify the signal from the *High-Pass Filter* and to perform digital multiplication by gating the operational amplifiers. The output signals of the *Amplifier and Multiplier* are given by:

$$\begin{aligned} V_{\mathrm{AMP}} &\approx \left(1+\frac{R_{\mathrm{G2}}}{R_{\mathrm{G1}}}\right)\frac{R_{\mathrm{F}}}{R_{\mathrm{B}}+R_{\mathrm{L}}}\frac{\Delta R_{\mathrm{S}}}{R_{\mathrm{S0}}}P'\overline{P}+V_{\mathrm{B}} \\ V_{\mathrm{AMQ}} &\approx \left(1+\frac{R_{\mathrm{G2}}}{R_{\mathrm{G1}}}\right)\frac{R_{\mathrm{F}}}{R_{\mathrm{B}}+R_{\mathrm{L}}}\frac{\Delta R_{\mathrm{S}}}{R_{\mathrm{S0}}}P'\overline{Q}+V_{\mathrm{B}} \end{aligned}, \tag{12}$$

where $\overline{P}$ and $\overline{Q}$ are inverted digital signals of the *Quadrature Oscillator* in phase *P* and in quadrature *Q* signals, respectively. The inverted versions of the signals were taken into account as the operational amplifier powers off when its PD input is connected to the high level signal. The inverted signals $\overline{P}$ and $\overline{Q}$ are also in quadrature. In order to achieve relatively high gain without distorting the signal and simultaneously keeping low power consumption, the following values for the resistors were chosen: $\boldsymbol{R_{G1}}$ **= 100 kΩ** and $\boldsymbol{R_{G2}}$ **= 1 MΩ**.

Adder, Filter, and Amplifier

Adder, Filter, and Amplifier has a triple role, i.e. to simultaneously sum the output signals of the *Amplifier and Multiplier*, to perform low-pass filtration and to additionally amplify the signal. The sum of the signals occurs at the common node of the resistors R_{F1} and R_{F2}, which also serve as the low-pass filter components. According to the Thévenin's theorem, at this particular node, the signal has the following value:

$$V_{\Sigma}=\frac{1}{2}\left(V_{\mathrm{AMP}}+V_{\mathrm{AMQ}}\right)\approx\frac{1}{2}\left(1+\frac{R_{\mathrm{G2}}}{R_{\mathrm{G1}}}\right)\frac{R_{\mathrm{F}}}{R_{\mathrm{B}}+R_{\mathrm{L}}}\frac{\Delta R_{\mathrm{S}}}{R_{\mathrm{S0}}}\left(P'\overline{P}+P'\overline{Q}\right)+V_{\mathrm{B}}\,. \tag{13}$$

Finally, after the filtration and additional amplification, the output signal, with respect to the virtual ground (V_B), i.e. we measure the output signal deviation from the common mode voltage, has the following value:

$$V\approx\alpha V_{\mathrm{DD}}\left(1+\frac{R_{\mathrm{G2}}}{R_{\mathrm{G1}}}\right)\left(1+\frac{R_{\mathrm{A2}}}{R_{\mathrm{A1}}}\right)\frac{R_{\mathrm{F}}}{R_{\mathrm{B}}+R_{\mathrm{L}}}\frac{\Delta R_{\mathrm{S}}}{R_{\mathrm{S0}}}\,, \tag{14}$$

where the analysis of the lock-in amplification signal processing chain, as presented in figure 1, has been considered, and where α is the proportionality factor which value depends on the operational amplifier gating process (switch on and off). In order to keep low power consumption, sufficient amplification and filtration with the second order Butterworth filter with approximately 1 Hz of the cut off frequency, the following values have been chosen: $\boldsymbol{R_{A1}}$ **= 100 kΩ**, $\boldsymbol{R_{A2}}$ **= 1 MΩ**, $\boldsymbol{R_{F1}}$ **= 2 MΩ**, $\boldsymbol{R_{F2}}$ **= 1 MΩ**, $\boldsymbol{C_{F1}}$ **= 56 nF**, and $\boldsymbol{C_{F2}}$ **= 390 nF**.

Example Implementation

We built the test circuitry setup based on two evaluation boards for the SLG88104 Quad OpAmp and the NTC thermistor for temperature measurement B57164K0104 from TDK Corporation, which is available for the price of about $1 USD. The photo of the proto-board realized circuitry and the complete measurement and test setup is given in figure 6. The photo of the circuitry only is presented in figure 7., where the lower evaluation board is used for the realization of the common mode voltage

(virtual ground) and the quadrature oscillator, and the upper evaluation board is used for realization of differential preamplifier, amplifiers and multipliers, adder, filter and amplifier.

In order to test the circuitry for temperature measurements we placed the NTC thermistor together with the calibration thermocouple into the test tube thus ensuring the same temperature of both sensors. The test tube is immersed into the water bath that was previously heated and then left to cool down. The temperature was also checked with the help of a control thermometer. The thermocouple temperature was measured with the digital multimeter that was also used for simultaneous measurement of the circuitry output signal.

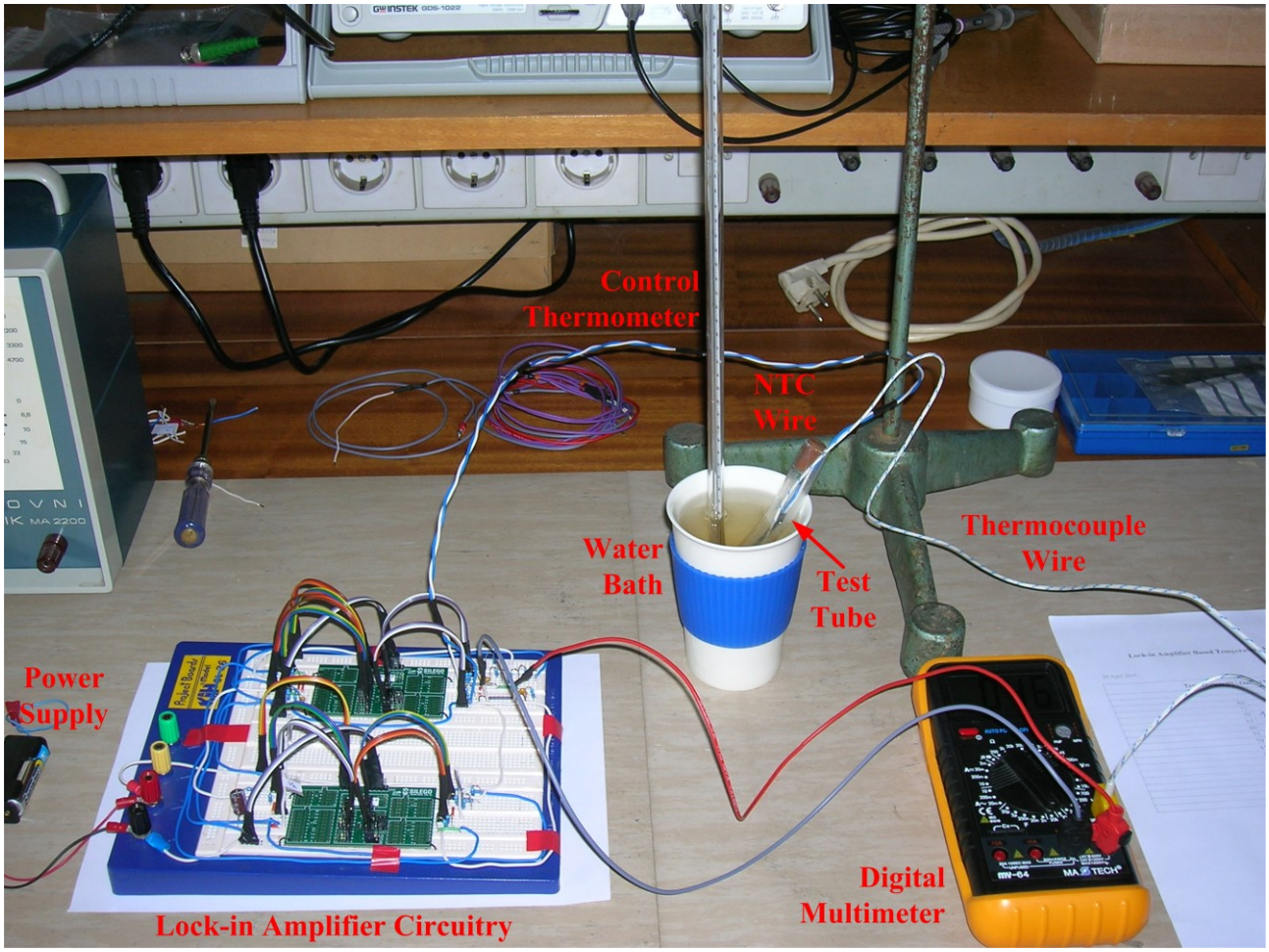


Figure 6. The photo of the proto-board realized circuitry and the complete measurement and test setup.

The NTC thermistor resistance changes with the absolute temperature change in the following way:

$$R_S(T) = R_{S0} \exp\left[-B\left(\frac{1}{T_0} - \frac{1}{T}\right)\right], \tag{15}$$

where R_{S0} is the thermistor nominal resistance at the absolute temperature T_0 and B is the thermistor parameter. For the thermistor used we have: R_{S0} = 100 kΩ, T_0 = 298.15 K (+25°C), and B = 4600 K. Based on equation (15), the thermistor sensitivity for a narrow temperature range around the nominal temperature T_0 can be defined as:

$$S = \frac{\partial R_S(T)}{\partial T}\bigg|_{T=T_0} = -\frac{BR_{S0}}{T_0^2}, \tag{16}$$

where the thermistor resistance change can be defined as:

$$\Delta R_S \approx S\Delta T = -\frac{BR_{S0}}{T_0^2}\Delta T, \tag{17}$$

where ΔT is the thermistor temperature change with respect to the nominal temperature.

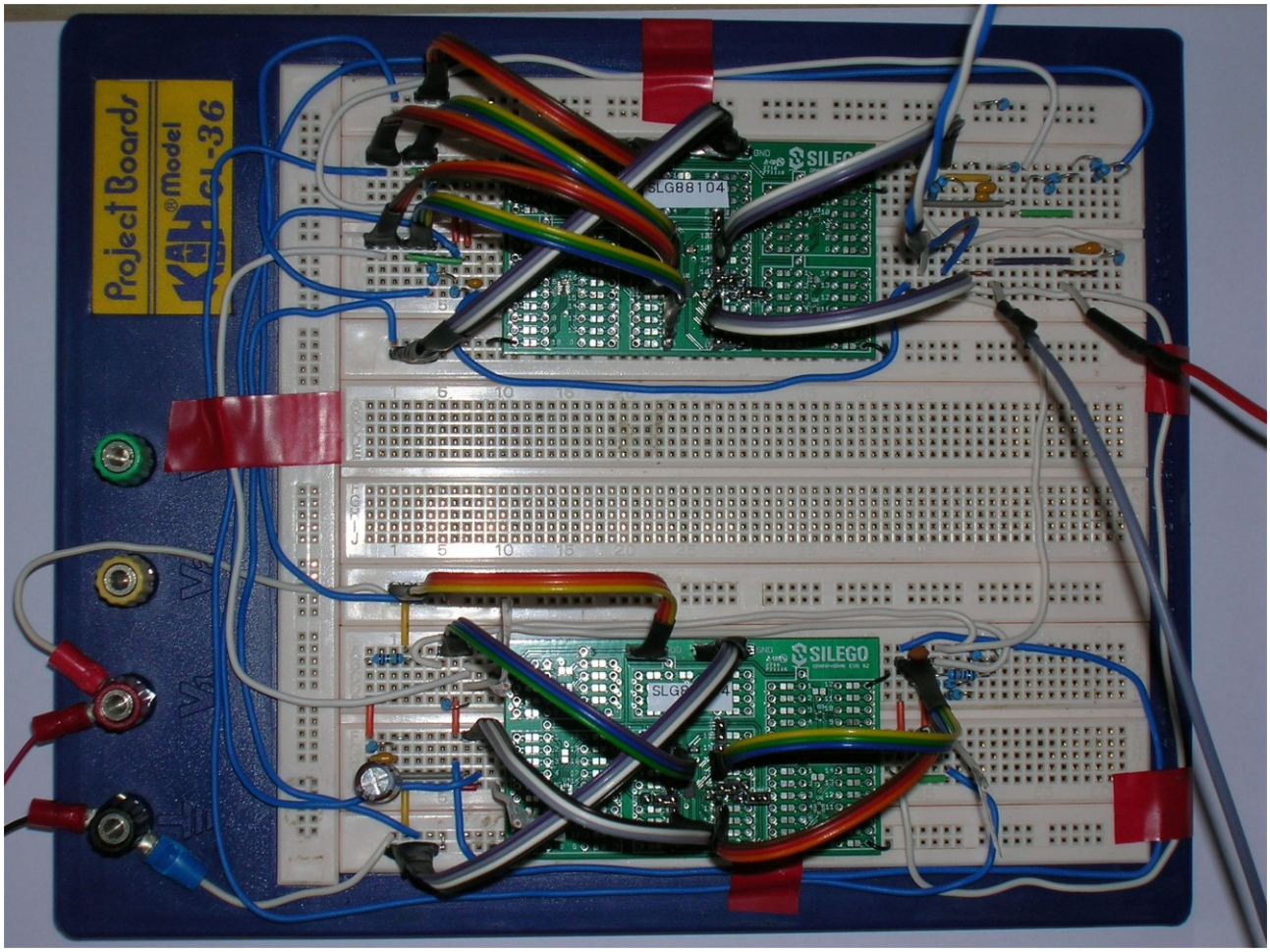


Figure 7. The photo of the circuitry only.

From equations (14) and (17) we have:

$$V = K\Delta T, \tag{18}$$

where K is the sensitivity of the sensing system. As the water bath was slowly cooled, the temperature was captured simultaneously with the thermocouple and digital multimeter and with the NTC thermistor in tandem with the presented sensor circuitry. The output voltage was also measured by the digital multimeter and the results are presented in figure 8. The temperature sampling was performed periodically. The temperature range that is possible to measure with this circuitry is from +17°C to +32°C because the circuitry reaches saturation voltages of ±1.575 V at these minimum and maximum temperatures. The measured sensitivity was obtained according to the diagram presented

in figure 8 and it is estimated to be $K \approx 0.22$ V/°C.

We tested the proposed design of the quadrature oscillator, whose outputs are presented in figure 9. One can notice from figure 9. that the quadrature oscillator output signals (in phase P and in quadrature Q) are phase shifted for approximately 90° and the oscillating frequency is approximately 130 Hz, which is very close to the simulated value of 135 Hz.

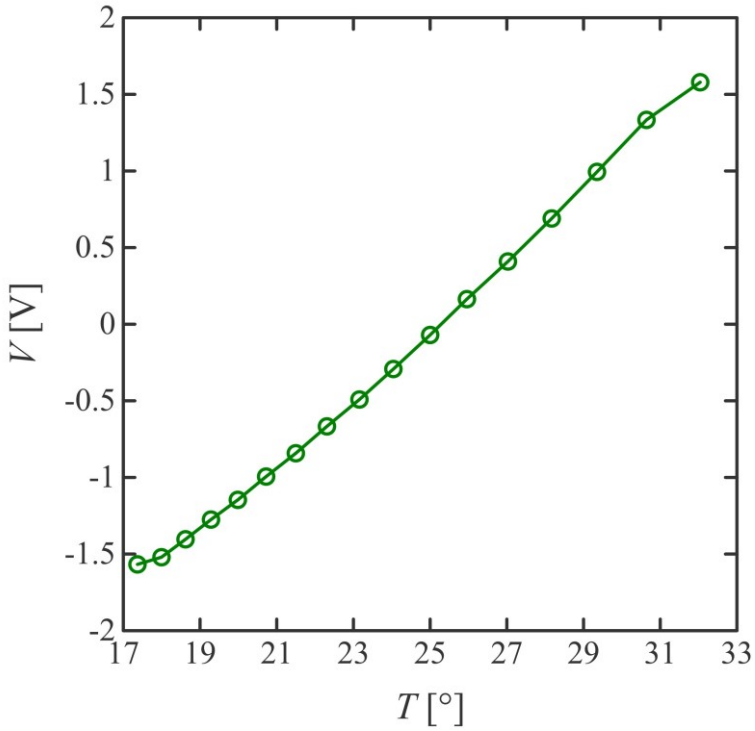


Figure 8. Temperature measurement with the NTC thermistor and suggested lock-in amplifier circuitry.

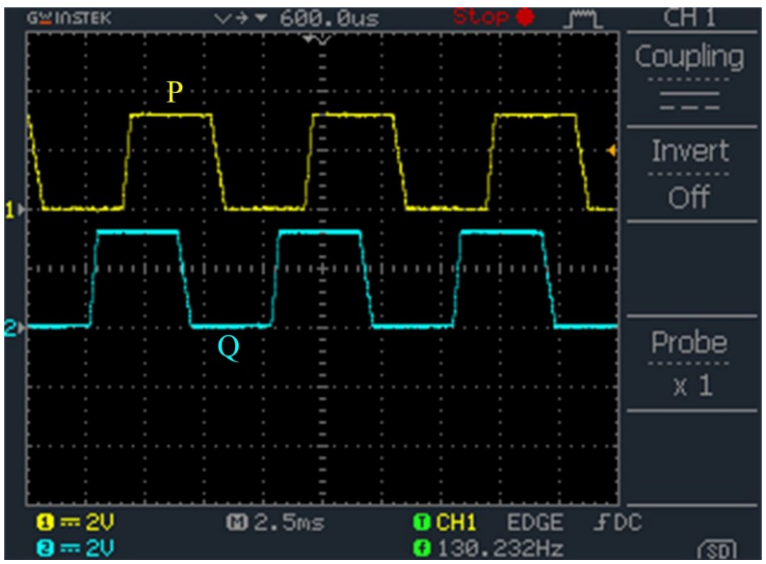


Figure 9. Quadrature oscillator output signals.

The most prominent feature of the lock-in amplification is the suppression of the high levels of low frequency flicker noise that cannot be seen from the above presented work. The aim of the above presented measurements is to prove the concept of such a designed lock-in amplifier. As shown, it is possible to measure a real physical quantity, such as the temperature, with the help of an appropriate

sensor and the proposed ultra-low power low voltage lock-in amplifier circuitry. In order to test the noise suppression of the lock-in amplifier, long-term stability of the circuitry was performed. Instead of NTC thermistor, a dummy metal film resistor with the same resistance as the nominal resistance of the thermistor was employed. In this way, we test the stability only of the lock-in amplifier thus eliminating the influence of the sensor, which is irrelevant for this measurement. The output lock-in amplifier voltage has been measured for 24 hours in a non-air-conditioned room. During the measurement, the room temperature was changed in the range from +17°C to +23°C. The output signal was sampled with the help of a 12-bit digital acquisition card with a sampling frequency of 2 Hz (bandwidth of the lock-in amplifier is approximately 1 Hz). The input voltage range of the digital acquisition card was set to ±2 V (full scale range $FSR = 4$ V) thus providing the resolution (less significant bit value) of $LSB = FSR/(2^n\text{-}1) = 0.977$ mV (for $n = 12$ bits resolution). The measured voltage is presented in figure 10.

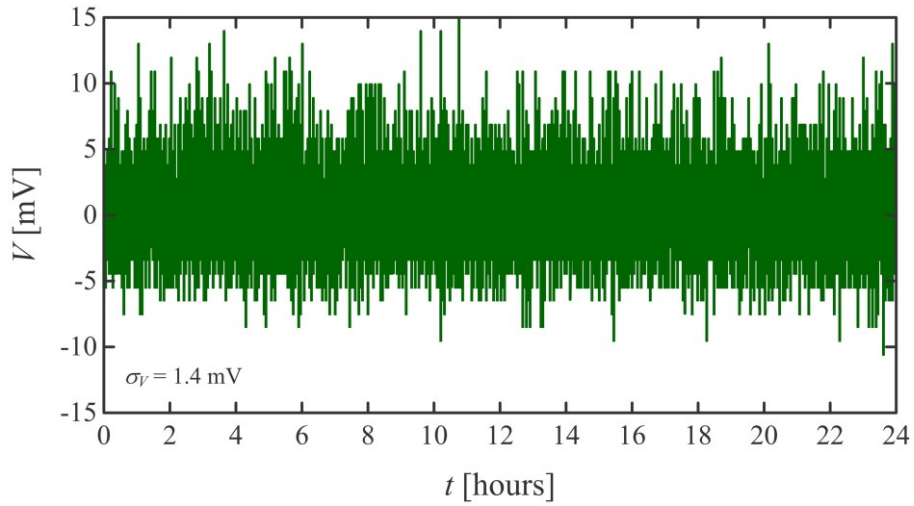


Figure 10. Output noise signal of the lock-in amplifier.

The measured standard deviation of the lock-in amplifier output noise signal is $\sigma_V = 1.4$ mV. Taking into account that the overall sensor sensitivity in temperature measurement with the presented NTC thermistor is $K \approx 0.22$ V/°C, the resolution in the temperature measurement is equal to $\sigma_T = \sigma_V/K \approx 0.0064$°C. Bearing in mind that the digital acquisition card quantization noise standard deviation is given by $\sigma_Q = LSB/\sqrt{12} = 0.28$ mV, we have fulfilled $\sigma_V^2/\sigma_Q^2 \approx 25 >> 1$, and as the noises of the lock-in amplifier and the digital acquisition card are independent (two independent devices), one can conclude that all the measured noise originates from the lock-in amplifier. The power spectral density of the measured output noise signal, presented in figure 10., is presented in figure 11.

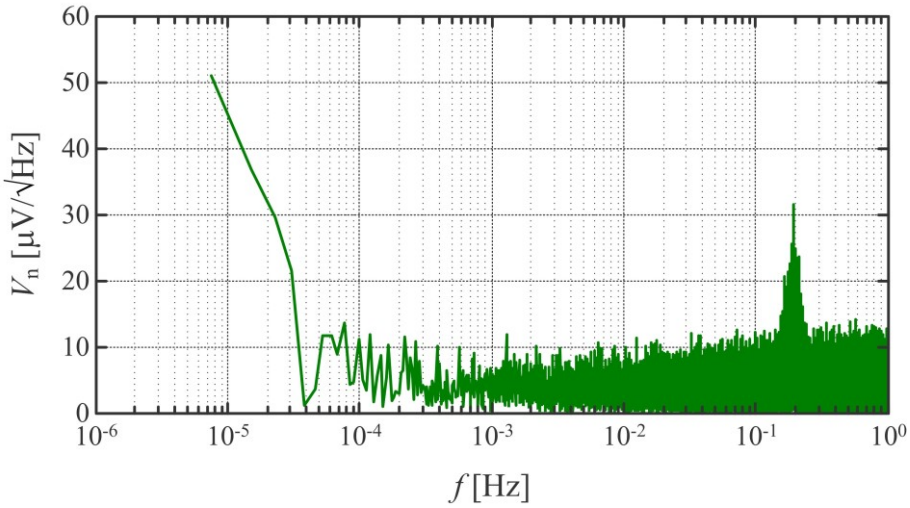


Figure 11. Power spectral density of the measured output noise signal.

The presented power spectral density spans from1 μHz up to 1 Hz, which is deeply located in the range of the flicker noise of the SLG88104 Quad OpAmp (as can be seen from the datasheet flicker noise corner frequency is approximately located at 0.7 Hz). One can expect that in this range we have an increase in the noise power spectral density starting from 1 Hz and going toward lower frequencies. However, this cannot be observed in the measured output noise power spectral density. Moreover, the power spectral density decreases as approaching lower frequencies. There is only a sharp increase in the power spectral density at very low frequencies (~2×10^{-5} Hz – ~7×10^{-6} Hz). The reason for this increase is limited only by the measurement time (measurement was performed for 24 hours). One can estimate the noise floor of the lock-in amplifier output noise at approximately $V_n \approx 10$ μV/√Hz, which translates to the noise floor of about $T_n \approx 45$ μ°C/√Hz in the temperature measurement. We have also obtained a noticeable noise source at 0.2 Hz (as can be seen from figure 11.) of unknown origin.

Finally, in order to prove the ultra-low power consumption statement, we measure the bias current of the circuitry. It was measured that the complete circuitry consumes 16 μA, which in combination with the measured power supply voltage of 3.15 V gives the overall power consumption of approximately 51 μW. This low value can be decreased even more with the help of the larger resistance values (larger than 1 MΩ). However, larger resistance values are followed by correspondingly larger voltage noise. Based on the datasheet parameters, the input voltage noise density of the SLG88104 is 195 nV/√Hz, which is still larger than the voltage noise density of a 1 MΩ resistor that is equal to 129 nV/√Hz.

Conclusion

The ultra-low power low voltage lock-in amplifier circuitry we described in this App Note is capable of providing high performance measurement that offers phase sensitive measurement. Flicker noise, which is the predominant noise component in any sensing system aimed for measuring slowly varying physical values such as temperature, force, pressure, etc. is effectively suppressed by the suggested design. The introduction of this low voltage, ultra-low power measurement system that can be easily battery powered, now opens broad new applictions. Furthermore, the circuitry has a very unique design that can be tested with different types of sensors thus proving the concept of the circuit design. Moreover, the result of this test can be used in order to improve the design in a way to reach higher-precision and wider bandwidth. Finally, by choosing larger resistor values one can further reduce the power consumption with the tradeoff of increased noise and lower measurement resolution.

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