## Introduction

An AC power mains utility frequency is typically either 50Hz or 60Hz. The frequency variation is normally restricted to about +/- 1% in most countries. Variation occurs usually because of varying load on the grid; a higher load causes the frequency to drop and vice versa. The importance of monitoring power frequency is especially important when a local minigrid is set up – such as with solar-powered or wind-powered installations. The inverter in such cases must shoulder the responsibility of monitoring the output power quality.

In industrial setups that use equipment such as induction motors, it is important to maintain the proper frequency because the speed of an induction motor is a function of the frequency. More elaborate and sensitive setups may use AC drives to maintain the motor speed, but in many situations the motor may be directly connected to the power source without a drive, in which case variations in power frequency directly impact the motor speed.

In this application note we show how to use a GreenPAK SLG46620V and a few external components to design a frequency deviation monitor that signals an alert if the frequency deviates by a specified margin.

## Broad Design Strategy

The design is based on measuring the period of the waveform. Many designs use a zero-crossing detector as the basis for period measurement. The mains input is stepped down and half-wave rectified with a few components as shown in Figure 1. The rectified pulses are fed to the GreenPAK chip and used to trigger an analog comparator (ACMP) reading at Pin 12. The ACMP's IN terminal is held at 50mV, and when it toggles, it enables a counter which counts pulses from an internal oscillator until the end of the half-cycle. The ACMP's low-bandwidth mode is enabled to prevent spurious responses due to noise.
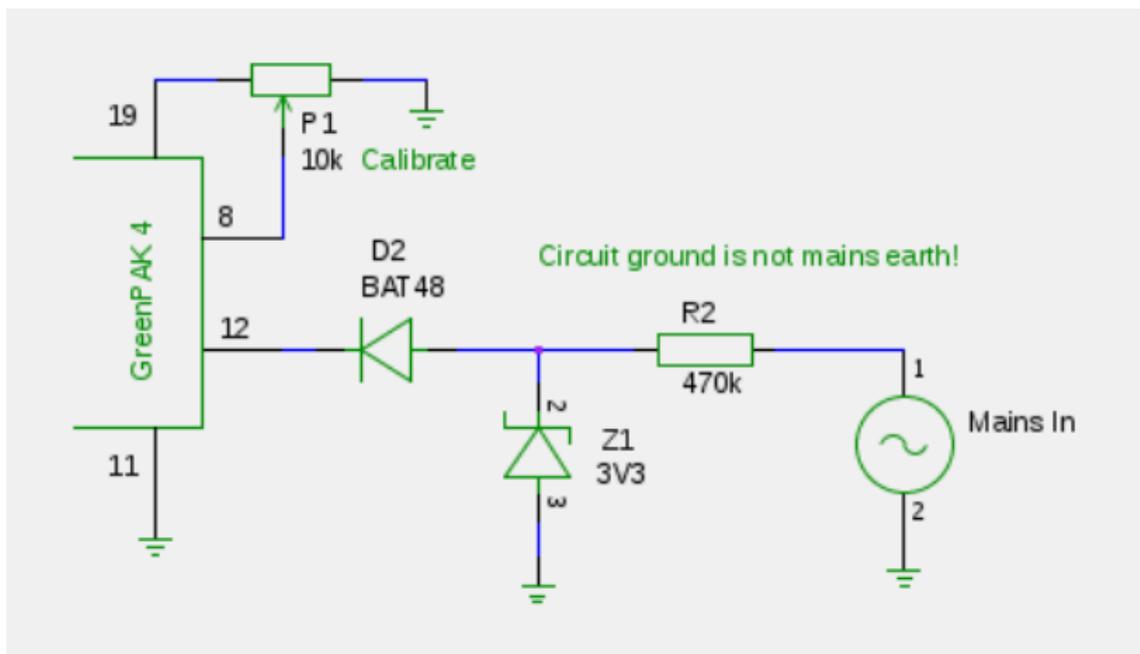


**Figure 1. Suggested input schematic**

To determine whether the deviation of the mains input frequency is acceptable, we use two DCMPs to compare the output of the counter at the end of the half-cycle with two registers which store the upper and lower bounds we are interested in. DCMPs are available in the GreenPAK 4 series, and therefore we select the SLG46620V for this application note.

The graph in Figure 2 shows the first few microseconds of the half-wave cycle for a 230V, 50Hz waveform (black curve). The error introduced by the use of a half-wave rectifier in the above fashion is quite small. Given the presence of the protective Schottky diode BAT48 at the input, we need a voltage of at most 350mV to trigger the ACMP. The time taken for the mains voltage to reach a level of 350mV is about 3.6us; double that to account for the ramp-down as well, and we have a 0.07% error which can be neglected in most mains frequency monitoring applications. The output of the ACMP is shown by the red line in Figure 2.

## Realization with the GreenPAK Designer

Figures 3 and 4 show the GreenPAK design. The broad idea is to drive the SET input of FSM1 low when the mains half-cycle starts, and bring it back high when the half-cycle ends. When the halfcycle ends, the rising edge produced by INV1 feeds into DFF6/7/8, locking the DCMPs' states into pins 14, 16 and 17 respectively, after which the rising edge (delayed slightly by DLY7), sets FSM1.

To make the above strategy work in practice, we need to work around a couple of things. Firstly, we note that the GreenPAK 4's DCMP works with 8-bit data, which offers us a resolution of only 1 part in 256. What if we are interested in better accuracy than this? Secondly, the internal oscillator is not as accurate as a crystal oscillator so if we need to keep the external parts count really low we need a method of calibrating the frequency monitor. We will describe how both these are achieved.
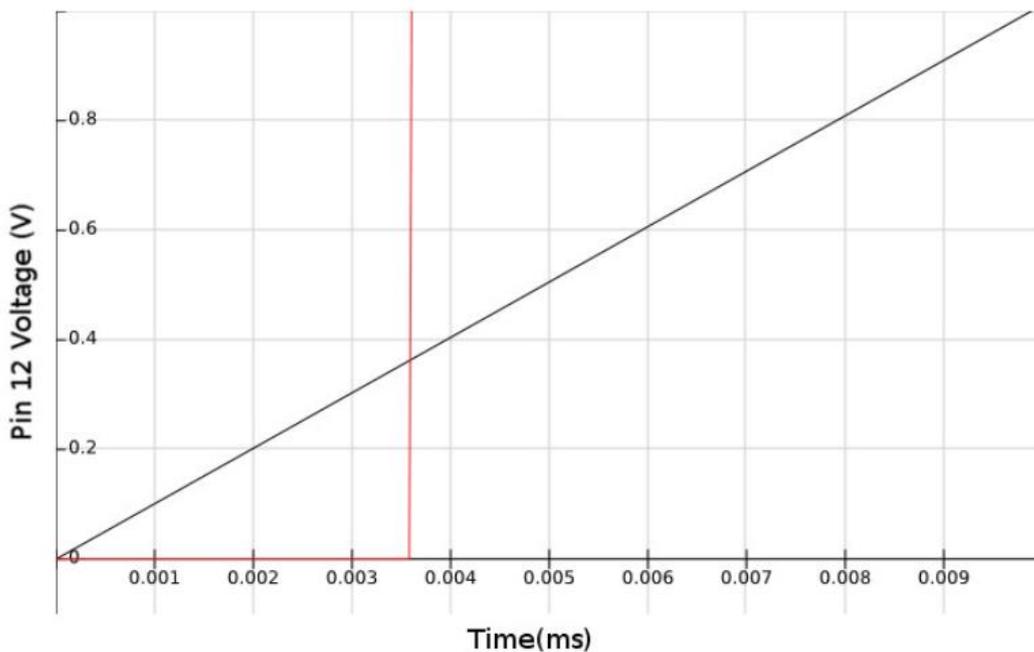


**Figure 2. The first few microseconds of a 230V 50Hz mains waveform**

## Oscillator and Counter Design

We choose OSC's 2MHz RC oscillator. The OSC output divider and the FSM1 clock input divider are set to 2 and 4 respectively so that the counter frequency is now 2000/8 = 250kHz (period = 4us). Let us see what happens with a nominal mains frequency of 50Hz, with the half cycle being 10ms. Suppose FSM1 is configured to count UP with counter data = 0. Then at the end of the 10ms half-cycle, the Q output of FSM1 will be 10ms/4us = 2500 modulo 256 = 196. Let us call this the "STOP value" for further discussion.

However, we now need to take cognizance of the error in the oscillator frequency. From the device's datasheet we see that if the SLG46620V operates at a supply voltage of 3.3V, the frequency tolerance of the 2MHz RC oscillator at 25° C is -1.74% / +1.55%.

Instead of adding an external crystal oscillator, we show how we can institute a calibration procedure to compensate for this variation in an actual implementation.

As a first step towards achieving this, we design things with an assumed OSC frequency that is at the upper end of the range (or a little beyond, to account for minor temperature variations). In other words, we design things in such a way that if the OSC frequency error was +2%, then the STOP value would be 128, which is the midpoint of the possible range 0-255 of the STOP value. Knowing that the OSC error is actually less than 2%, what this implies is that the actual STOP value will be (slightly) less than 128. The next step is to have a trimmer external to the GreenPAK which may be tweaked to "push" the actual STOP value to 128 when the input frequency is known to be exactly 50Hz.
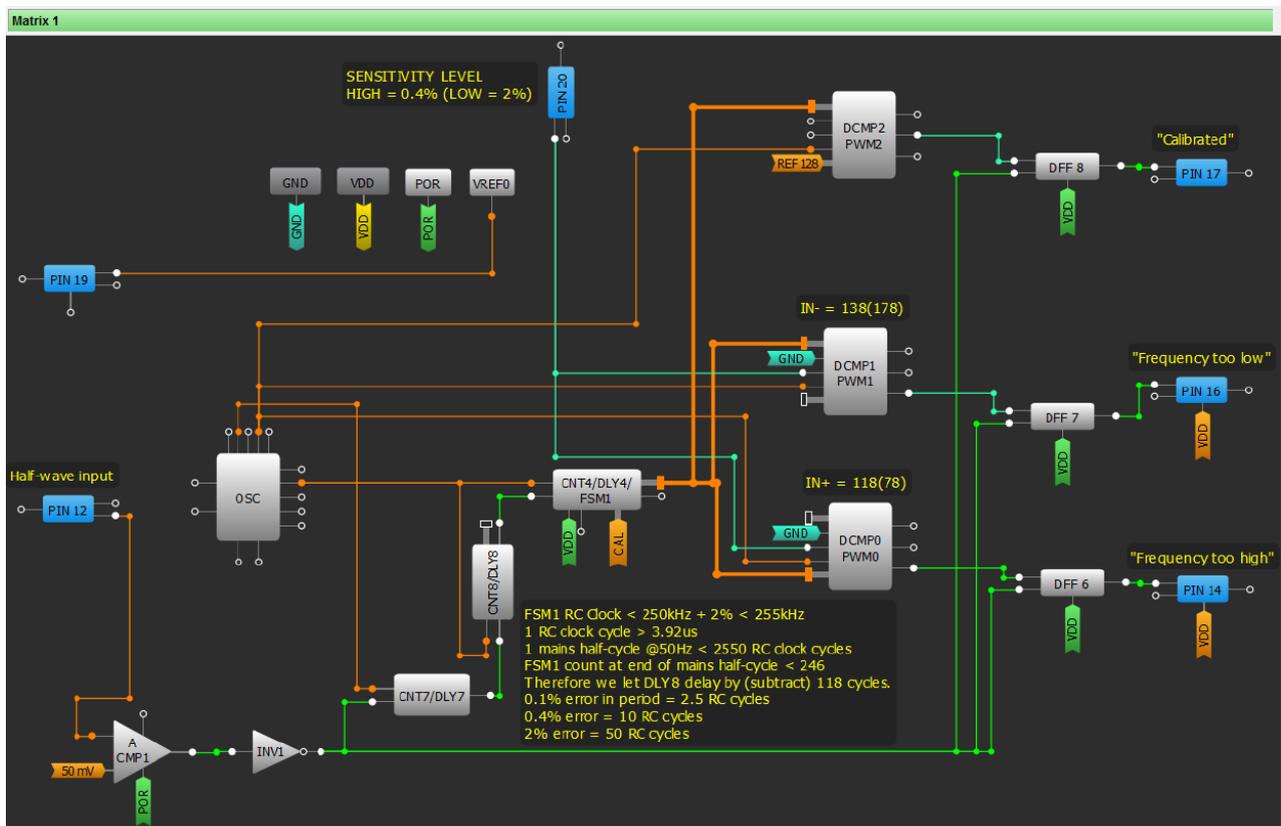


**Figure 3. GreenPAK Design - Matrix 1**

This would give us a practical calibration procedure that can be used in the field.

Let us now work out the numbers and calculate the STOP value:

Assumed OSC RC frequency = 2040kHz/8 = 255kHz

> One RC clock cycle = 3.92us
>
> STOP value after 10ms = 246.
>
> Delay introduced by DLY8 = 118 cycles
>
> New STOP value = 246-118=128 (1)

which is as desired.

## Field Calibration

When the actual OSC frequency is less than 2040 kHz, the STOP value will be somewhat less than 128. How do we now "push" the STOP value using an external trimmer?

Enter the ADC (Figure 4). The ADC takes an analog voltage from Pin 8 and generates a digital value labelled CAL, which is used by FSM1 as its counter data. When the input voltage at Pin 8 is zero, the CAL value is zero. As we increase the voltage, the CAL value increases. Since FSM1 starts counting at the CAL value rather than at zero when it receives a SET signal, the STOP value also increases. We now have the following procedure for field calibration when the input signal is known to be at 50.00Hz: the Pin 8 voltage is increased slowly from zero till the STOP value touches 128. At that point, DCMP2, whose IN- pin is fed with the constant reference value of 128 generated by FSM0, outputs a signal on its EQ output which lights up an LED on Pin 17 indicating that the unit is calibrated.

The calibration input voltage for Pin 8 may be conveniently generated by using the VREF microcell to output a reference voltage of 1V on Pin 19 and using a trimmer as shown in Figure 1.
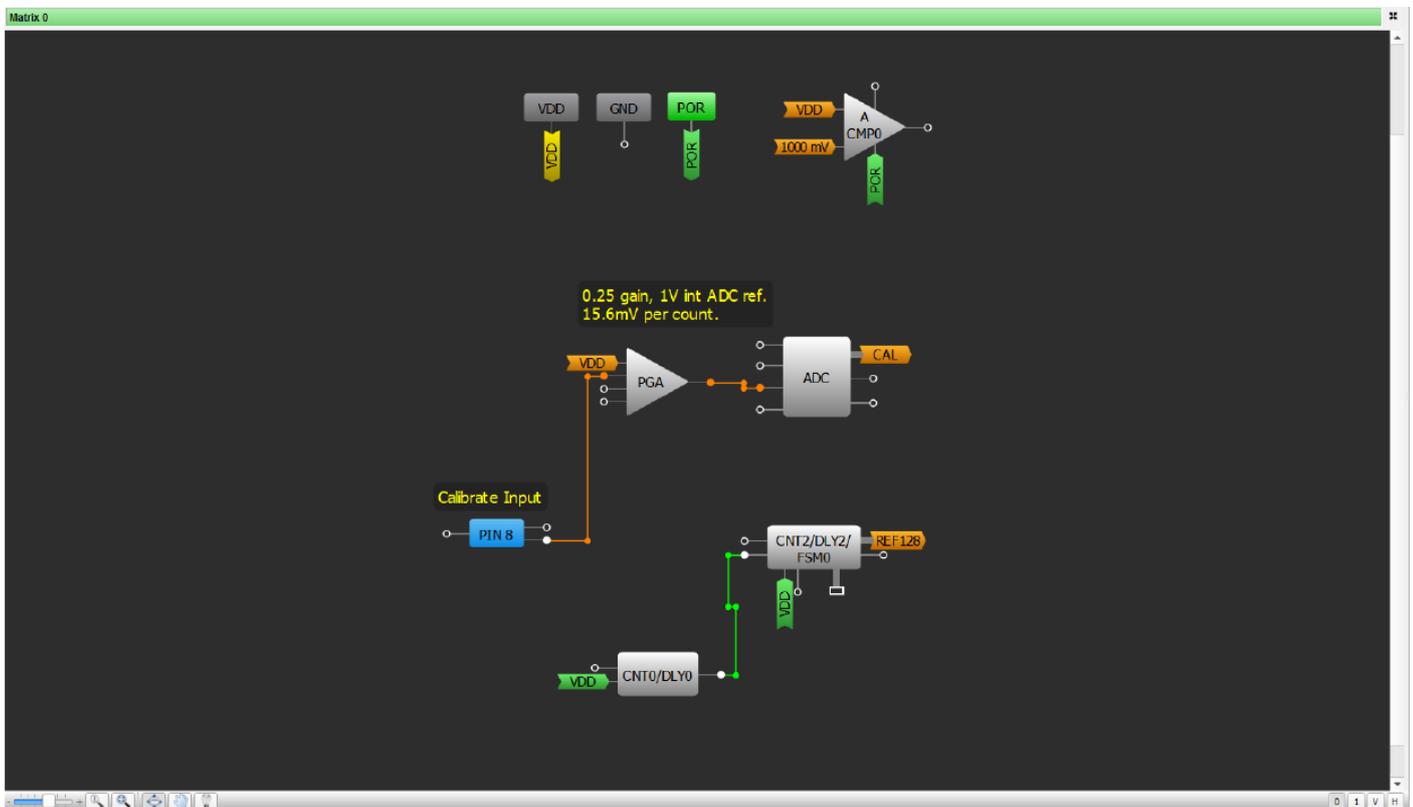


**Figure 4. GreenPAK Design - Matrix 0**

(There is a small subtlety here – note that after field calibration the STOP value of 128 no longer be at the exact center of the count range which is now less than 255; however, this does not cause serious problems because the FSM1 CAL value is expected to be relatively small.)

## DCMP0/1 bounds

Now comes the relatively simple part: deciding what the reference values for DCMP0/1 should be. From the calculations at (1) we see that a 0.1% error in mains frequency amounts to an error of 2.5 in the STOP value. For this application note we have chosen selectable sensitivity levels of 0.4% and 2%. A 0.4% error equals 10 RC cycles and 2% error equals 50 RC cycles. Correspondingly, the lower and upper limits for the DCMPs may be set to 128 +/- 10 or 128 +/- 50 depending on the sensitivity level desired. The sensitivity level is selectable using a LOW / HIGH input on Pin 20 which feed the MTRX SEL inputs of the two DCMPs which select from Register 0-3 into which the corresponding bounds are programmed.

## Implementation Notes and Results

For the most part, the design can be tested with emulation.

The emulation signal generator has a resolution of about 1% so it is possible to test the basic correctness of the design with a sensitivity not greater than 1%. It is difficult to test a breadboarded unit with mains input because of the stray hum pickup at the ACMP inputs that cause spurious readings. The author has tested this design under emulation where the calibration input to Pin 8 was via emulation, and the waveform input at Pin 12 was from a Tektronix SG502 square wave generator set to 50Hz. Time periods were verified using a Tektronix DC503A counter reading the time period at a resolution of 0.001ms.

The unit under emulation attained calibration at a Pin 8 voltage of about 440mV, corresponding to a CAL value of about 28, after which the design worked correctly at both low and high sensitivities.

## Conclusion

This Application Note has described a simple but useful design for a mains frequency monitor. The design can be used for simple alert or data collection purposes, or can be made a part of a more elaborate feedback loop or changeover/shutdown circuitry in, say, an inverter design. In a real implementation, care must be taken to lay out the circuit and provide adequate shielding so that there is no noise or hum at the ACMP input that could cause spurious triggering and affect the reliability of the unit.

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TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

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