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Introduction

This application note describes how to make a PWM LED dimming circuit incorporating feedback control in GreenPAK. This circuit is implemented in one of the smallest GreenPAK's, the SLG46120V, and thus is easily portable to other GreenPAK's.

External Circuit

As shown in Figure 1, there are 2 analog voltages; one is made by R1 and VR (0V…VDD/3) which is fed to PIN4 and PIN6. Another is made by R2 and C1, which converts the LED PWM duty (0%...100%) to analog voltage (0V…VDD), and goes to PIN3 which is configured to divide by 3 by internal gain control. The 2 analog voltages are compared to each other by internal comparator ACMP0 (see Figure 2). If PIN4 voltage is higher than PIN3, the PWM duty need to be increased; otherwise PWM duty need to be decreased. This comprises the analog feedback path that provides the desired regulation.

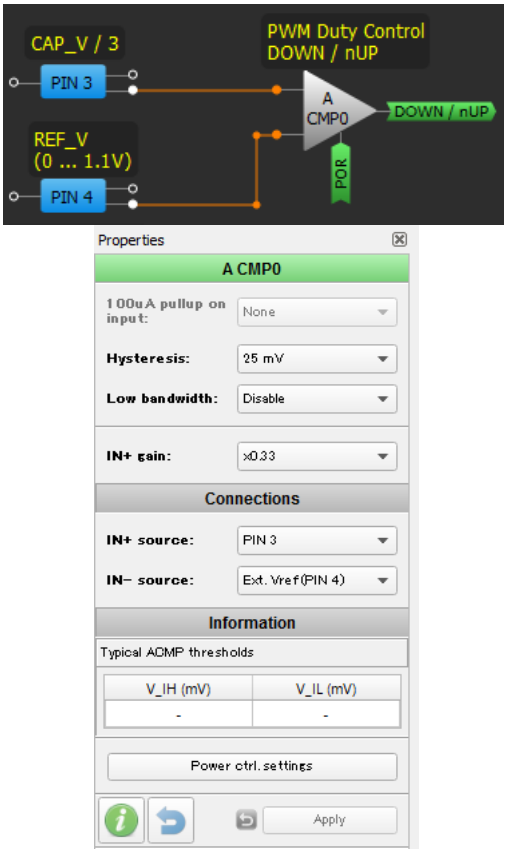


Figure 2. ACMP0 Settings

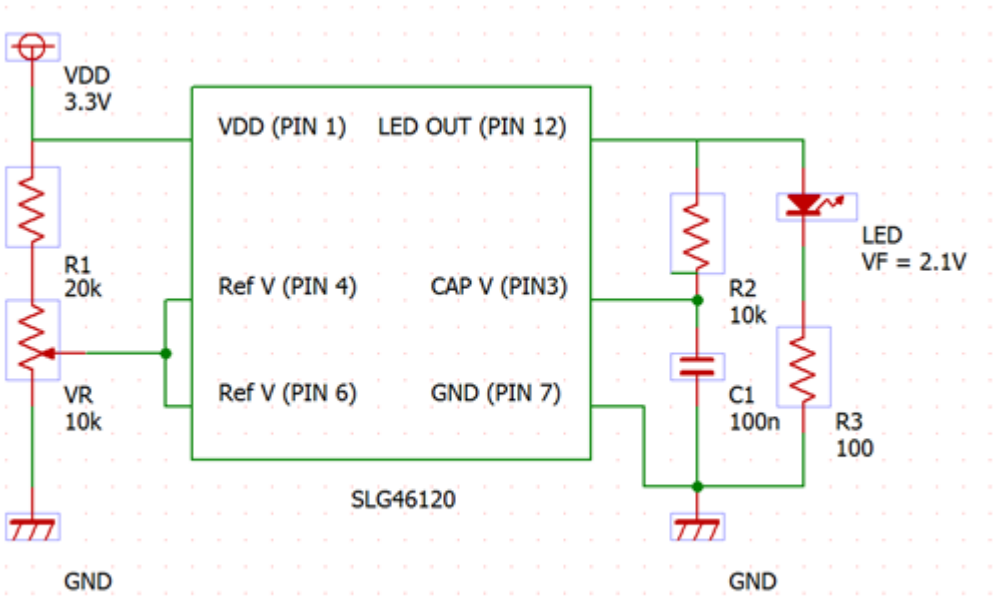


Figure 1. External Circuit

GreenPAK Design, PWM Control

Figure 3 shows the main part of the PWM circuit which is the same as the one described in AN-1117. CNT2 makes a "reset" pulse every 0.1ms and CNT3 makes a "set" pulse every 0.1ms. LUT6 latches the "set" and "reset" signals and makes the PWM waveform (see Figure 4).

Both of CNT2 and CNT3 counter data are set to 199, so the resolution of this PWM is 200 steps and its period is 0.1ms Please note that these two counter values must be equal to keep the PWM consistent.

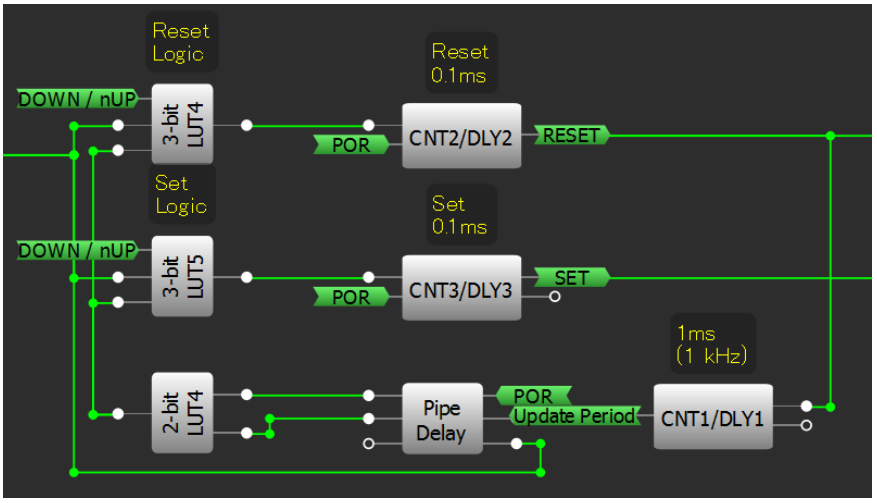
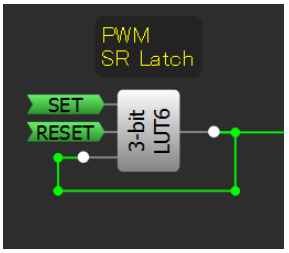
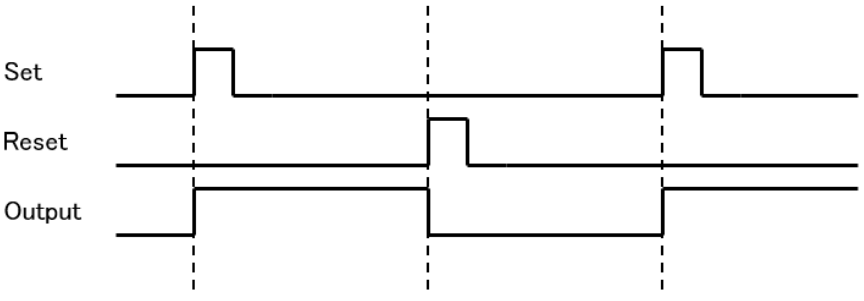


Figure 3. PWM Circuit





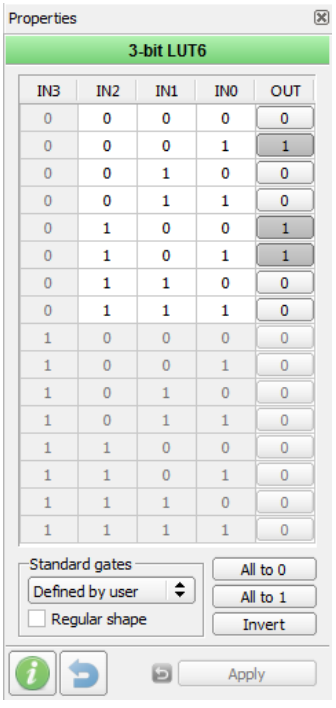


Figure 4. PWM SR Latch

Figure 5. LUT4, LUT5 Settings

At every CNT1 period (1ms), either CNT2 or CNT3 gets one extra clock by 3-bit LUT4 or LUT5, respectively (see Figure 5). Thus PWM duty is 1 step increased or decreased depending on the "DOWN/nUP" signal every 1ms. By increasing CNT1 value, we can slow down the LED brightness ramp late, and thus get more "smoothing" effect.

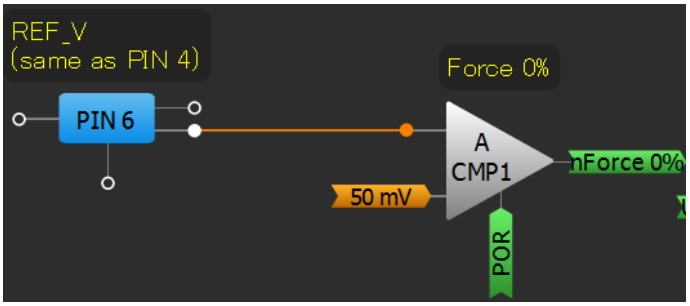


Figure 6. Underflow Control

PWM Overflow Prevention

In order to avoid overflow or underflow of PWM cycle, there are two additional circuits.

For underflow control, ACMP1 is used with 50mV internal reference (see Figure 6). When REF_V is lower than 50mV "nForce 0%" signal is activated (active low) and forces PWM duty to 0%.

Figure 7 illustrates overflow control.

When "set" and "reset" pulses are overlapped completely and "DOWN/nUP" signal is "nUP", "Force 100%" signal is activated (active high) and PWM duty is forced to 100%.

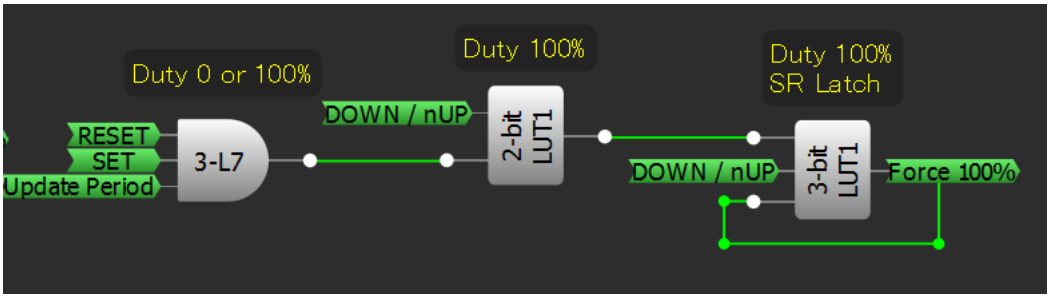


Figure 7. Overflow Control

As a result, a relashionship between "REF_V" and "PWM Duty" is as follows;

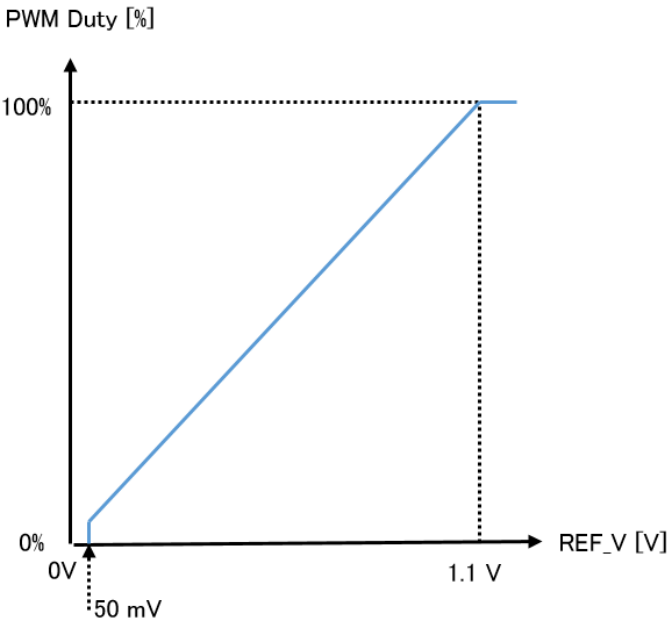


Figure 8. REF_V vs. PWM Duty

In order to make smooth transitions to/from "Force 0%/100%" and normal operation, OSC output is gated when this "Forced" situation happens so that both of CNT2 and CNT3 keep last counter value (see Figure 9)

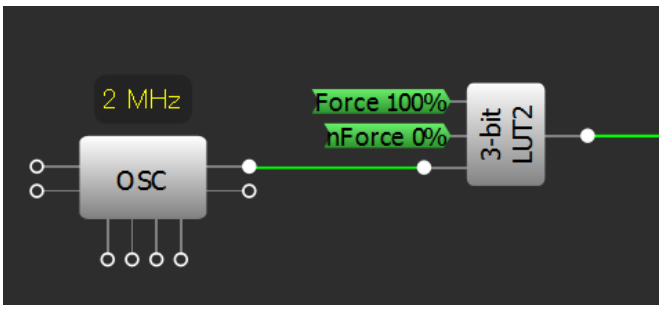


Figure 9. Clock control when PWM duty is 0 or 100%

Functionality Waveforms

Figure 10 shows actual PWM waveform with internal "set" and "reset" signals.

Channel 1 (yellow) – "RESET"

Channel 2 (light blue) – "SET"

Channel 3 (magenta) – LED OUT (PIN 12)

Channel 4 (blue) – REF_V (PIN 4 and 6)

A movie file, "LED_Dimmer.mov" is available; it shows how "REF_V" signal controls "SET", "RESET" signals and PWM output.

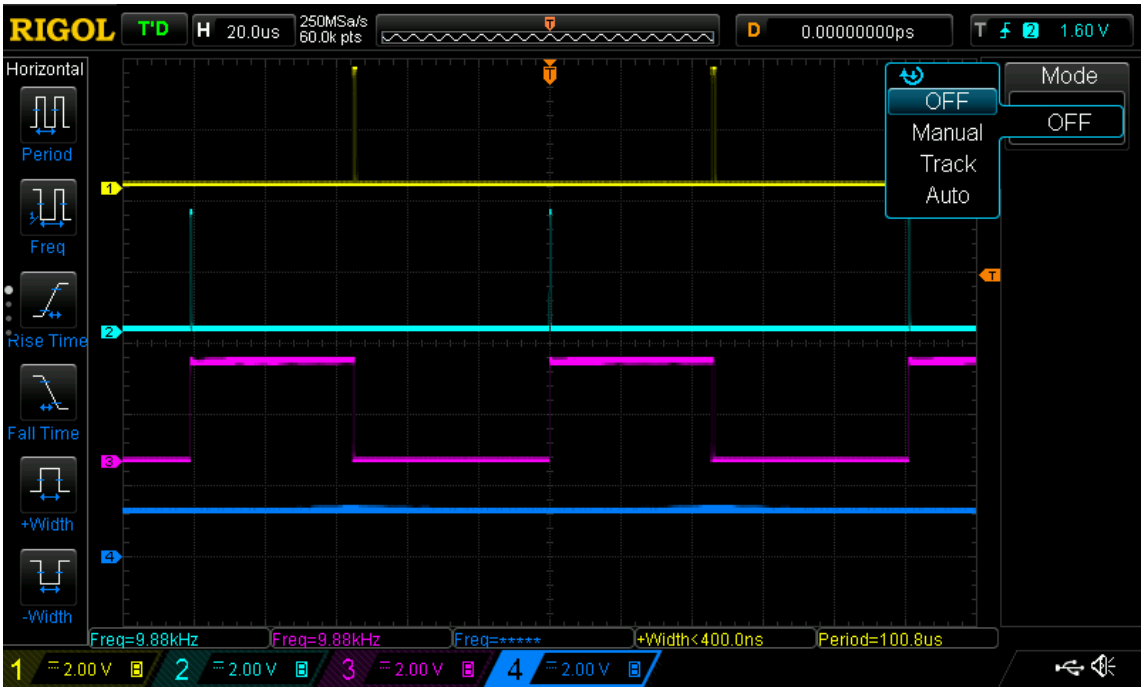


Figure 10. PWM waveform

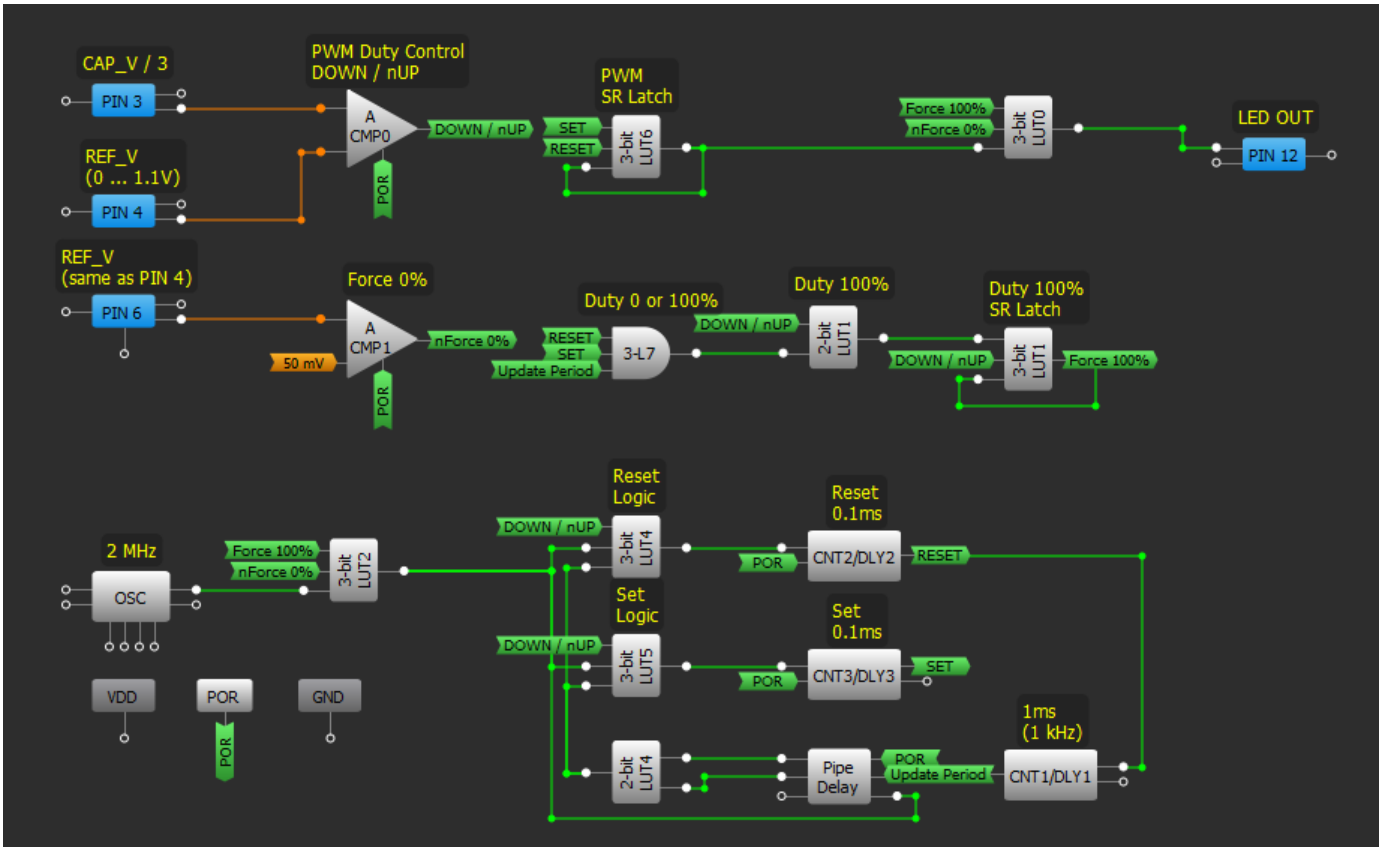


Figure 11. Entire Circuit

Conclusion

This LED dimmer circuit example shows how to create a PWM circuit with feedback control, making use of both analog and digital elements. With GreenPAK's flexible analog and digital components, such circuits can be easily implemented.

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