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Introduction

This application describes how to design a multi-power source management system using a Silego 1.6 x 1.6mm SLG46110V GreenPAK.

In battery powered devices, there is typically a re-chargeable battery, a backup battery, and a port for the power adapter. In a device where there are multiple power sources, a management IC is needed to monitor and prioritize between power lines on the main bus. This application note describes how to implement a power manager in one of Silego's smallest configurable mixed signal ICs (CMICs), the SLG46110V.

Design requirements for a power management controller are as follows:

1. Detect if the rechargeable battery is plugged in. Then read the battery level to check for under-voltage.
2. When either the rechargeable battery is under-voltage or an adapter is plugged in, determine which power source should be switched on according to a priority table.
3. Switch time delay between power sources must be fast enough to prevent the main bus from dropping outside the operating range.
4. At initial power-on, the system should operate as expected regardless of which power source is used.
5. Switch to a low current consumption mode when powered by the battery.

In the following sections, we will examine two applications with the following power sources in the system:

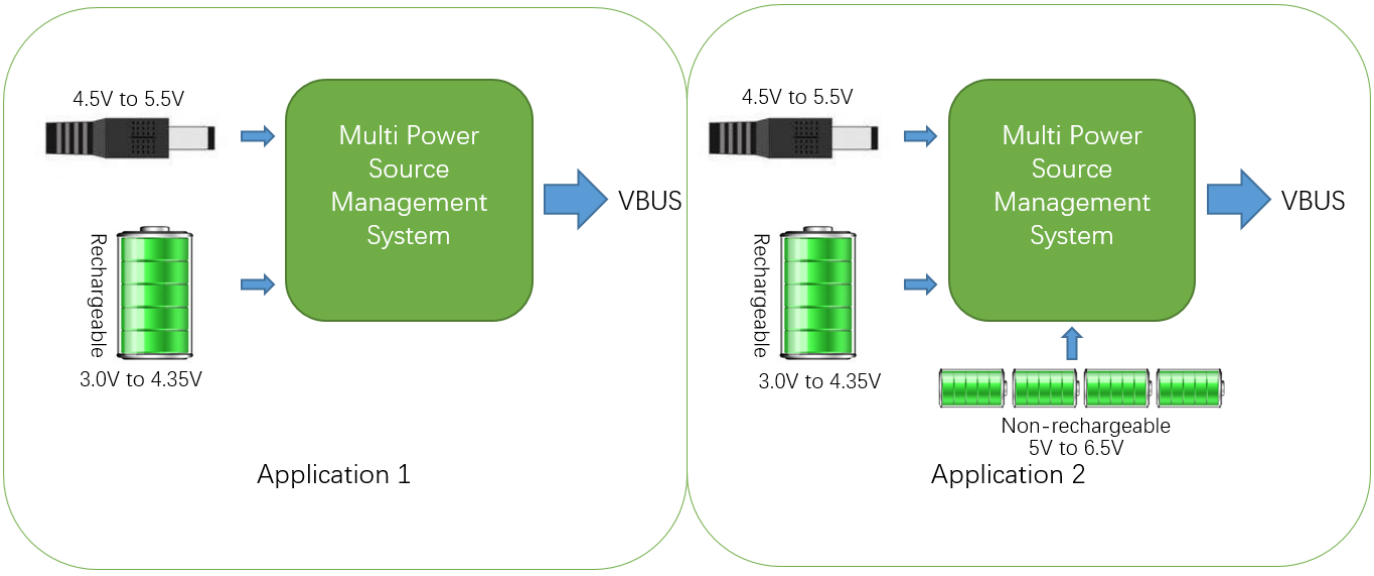

Figure 1. Two and Three power source applications, system-level view

1. Two power sources: One-cell Li-ion rechargeable Battery and one 5V adapter power source.

2. Three power sources: One-cell Li-ion rechargeable Battery, one set of backup 6.5V alkaline battery and one 5V adapter power source.

Refer to Figure 1 for the system-level view to both the first (on the left) and second (on the right) application examples.

Circuit and analysis for a two-power source management

Figure 2 is an example schematic for a two-power source, battery and adapter, application.

In this circuit, there is one Silego GPAK SLG46110V and one Silego IPS (Integrated Power Swtich) SLG59M1639V. U2 SLG46110V is the logic controller and U3 SLG59M1639V is the power path's reverse-blocking load switch.

U3 is Silego's Dual-channel reverse-blocking IPS. The switch opens or closes the power path of the battery and adapter to VBUS, while the inputs ON1 and ON2 are the gate drivers for VCC_ADA (adapter voltage) and VCC_BAT (battery voltage) respectively. The IPS supports up to 2A on each channel, and operates at input voltages 1.5V through 5.5V.

The top level circuit is shown in Fig. 2:

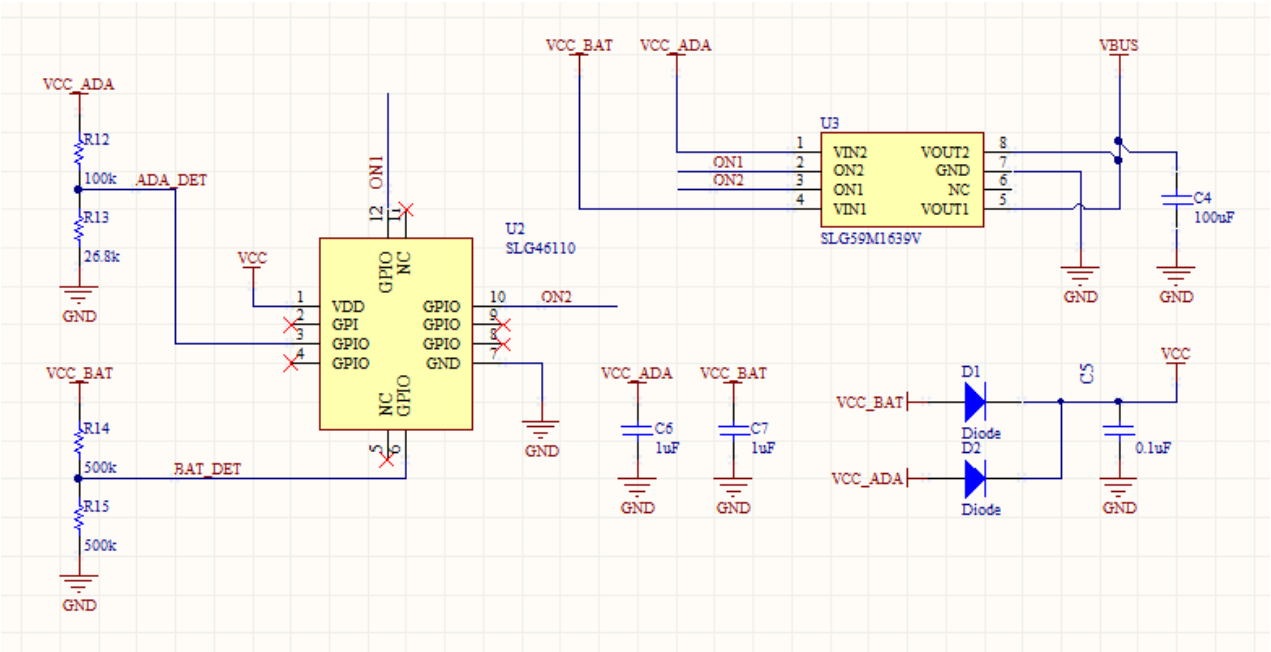

Figure 2. Circuit for One battery and one adapter

1. The divided adapter voltage, through R12 and R13, enters the GreenPAK through an analog input on (PIN#3). The analog comparator compares this signal to 4.3V, the threshold at which the battery is too low. After factoring in hysteresis, the threshold is approx. 4.13V.

2. The adapter will have the highest priority. Once the adapter is plugged in and the voltage becomes stable, the system will automatically switch to using the adapter. If the battery is low and the adapter is not plugged in, the system will be switched off until the adapter is plugged in or battery recharged.

3. The maximum turn on delay, Ton_delay, of the SLG59M1639V is 1.65ms. The engineer should choose the correct value for C4, the VBUS capacitor, such that there will be no significant voltage drop while switching between power sources. In this schematic, C4 is set to 100µF.

4. When the system is first powered on, from either the adapter or battery, U2 SLG46110V will also be powered on to switch the system to the correct power source. D1 and D2 power the GreenPAK directly through a max function where the greater voltage, either battery or adapter, is delivered. Once the GreenPAK is powered, it will take control of the U3 IPS.

5. While using the battery, the system will switch to a low power wake and sleep mode where the average current consumption is less than 10 µA. Only U2 and R14, R15 will be consuming power.

Design detail for GPAK

Figure 3 is a screen capture of the SLG46110V design. Pin 3 is an analog input to detect Adapter. Pin 6 is set to be a digital input to detect if the battery is plugged in or not. Pin 12 is the output to control switch of adapter path. Pin 10 is the output to control switch of battery path.

The key values of this design are:

1. 4.13V. The threshold where if the adapter falls below, indicates the adapter is disconnected and the system switches to battery power.

2. Switch time:

   a) From battery to adapter is between 500ms and 2.5s.

   b) From adapter to battery is almost immediate (6µs), limited by the component prop delays in the signal path: 6uS(ACMP) + 15nS (CNT2)+ 7.4nS (LUT3)+26nS (IO).

3. Wake & sleep time: 2 seconds

ACMP0 is used to detect the voltage drop of the adapter. Figure 3 shows the property settings for ACMP0. There is a 50mV hysteresis used to filter noise when the adapter voltage is close to 4.3V. So the real detect range of Pin 3 is 875mV to 925mV. With external R12 and R13 resistor divider, the real detect points are 4.139V low side and 4.376V high side.

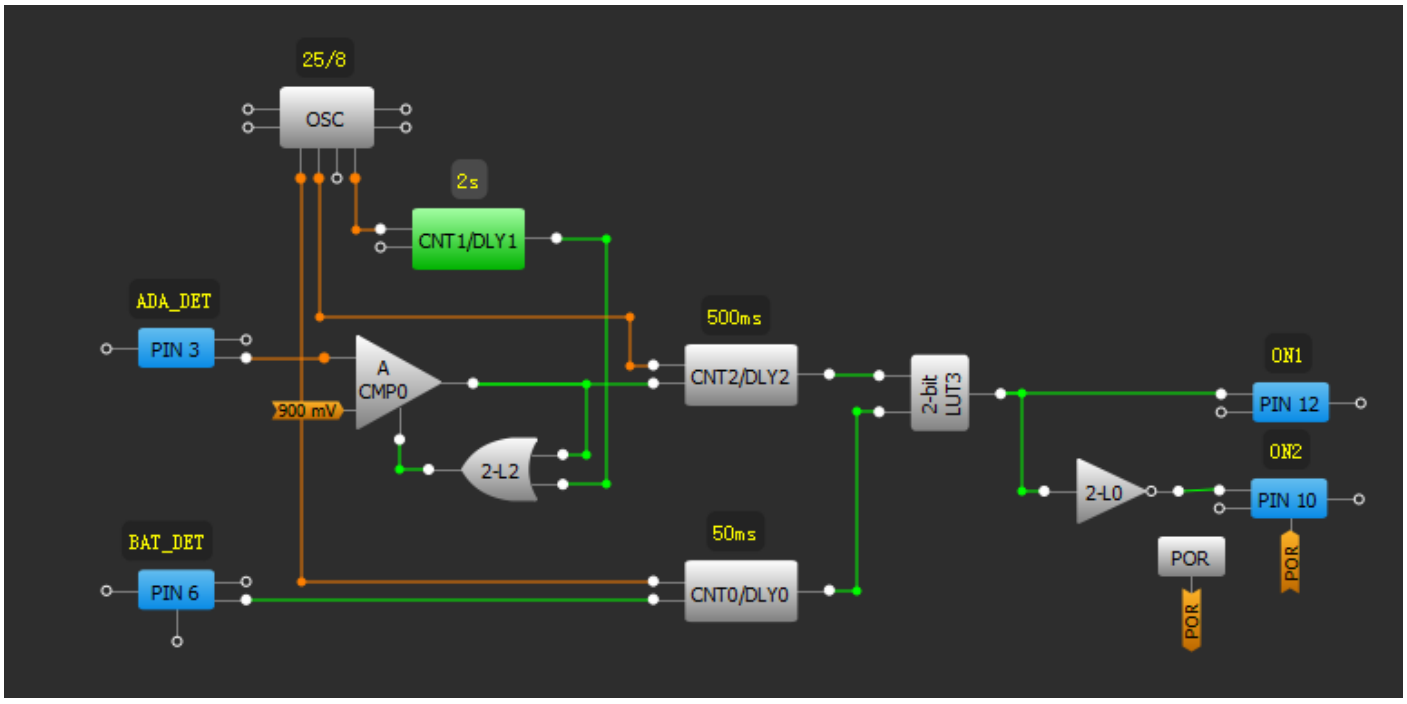

Figure 3. design detail for One battery and one adapter

DLY2 is a 500ms deglitch to filter noise while the adapter is plugged in.

2-L3 is used to set the priority of the power sources. Refer to Figure 4 and Table 1 for the priority rules.

2-bit LUT3

N2	IN1	IN0	OUT
0	0	0	1
0	0	1	0
0	1	0	1
0	1	1	1
1	0	0	0

Figure 4. LUT 3 Truth table

Adapter Plugged	Battery Attached	VBUS source
No	No	Adapter
No	Yes	Battery
Yes	No	Adapter
Yes	Yes	Adapter

Table 1. Priority table

2-L0 is used to reverse the output of ON1 to control ON2. ON1 and ON2 are the IPS switches for the adapter and battery voltages respectively.

CNT0 is used as a 50ms deglitch to filter noise while the battery is plugged in.

Low Power Consumption Mode

In this design, there is a wake and sleep timer CNT1 that controls the power on and off of ACMP0. When the system is powered by the adapter, ACMP0 will constantly check for an adapter-unplug event. When the system is powered by battery, ACMP will wake up every 2s and check for an adapter-plug-in event. Due to this wake and sleep function, the system saves power but response time increases to 0.5 - 2.5 seconds.

The battery detector input, PIN6, is set as a low voltage digital IO as shown in Figure 5.

Setting the GPIO as a digital input will not consume as much power as an analog input with ACMP. The only information required for the battery is to know whether it is absent or not, a digital IO's LVDI threshold is sufficient.

In the above example schematic, the total power consumption of this system while using the battery only is ~7µA.

Figure 6 is an example schematic for this application.

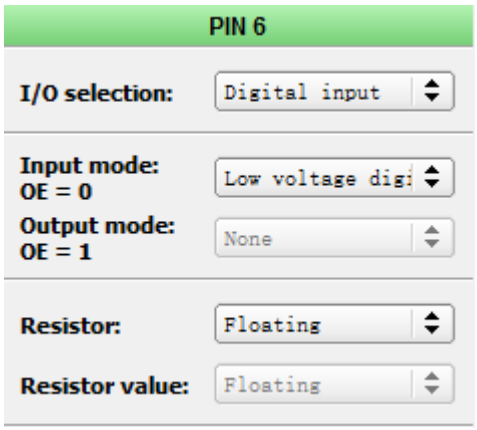

Figure 5. Pin6 settings

Circuit and analysis for a three-power source management

There are three power sources, 1 from the adapter or USB connected to VCC_ADAPTER net, 1 from the rechargeable Li-ion battery and the last one from the non-rechargeable battery array which has a higher voltage range.

Because the voltage of the non-chargeable battery is greater than 5.5V, outside the IPS operating range, discrete MOSFETs with reverse blocking will be used instead.

The resister dividers of R4 and R6, R5 and R10, R17 and R19 are used to turn on the respective MOSFET switches for the adapter, rechargeable battery and non-rechargeable battery. Upon system power on, when GPAK is still initializing, these resistor dividers make sure the VCC_VBUS will receive power when any of the three power sources is plugged in.

Design detail for GPAK

Similar to the two-power source design, the GPAK uses analog comparators to detect low power source voltages, and wake/sleeps the analog comparators when powered by battery. ACMP1 and CNT0 are used to detect the rechargeable battery voltage. If the voltage is lower than 3.0V, the system will assume the battery has been disconnected.

Three 3-bit LUTs are used to set the priority. See Table 2 for the priority logic.

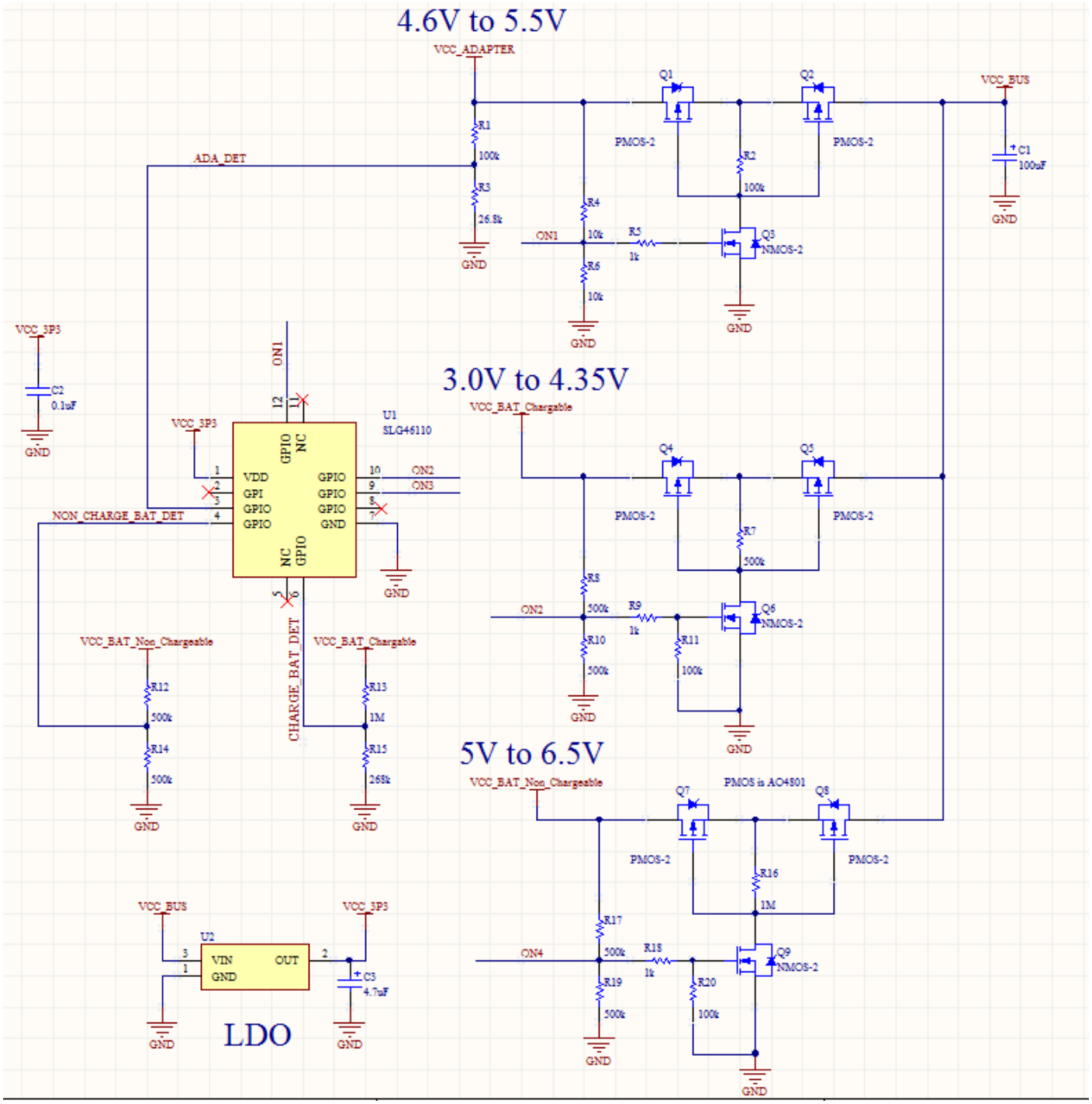

Figure 6. Circuit for 1x rechargeable battery, 1xnon rechargeable battery and one adapter

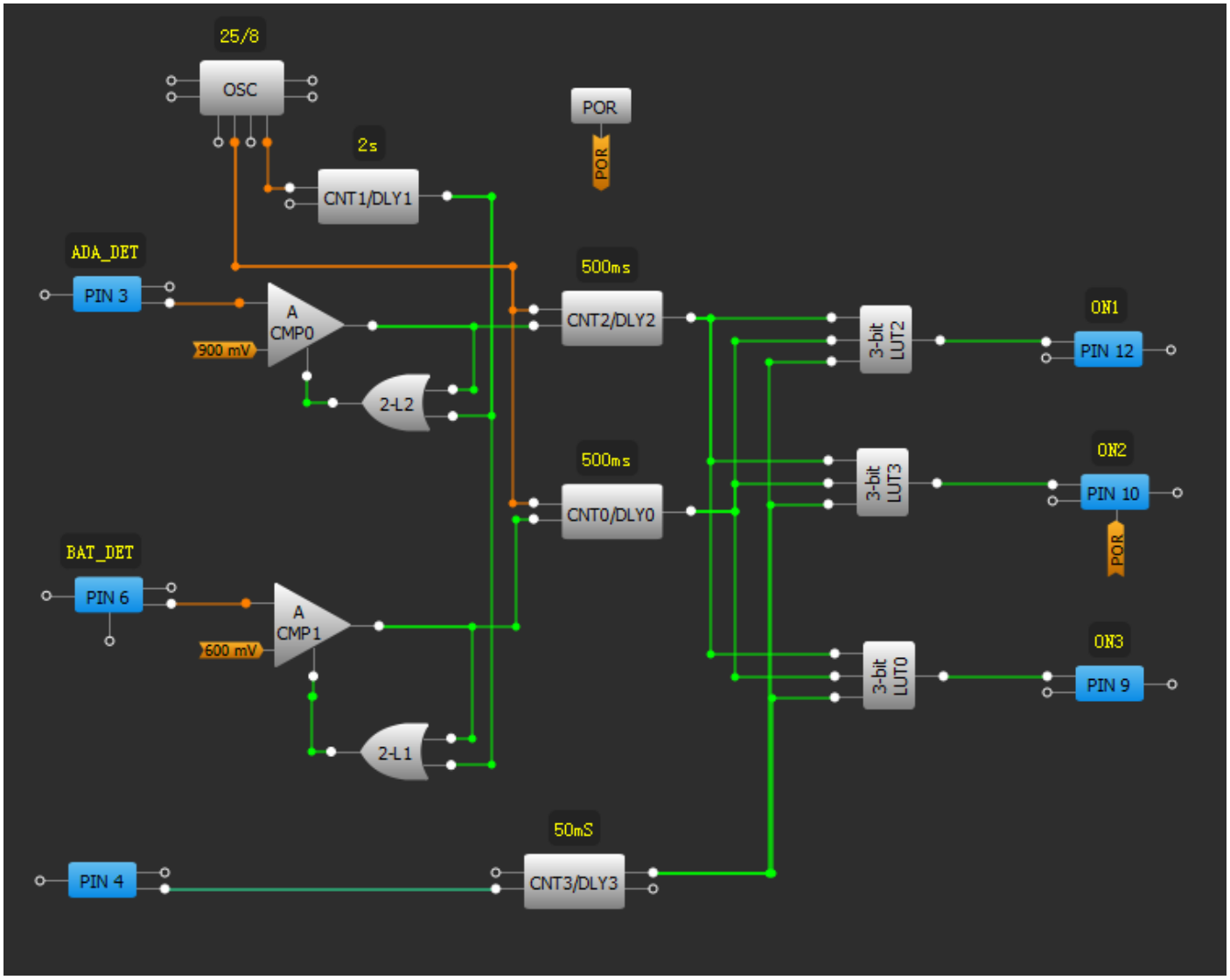

Figure 7. Design detail for 1x rechargeable battery, 1x non-rechargeable battery and one adapter

In this table, whenever the adapter is plugged in, the system will switch the power source to use the adapter. The non-rechargeable battery has the lowest priority and switches on only when both the adapter and rechargeable battery are disconnected.

Saving Power

Similar to Application 1, Application 2 uses a wake sleep timer on the analog comparator. The resulting power consumption is equally reduced; however, the total current draw is typically higher due to using more internal resources.

Adapter Plugged	Chargeable Battery	Non-chargeable Battery	VBUS source
No	No	No	Adapter
No	No	Yes	Non-chargeable Battery
No	Yes	No	Chargeable Battery
No	Yes	Yes	Chargeable Battery
Yes	No	No	Adapter
Yes	No	Yes	Adapter
Yes	Yes	No	Adapter
Yes	Yes	Yes	Adapter

Table 2 Priority table

Conclusion

A multi-power source management system (for 2 source or 3 power source) using power saving techniques has been successfully designed and demonstrated. The Silego GreenPAK is straightforward to design with, highly customizable, and occupies only a very small board area. Additionally, a GreenPAK design typically has unused circuit resources available to integrate other on-board functions as well. This further reduces board area and cost.

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A	Aaron Wang	05/27/2016	New application note

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