Introduction
When using a delay cell in a GreenPAK design, one must consider the accuracy of the delay cell. This is because the GreenPAK IC delay time depends on the clock frequency and counter data. If the counter data is a fixed value, the clock frequency can vary, especially if internal RC OSC is used. That is why the accuracy of the delay cell is determined by the OSC inaccuracy. This application note offers a way to calculate the accuracy of the delay cell in a GreenPAK3 IC in different cases such as: 25kHz or 2MHz RC OSC used, different VDD voltages or ranges, different temperatures, different combinations of the delay cells connections.

25kHz RC OSC Frequency Setting
A 25kHz RC OSC setting is the most stable and accurate setting within the GreenPAK3 family IC's. This setting is most common in GreenPAK designs, and is why understanding how to calculate the best accuracy for this setting is crucial.

In the case where separate delays are used and RC OSC is not active before the delay operation, the functional waveforms are shown in Fig. 2a. In the case where this is the first delay in a series connection of delays, the functional waveforms are shown in Fig. 2b.
Calculation of the delay timing can be made using the following formulas:

\[
T_{\min} = \frac{\text{Counter }_\text{Data} + 2}{F_{\text{osc}} \cdot \text{pre } _\text{div} \cdot \text{clk } _\text{div}} \cdot (1 + \text{var}_{\text{max}})
\]

\[
T_{\text{typ}} = \frac{\text{Counter }_\text{Data} + 2.5}{F_{\text{osc}} \cdot \text{pre } _\text{div} \cdot \text{clk } _\text{div}}
\]

\[
T_{\max} = \frac{\text{Counter }_\text{Data} + 3}{F_{\text{osc}} \cdot \text{pre } _\text{div} \cdot \text{clk } _\text{div}} \cdot (1 + \text{var}_{\text{min}})
\]

Description of variables:

\(T_{\min}\) – minimum delay time;

\(T_{\text{typ}}\)  – typical delay time;

\(T_{\max}\)  – maximum delay time;

\(\text{Counter }_\text{Data}\)  – Counter data value of the delay cell (mark A on Fig.1);

\(F_{\text{osc}}\)  – oscillator frequency, in this case it is a 25kHz (mark B on Fig.1);

\(\text{pre } _\text{div}\)  – oscillator predivider (mark C on Fig.1);

\(\text{clk } _\text{div}\)  – delay clock predivider (mark D on Fig.1);

\(\text{var}_{\text{max}}\)  – maximum value of the variable that depends on VDD voltage, temperature;

\(\text{var}_{\text{min}}\)  – minimum value of the variable that depends on VDD voltage, temperature.

<table>
<thead>
<tr>
<th>Parameter</th>
<th>SLG46110/SLG46120</th>
<th>SLG46721/SLG46722</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>RC OSC trim error</td>
<td>Min</td>
<td>Max</td>
<td>Min</td>
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<tr>
<td></td>
<td>-2.5%</td>
<td>2.5%</td>
<td>-2.5%</td>
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<tr>
<td>RC OSC variation with VDD</td>
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<td>10.9%</td>
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<td>-10.3%</td>
<td>10.9%</td>
<td>-10.3%</td>
</tr>
</tbody>
</table>

Table 1. GreenPAK3 Additional variation tolerance (25kHz Frequency Option)

\(^1\) means that chip is trimmed at VDD=1.8V and VDD operation range is 1.71V to 1.89V

\(^2\) means that chip is trimmed at VDD=3.3V and VDD operation range is 3V to 3.6V

\(^3\) means that chip is trimmed at VDD=5V and VDD operation range is 4.5V to 5.5V
\( \text{var}_{\text{max}} \) and \( \text{var}_{\text{min}} \) consist of the following components:

- RC OSC trim error;
- RC OSC variation with VDD;
- RC OSC variation with temperature;
- Settling time with 25kHz option is not considered as this time is too small compared to the minimum possible delay time.

By summing all chosen min or max error values we get \( \text{var}_{\text{min}} \) or \( \text{var}_{\text{max}} \) that can be substituted into the formulas.

If the delay cell is inside the series connection of delay cells and it is not the first one (as shown in Fig.3), the delay time calculation will be different. Such a connection is very frequently used in power rail sequencing designs. Fig.4 shows the resulting delay time waveforms where the first cell has a shorter delay time than an inside one, even though their settings are the same.

Visible in Fig.4 is the additional RC OSC clock latency for the inside delays connection. Therefore, the following formulas should be used for min, max and typical delay times calculation.

\[
T_{\text{min}} = \frac{\text{Counter}_\text{Data} + 2 + N_{\text{var}}}{F_{\text{osc}}} \cdot \frac{1}{\text{pre}_\text{div} \cdot \text{clk}_\text{div}} \cdot (1 + \text{var}_{\text{max}})
\]

\[
T_{\text{typ}} = \frac{\text{Counter}_\text{Data} + 2.5 + N_{\text{var}}}{F_{\text{osc}}} \cdot \frac{1}{\text{pre}_\text{div} \cdot \text{clk}_\text{div}}
\]

\[
T_{\text{max}} = \frac{\text{Counter}_\text{Data} + 3 + N_{\text{var}}}{F_{\text{osc}}} \cdot \frac{1}{\text{pre}_\text{div} \cdot \text{clk}_\text{div}} \cdot (1 + \text{var}_{\text{min}})
\]

where \( \text{var}_{\text{min}} \) and \( \text{var}_{\text{max}} \) parameters are calculated in the same way as for the previous formulas.

\( N_{\text{var}} \) – additional delay variable that appears in the case of inside delays connection. \( N_{\text{var}} = 0..1 \).

Fig. 3. Series Connection of Delay Cells (25kHz Frequency Option)
Delay cell calculation

in GreenPAK3

2MHz RC OSC Frequency Setting

The delay timing calculation for 2MHz option is pretty much the same as for the 25kHz frequency setting, with the only difference that in addition the settling time is taken into account in max time calculation.

\[
T_{\text{max}} = \frac{\text{Counter \_ Data} + 2}{F_{\text{osc}} \cdot \text{pre \_ div} \cdot \text{clk \_ div}} \cdot (1 + \text{var}_{\text{max}})
\]

\[
T_{\text{typ}} = \frac{\text{Counter \_ Data} + 2.5}{F_{\text{osc}} \cdot \text{pre \_ div} \cdot \text{clk \_ div}}
\]

\[
T_{\text{max}} = \frac{\text{Counter \_ Data} + 3}{F_{\text{osc}} \cdot \text{pre \_ div} \cdot \text{clk \_ div}} \cdot (1 + \text{var}_{\text{min}}) + T_{\text{settle}}
\]

where \(T_{\text{settle}}\) – maximum RC OSC settling time.

Of course, if you are calculating the delay time while the RC OSC is already operational (Forced Power On, or another delay is operating, etc.) there is no settling time to account for. So, in this case the first three formulas should be used for calculations.

The 2MHz RC OSC frequency option differs from 25kHz option not only by the clocking frequency, but with different tolerance for VDD and temperature variation.

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Delay cell calculations in GreenPAK3

The \( \text{var}_{\text{min}} \) and \( \text{var}_{\text{max}} \) parameters are calculated in the same way as for previous cases. Table 2 shows the frequency variation percentage depending on different parameters as well as maximum RC OSC settling time.

If the delay cell is inside the series connection of delay cells and it is not the first one (as shown in Fig.5), the delay time calculation will be different. Such a connection is very frequently used in power rail sequencing designs. Fig.6 shows the resulting delay time waveforms where the first cell has a shorter delay time than an inside one, even though their settings are the same.

Visible in Fig.6 is the additional RC OSC clock latency and settling time for the inside delays connection. Therefore, the following formulas should be used for \( \text{min} \), \( \text{max} \) and typical delay times calculation.

\[
T_{\text{min}} = \frac{\text{Counter _ Data} + 2 + N_{\text{var}}}{F_{\text{osc}} \cdot \text{pre _ div} \cdot \text{clk _ div}} \cdot (1 + \text{var}_{\text{max}})
\]

\[
T_{\text{hp}} = \frac{\text{Counter _ Data} + 2.5 + N_{\text{var}}}{F_{\text{osc}} \cdot \text{pre _ div} \cdot \text{clk _ div}}
\]

\[
T_{\text{max}} = \frac{\text{Counter _ Data} + 3 + N_{\text{var}}}{F_{\text{osc}} \cdot \text{pre _ div} \cdot \text{clk _ div}} \cdot (1 + \text{var}_{\text{min}}) + T_{\text{settle}}
\]

The \( \text{var}_{\text{min}} \) and \( \text{var}_{\text{max}} \) parameters are calculated in the same way as for previous formulas. As in the case of 25kHz frequency option \( N_{\text{var}} \) is a variable in range of 0 to 1.

<table>
<thead>
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<th>Parameter</th>
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<td>5.698 µs</td>
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<td>5.451 µs</td>
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Table 2. GreenPAK3 Additional Variation tolerance and Settling Time. 2MHz Frequency Option

\(^1\) means that chip is trimmed at VDD=1.8V and VDD operation range is 1.71V to 1.89V

\(^2\) means that chip is trimmed at VDD=3.3V and VDD operation range is 3V to 3.6V

\(^3\) means that chip is trimmed at VDD=5V and VDD operation range is 4.5V to 5.5V
Conclusion

Using the given formulas and tolerance variation data will aid in calculating accurate delay times of the delay cell in GreenPAK designs. Also presented was the effect on delay time of possible cell connections.
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