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*Date: May 14, 2015*

## Introduction

This application note shows how to use a single GreenPAK IC to design a circuit to determine whether the input voltage is rising, falling, or constant in time.

## Voltage slope direction determination circuit design

In this circuit, the ADC is connected to the SPI block. DCMP takes data from ADC and SPI. Signals from DCMP go to LUTs, DFF, P DLY, and DLYs, which are used to avoid glitches and form output signals.

Block configuration is presented in figures 2-10 below.

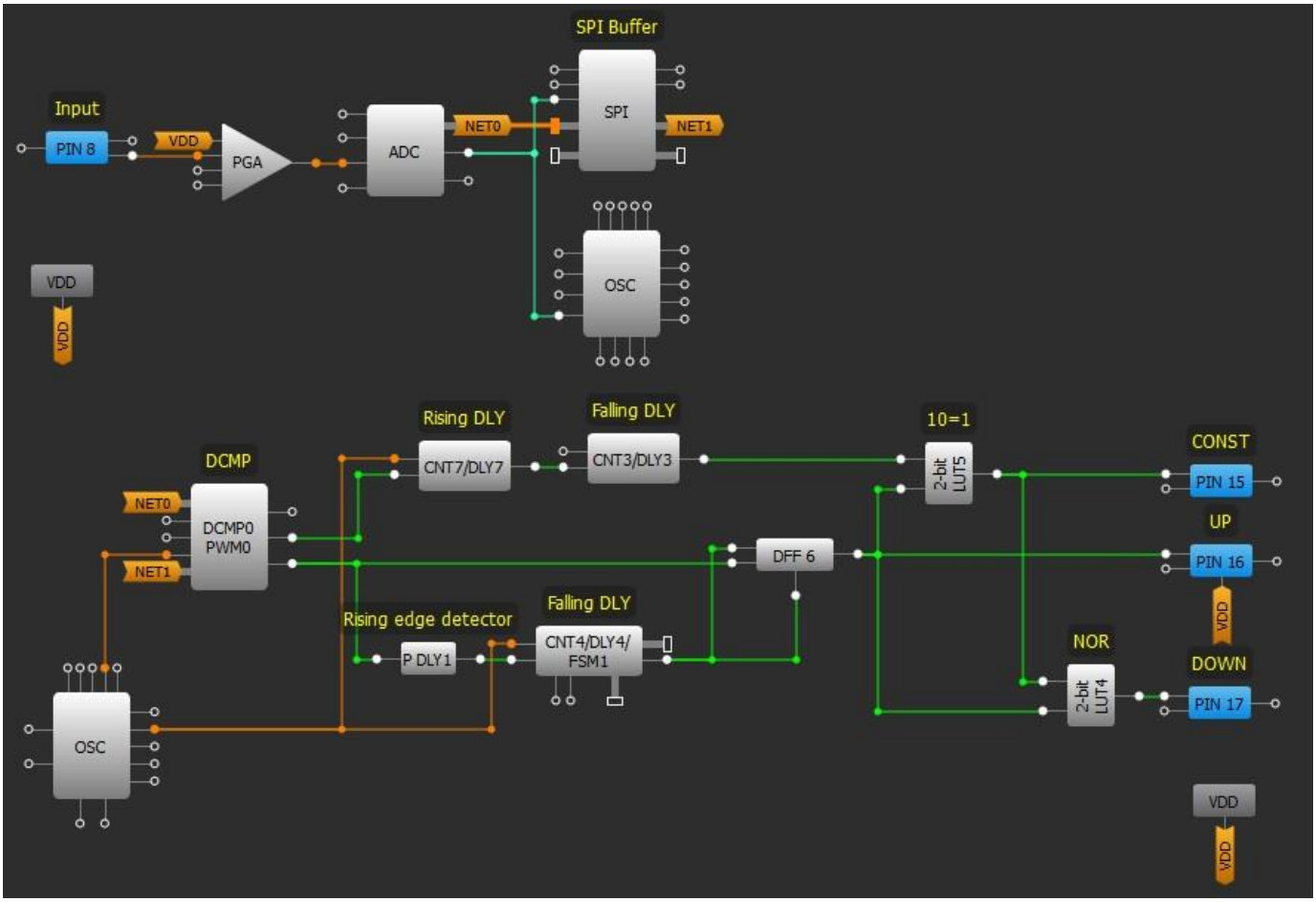


**Figure 1. Voltage slope direction definer circuit schematic**

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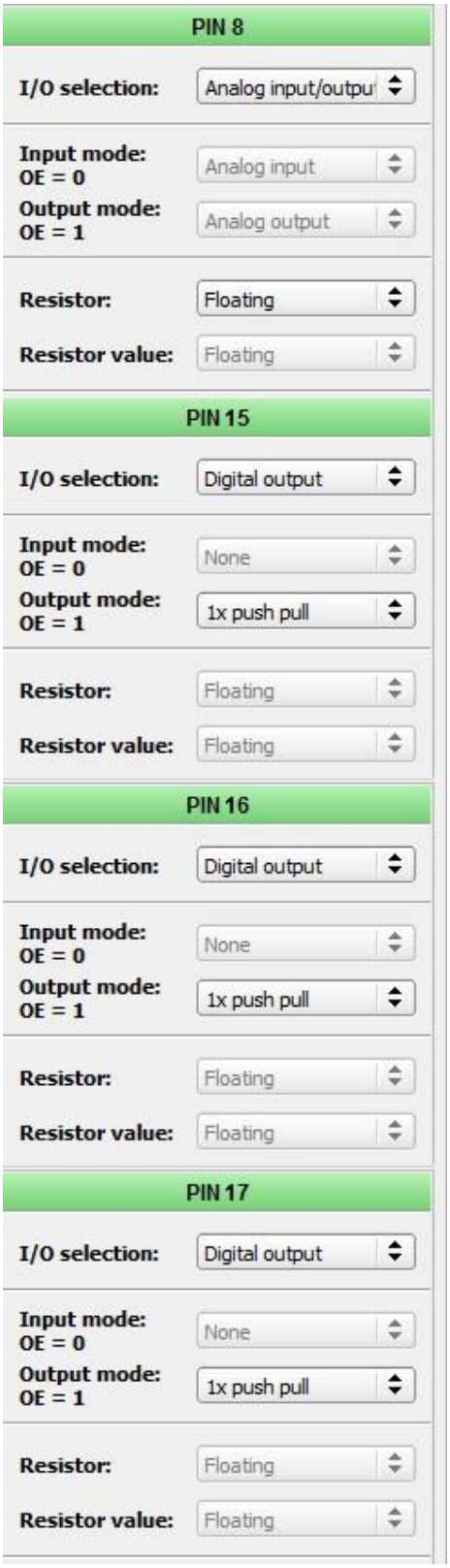


Figure 2. Pins properties

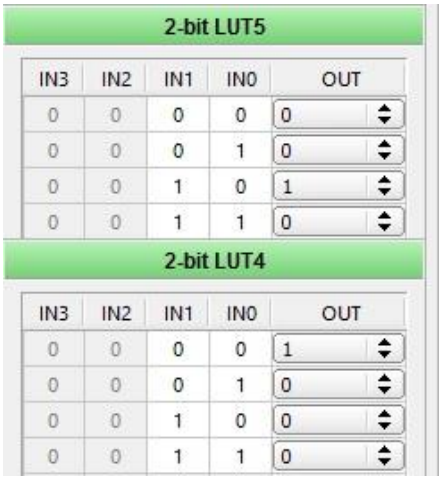


Figure 3. LUTs properties

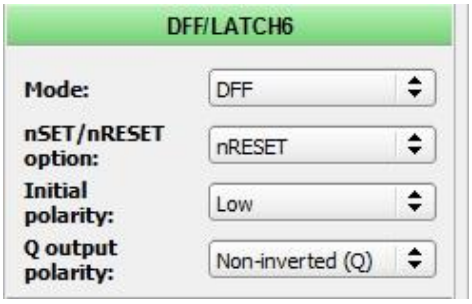


Figure 4. DFF properties

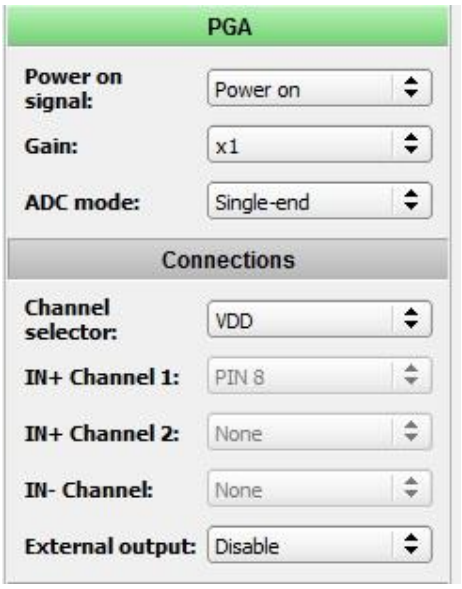


Figure 5. PGA properties

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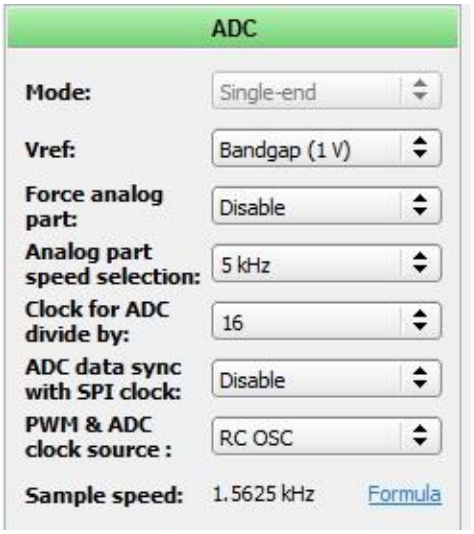


Figure 6. ADC properties

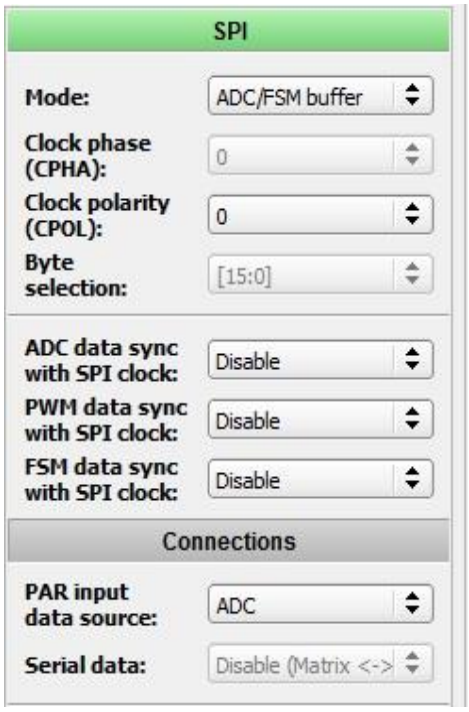


Figure 7. SPI properties

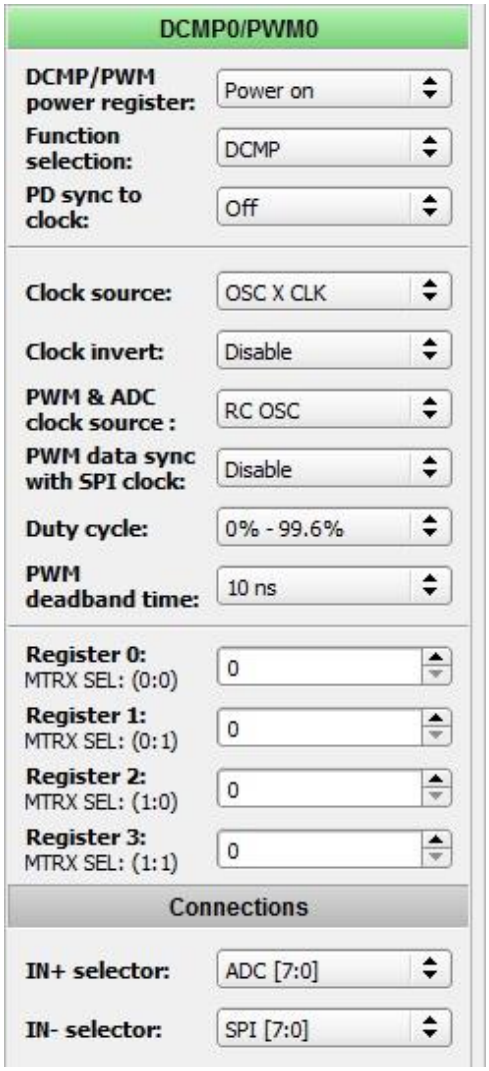


Figure 8. DCMP properties

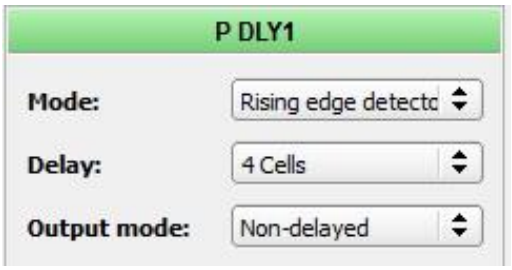


Figure 9. P DLY properties

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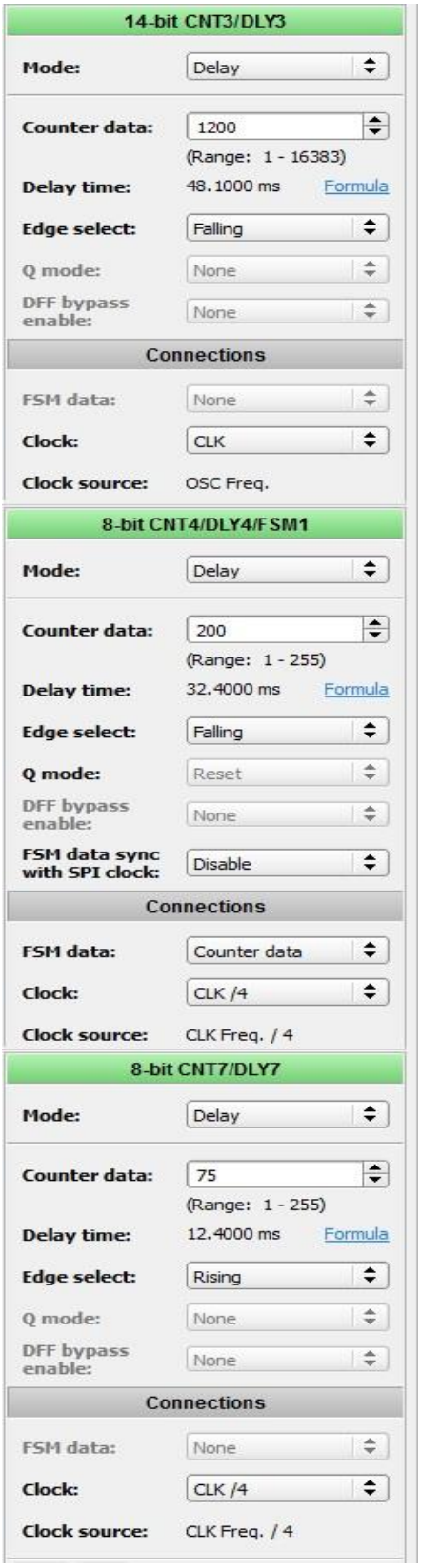


**Figure 10. DLYs properties**

## Voltage slope direction determination circuit analysis

The Analog signal comes from Input 8 to the PGA block with 1x gain. It then goes to the ADC input. The ADC operates in single-ended mode and converts the analog signal to an 8-bit digital code. The ADC transfers the parallel signal to the SPI block, configured as ADC/FSM Buffer, where digital code can be stored and won`t change until the next CLK clock comes to SPI SCLK input. The DCMP is used to compare current and previous ADC data, which is stored in the SPI block. SPI takes the CLK from ADC INT OUT, because only one pulse is needed to reload the SPI Buffer code and the DCMP for the 8-bit code comparison. In addition, the ADC INT OUT signal is coordinated in time with the ADC parallel data (see figure 11).

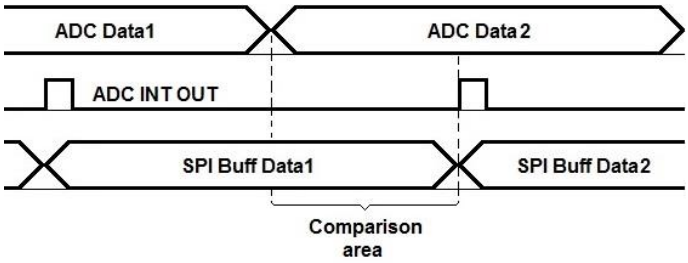


**Figure 11. ADC and SPI Buffer timing diagram**

If the voltage is rising, then the ADC Data2 8-bit code is greater than the ADC Data1 code (SPI Buffer Data1). In this situation we will receive pulses from the DCMP OUT+ (OUT+ will go high in Comparison area (see Figure 11)). Rising edge detector (P DLY), Falling edge DLY and DFF6 are used to check if pulses from DCMP are regularly repeated. If they are, UsilP output will go high.

If voltage is constant we will receive a high level signal from the DCMP EQ output. Rising edge DLY7 and Falling edge DLY3 are used to eliminate short pulses on this output. UP output priority is higher than CONSTANT output thanks to 2-bit LUT5. So if UP output is high, CONSTANT output will stay low.

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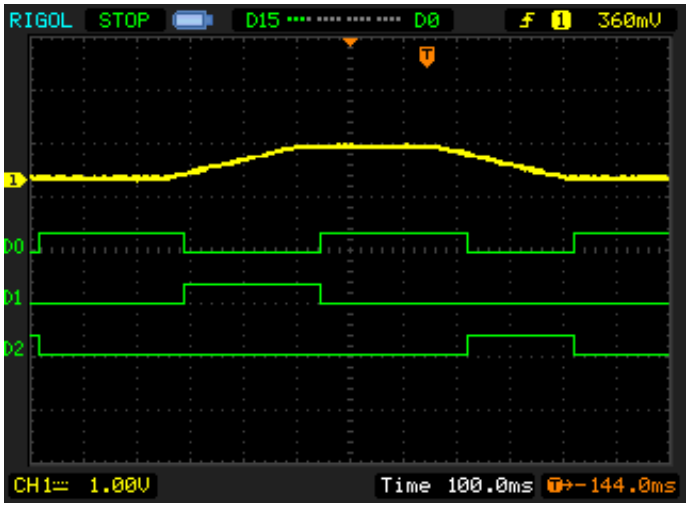
If CONSTANT output is low and UP output is low, DOWN output goes high.




**(CH1 – Input voltage; D0 – CONST; D1 – UP; D2 – DOWN)**

**Figure 12. Voltage slope direction definer functional diagram (First case)**

## Conclusion

A simple device that can detect whether an input voltage is rising, falling, or constant can be easily implemented using ADC, SPI, DCMP, and some additional blocks, which helps to form the output signals. All this functionality is contained in a single SLG46620 IC.

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