

Introduction

This application note provides a working design example of a PWM using ADC to control the output duty cycle. While this design uses only a fraction of the SLG46620 GreenPAK available resources, this example can speed successful completion of more complex designs.

ADC PWM

Detail ADC operation within the SLG46620 is as follows:

After ADC power down signal goes LOW, the ADC becomes active and receives clock signals from the Oscillator block. It takes 6 falling edges for the ADC to make a conversion. After that, the ADC outputs 8 bits of serial data (bits change on the falling edge of the clock). Then, parallel data will appear on the 13th clock (rising edge) and will be stored until the next conversion cycle.

On the 16th clock the ADC will output an interrupt signal of 1 clock cycle width. After that a new conversion cycle starts and will continue until the ADC power down signal goes HIGH.

This whole conversion process is summarized by the timing diagram shown in figure 3.

Detail of creating the PWM signal is as follows:

The PWM generator is similar to a digital comparator except that the data on one of the inputs is cycling and changes linearly. So, to create a PWM signal, we need a PWM ramp source. This is a counter that counts from 255 down to 0 or vice versa. Another source of data for the DCMP/PWM block should be parallel data that is stable for at least for 1 PWM signal period (PWM ramp counter period). It could be data from SPI, ADC, FSM blocks, or from an internal register. PWM generation is summarized by the timing diagram shown in figure 4.

As can be seen from Figure 4, it takes 1 clock cycle for the DCMP to make a comparison, so the shift of one clock period appears.

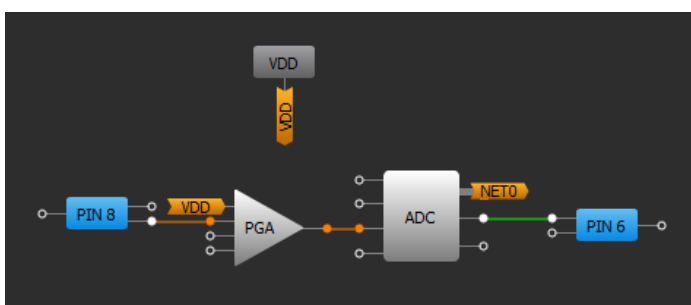


Figure 1. ADC block configuration in GreenPAK Designer software

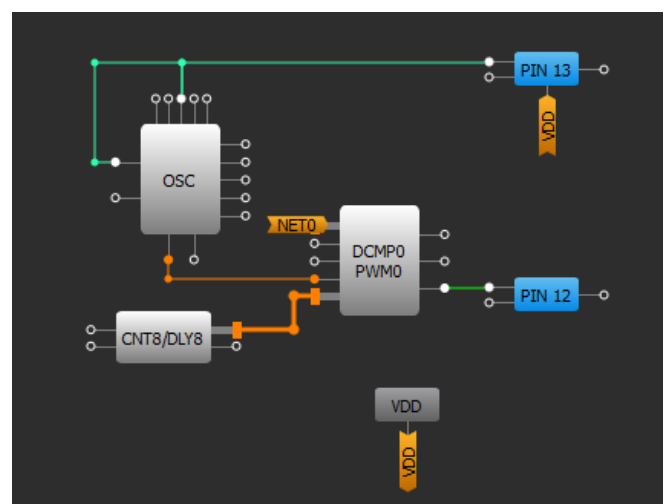


Figure 2. PWM block configuration in GreenPAK Designer software

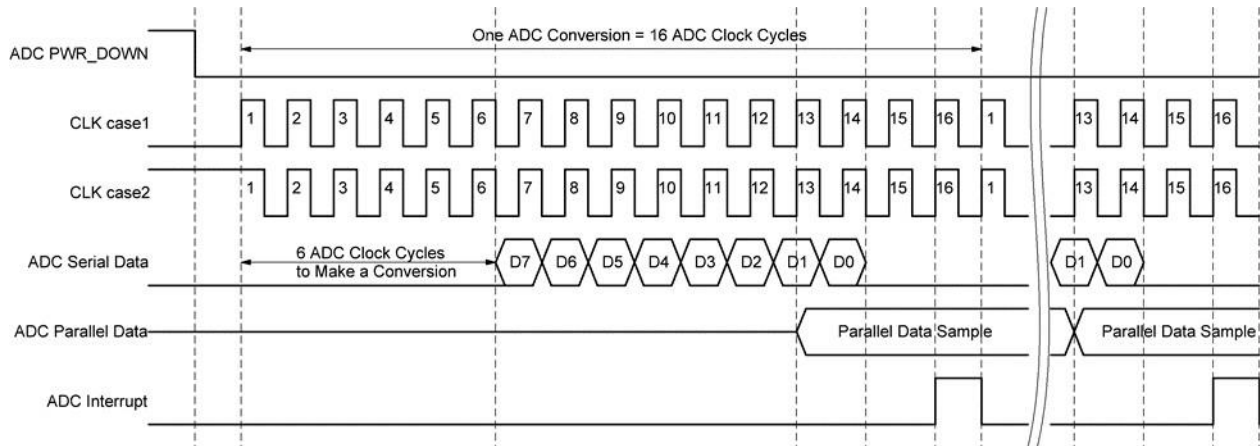


Figure 3. ADC operation timing diagram

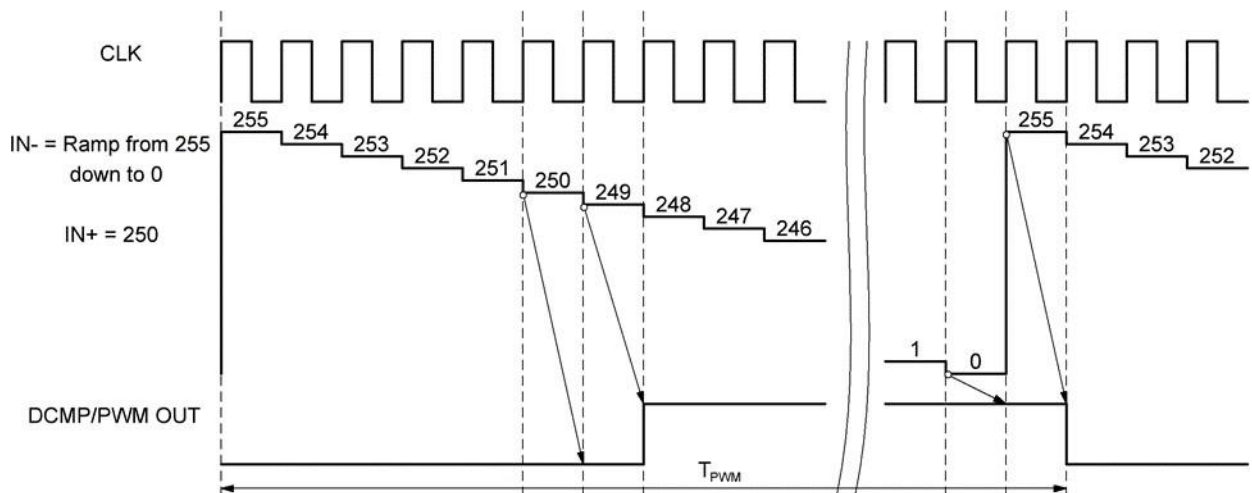


Figure 4. PWM signal formation timing diagram

Summarizing the previous description:

- There are various configurations and combinations of the ADC/PWM design due to a big variety of separate ADC and DCMP/PWM block configuration options.
- The main consideration in building correct ADC/PWM designs is assuring the correct clock synchronization.

To achieve this, proper clock sources should be chosen. Since each block could conceivably be powered on dynamically at different times, synchronization to one clock source should be used.

Let's build up a design that will accommodate all the recommendations described. In this example, the PWM generator will be set to its maximum output frequency.

This can be achieved by using the Ring OSC as a clock source for the ADC and DCMP/PWM blocks.

Figure 5 shows the configuration setting of each block used in ADC/PWM circuit. The maximum output PWM frequency is

$$\frac{F_{RING_OSC}}{(PWM_Ramp_Counter_Data + 1)}$$

(26MHz/(255+1)≈101kHz).

First, configuring the ADC is straightforward. Turn on the ADC by connecting PWRDN to a LOW signal, or to a PIN to control the ADC operation externally (such as PIN8 configured as an Analog Input). Next, turn on and configure the PWM generator. This is done by turning on the Power register, setting the Function Selection to PWM, set connections configuration of IN+ as ADC[7:0] and IN- of CNT8->Q[7:0]. As for the clock source, the same clock that is used by ADC will be used in this example (OSC X CLK configuration). The last configuration is to connect CNT8 parallel output to the IN- input of PWM generator.

The next step will be configuring CNT8: set mode to Counter/PWM Ramp, set Counter Data to 255 choose the clock source to Ring OSC (which makes PWM operate at the maximum frequency). The last step is to correctly configure the clock signal source for this application – OSC block. The OSC will produce clocks from its Ring Oscillator. So, the PWM&ADC source should be set to Ring OSC and enable Clock to matrix input of the Ring OSC.

Resolving reset and timing latency

For correct and synchronous PWM operation and to have the first data correct (first PWM period), it needs to be reset. PIN2 is used for the reset and dynamic on/off. When it is HIGH, the ADC, PWM and DLY7 will be turned off. When it is LOW, ADC, PWM and DLY7 will be in normal operation mode. With ADC & PWM dynamically on/off, they must be reset at the off state. DLY7 is used to compensate the startup time (latency) of the ADC, so in this case the Counter Data in it should be “193” (12 ADC clocks * 16 Ring OSC clocks + ~4 Ring OSC clocks for ADC to start up – 3 clocks due to delay structure).

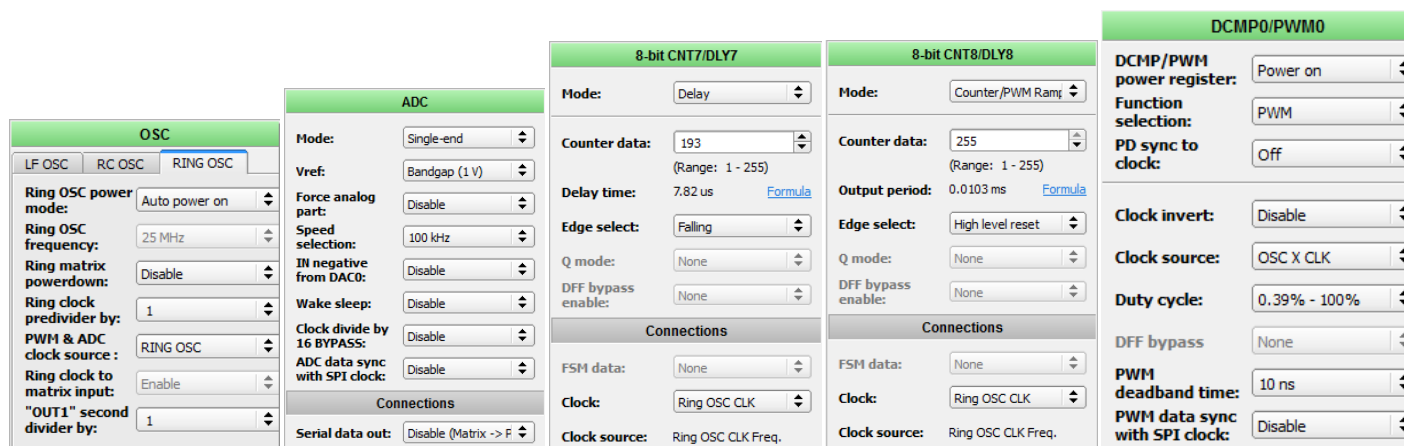


Figure 5. OSC, ADC, CNT7, CNT8, PWM0 block properties configuration in the GreenPAK Designer software

Because the CNT8 is reset to 0, but PWM ramp startups at “255”, it has one clock delay from “0” to “255”. So, there will be a glitch at the time when ADC & PWM are starting.

Two DFFs have to be added to filter out this glitch. The clock source for these DFFs will be a Ring OSC. The final design configuration is shown in Fig.6.

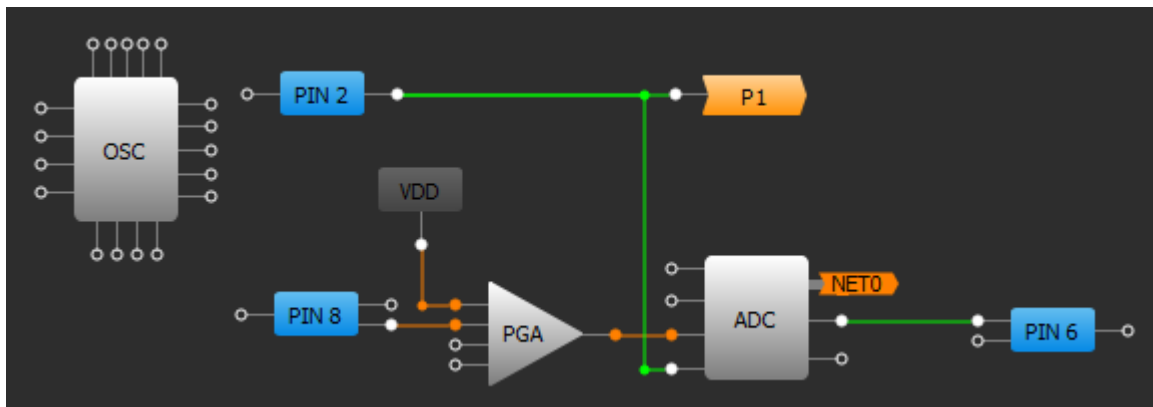


Figure 6. Schematic view of Matrix0 pane

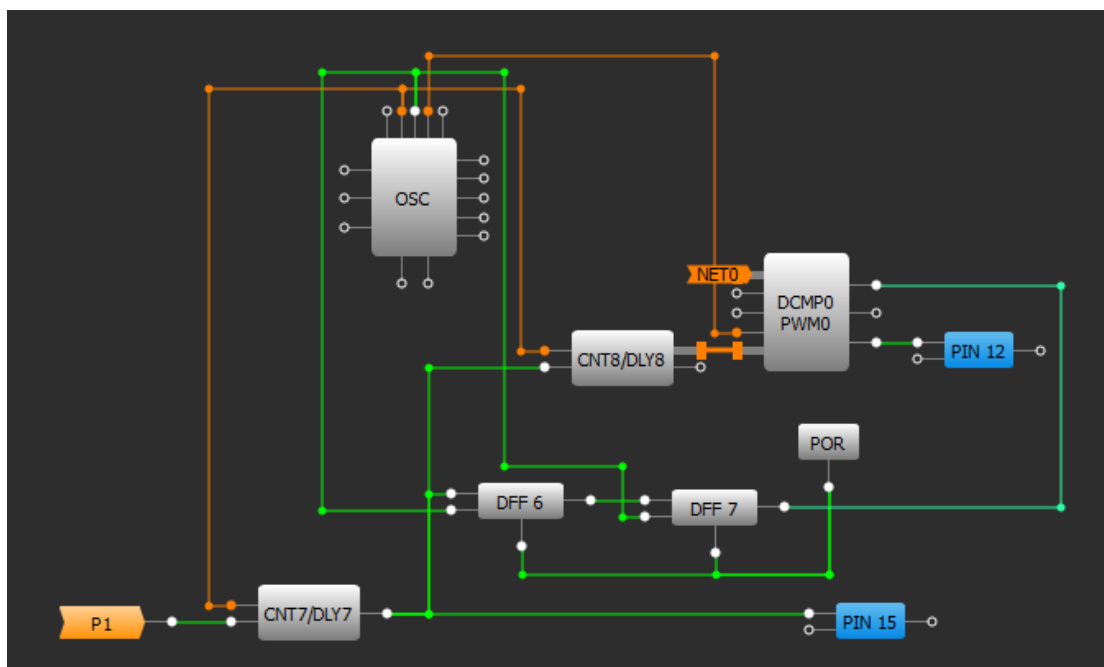


Figure 7. Matrix1 pane in the GreenPAK Designer Software



Figure 8. PWM generator turns on



Figure 9. PWM generator turns off

Channel 1 (yellow/top line) – PIN#2
 Channel 2 (light blue/2nd line) – PIN#8
 Channel 3 (magenta/3rd line) – PIN#6
 Channel 4 (blue/bottom line) – PIN#12

Conclusion

The GreenPAK4 SLG46620 IC is a versatile device with many possibilities. Being universal also puts some restrictions on device use. For correct and precise operation of the high speed PWM block in your GreenPAK4 design, one should keep in mind that some additional blocks may be required. The detail presented in this application note is intended to show a working example in order to speed the design process.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES ("RENESAS") PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES "AS IS" AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.