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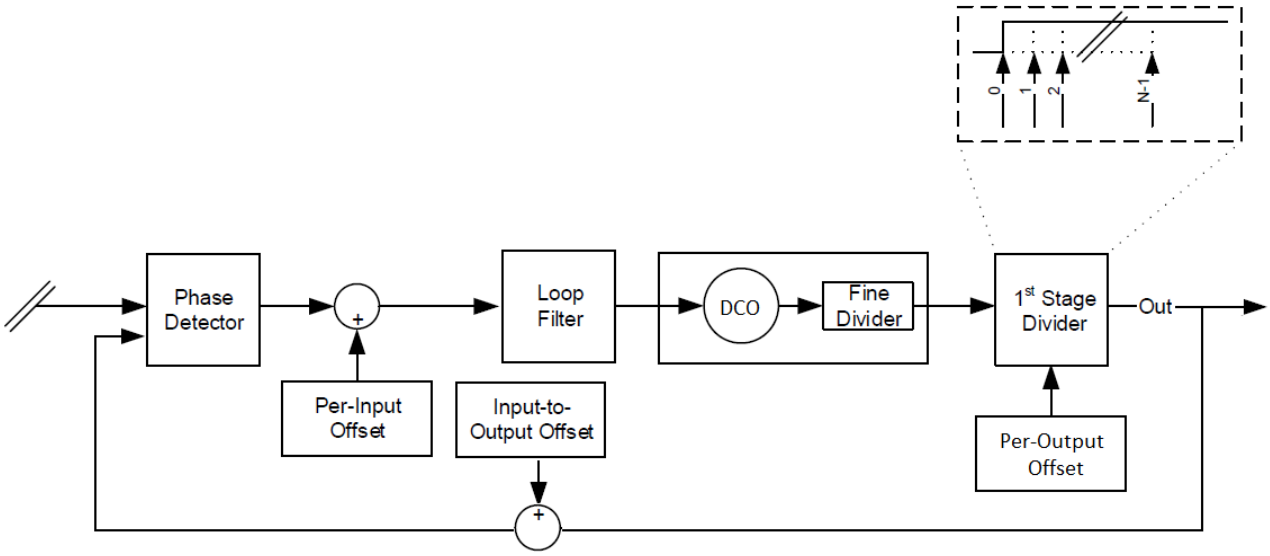
Introduction

The ClockMatrix (CM) family is a new generation of IDT's advanced timing devices. It has built in a rich and powerful set of features to meet the evolving requirements of modern timing and synchronization systems, including Sync-E and IEEE 1588 applications.

ClockMatrix implements clock phase adjustment at three different locations in the clock path, as shown in Figure 1. The phase adjustment methods include:

- Input clock phase adjustment
- Input-to-output phase adjustment
- Output clock adjustment

Figure 1. Functional Blocks where a Phase Adjustment Can be Made



In IEEE 1588/PTP applications, 1PPS is used as a basic time reference. In order to align the edge of the local 1PPS and other higher frequency clocks to the network Grandmaster (GM), a "snap" is used to achieve the alignment quickly, instead of adjusting a possible ±500ms phase skew by small increments. Therefore, on top of the three phase adjustment methods, there is a fourth method of phase adjustment in ClockMatrix: 1PPS snap.

The remainder of this document describes how each phase adjustment method works. Table 1 lists the range and the step size of each phase adjustment method.

Table 1. Range and Resolution for Input/Input-to-Output/Output Phase Adjustments

Phase Adjustment at	Range	Resolution
Input	±1.6834ms	50ps
Input-to-Output	±1717.9ms	0.391ps
Output	1UI of output clock	1ns (FoD = 1000MHz)
1PPS Snap	±500ms	50ps

Method 1: Input Phase Delay Adjustment

Input phase adjustment is intended to support clean switchovers. In a system that accepts multiple inputs, phase skew may exist among these input clocks due to different trace lengths or other reasons. When the DPLL is switching from one input clock to another, there will be output phase upsets due to the phase skew of different input clocks. By adjusting these phase skews using input phase delays, the output phase hit is minimized.

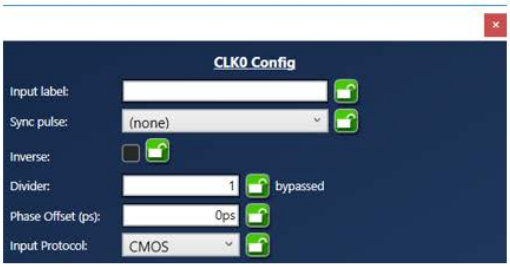
A phase adjustment can be made on each of the eight differential inputs (or configured as 16 LVCMOS) independently. The register used to configure the input phase adjustment is INx_PHASE, where x = 0…15. The register holds a signed 16-bit value, which means it can be negative or positive. For offset addresses of these registers, search by the register name under the BITS SET tab in Timing Commander GUI.

In Timing Commander, the input phase offset value is configured in the configuration window for the input clock (click at the triangle following each input frequency entry box) (see Figure 2 for the CLK0 configuration window). Hovering the mouse at the “Phase Offset” field will display the address of this input’s phase offset register.

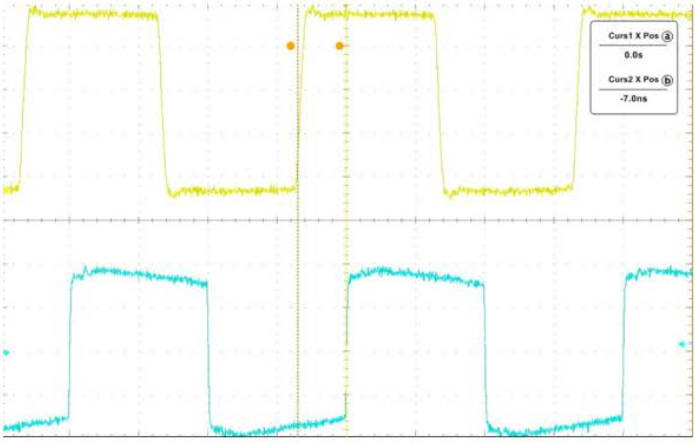
As shown in Figure 2 and the following figures, a negative phase adjustment will move the targeted clock edge to the left on a scope screen, while a positive phase adjustment to the right.

Figure 2. Output Phase Adjustment by Configuring Input Phase Delay

Phase skew between input and output clocks without any adjustment

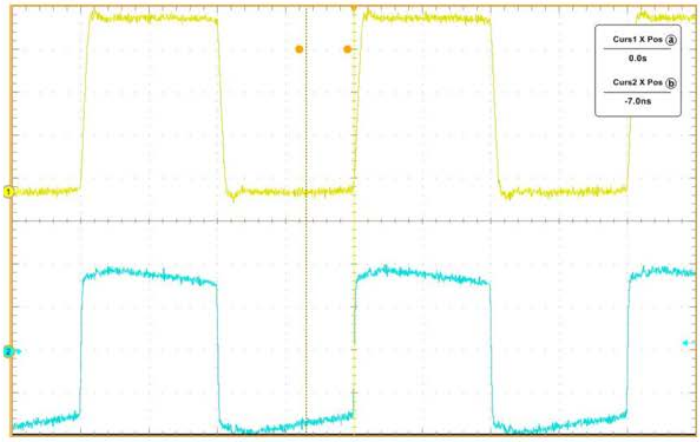


Input clock (yellow trace) leading output clock (blue trace) by 7ns



Phase aligned by adjusting input clock phase delay (IN0_PHASE)

By setting IN0_PHASE = -7ns, input clock (yellow trace) and output clock (blue trace) are aligned



The input phase adjustment register is a signed 16-bit register. It can be set with a positive value (the result is the clock edge will move to the right on the scope) or a negative value (the result is that the clock edge will move to the left on the scope).

Inx_PHASE register contains a signed 16-bit phase offset value indicating the number of ITDC_UIs to adjust the input by. One ITDC_UI = (Period of Input TDC frequency)/32. By default, Input TDC frequency is 625MHz. Using this default frequency, the resolution of input clock phase adjustment is (1/625MHz)/32 = 1.6ns/32 = 50ps. The range of this phase adjustment can be calculated by ±2^15 * 50ps = ±1.6834ms (see Table 1).

The maximum input TDC frequency can be up to 1GHz for differential input clocks.

Method 2: Input-to-Output Phase delay Adjustment

Input-to-output phase adjustment can be implemented on a per DPLL channel basis. It provides flexible phase adjustments both in wide ranges and in fine resolutions. The limit is that it is per-channel shared. Two outputs driven from the same channel will share the same adjustment value.

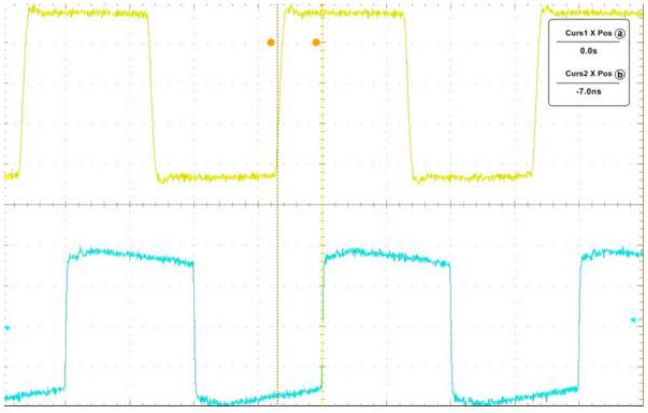
Input-to-Output phase offset is implemented by a phase offset on the feedback path from the FoD applied to the phase detector (PD). The phase offset is represented by two registers:

- DPLLx_PHASE_OFFSET_CFG (x = 0…7) – This is a signed 36-bit value to define the phase adjustment in either direction: MSB of 1 defines a negative phase delay and MSB of 0 defines a positive phase delay. Since it is a signed register, both negative and positive values can be configured to this register. A negative phase adjustment will move the targeted clock edge to the left as shown in a scope screen, while a positive value to the right.
- DPLLx_FINE_PHASE_ADVANCE (x = 0…7) – This is an unsigned 13-bit register to define the fine phase adjustment resolution as input TDC period/4096. For a TDC input TDC clock of 500MHz, this resolution will be 1/500MHz/4096 = 0.4883ps. Please note that this register will take effect only when the DPLL feedback divider is an integer. This register can only hold a positive value.

Figure 3. Phase Adjustment by Using Only the Register DPLLx_PHASE_OFFSET

No input-to-output phase adjustment is configured,
Input clock leads output clock by 7ns

No phase adjustment is configured. Input clock (yellow trace) is leading the output clock (blue trace) by 7ns



DPLL0_PHASE_OFFSET = -128, DPLL0_FINE_PHASE_ADVANCE = 0

By configuring only DPLL0_Phase_Offset, the output clock (blue trace) is not quite aligned with the input clock (yellow trace)

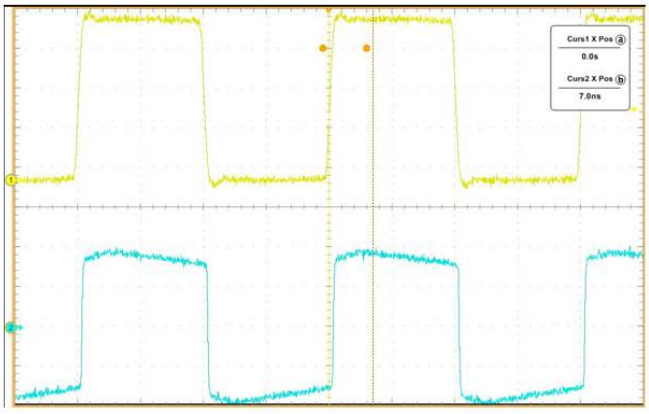
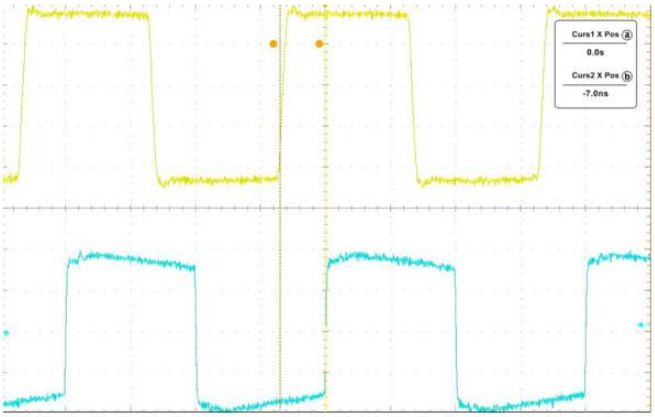


Figure 4. Phase Adjustment by Using both DPLL0_PHASE_OFFSET_CFG and DPLL0_FINE_PHASE_ADV Registers

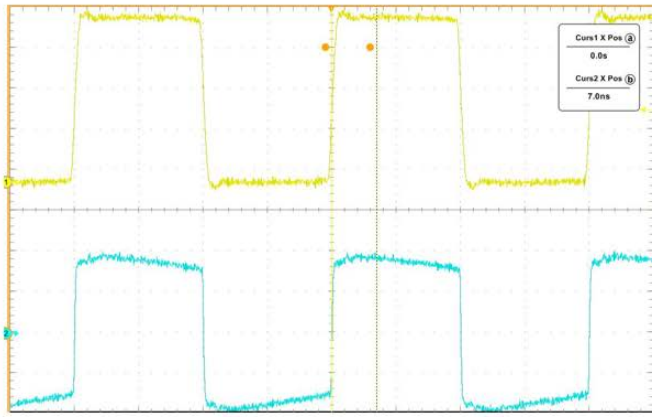
No input-to-output phase adjustment is configured,
Input clock leads output clock by 7ns

No phase adjustment is configured. Input clock (yellow trace) is leading the output clock (blue trace) by 7ns



By configuring both "coarse" and "fine" phase adjustment registers, input and output clocks are perfectly aligned

By configuring both DPLL0_Phase_Offset = -128 and DPLL0_Fine_Phase_Advance = 2048 , the output clock (blue trace) is aligned with the input clock (yellow trace)



On the right-hand side of Figure 4, "coarse" phase adjustment register – DPLL0_PHASE_OFFSET_CFG and "fine" phase adjustment register – DPLL0_FINE_PHASE_ADV are given a value of -128 and 2048, respectively.

DPLL0_PHASE_OFFSET defines the phase adjustment equal to the number of ITDC_UI. ITDC_UI = 1/(32 * input TDC frequency). It can be configured with a negative or positive number. A negative number will move the phase to the left, while a positive number will move the phase to the right. In this example, input TDC frequency is 500MHz. Thus, each ITDC_UI = 1/(32*500MHz) = 0.0625ns. As a result, setting DPLL0_PHASE_OFFSET_CFG = -128 will cause a negative phase of -128 * 0.0625 = -8ns.

DPLL0_FINE_PHASE_ADV can be set only as a positive number. It defines a phase adjustment in units of input TDC period divided by 4096. From above, input TDC period is 2ns (Input TDC frequency = 500MHz). Thus, a value of 2048 will move the phase by 2048 * 2ns/4096 = 1ns. Both "coarse" and "fine" registers configured above will have an effect on the phase by -8ns + 1ns = -7ns, compensating the output phase lagging the input phase by the same amount (shown in the left-hand side of Figure 4). After the adjustment, the output and input are phase aligned.

Default input TDC frequency is 625MHz. According to the description above, the DPLLx_PHASE_OFFSET_CFG register can define a phase adjustment resolution of ±1/(32 * 625MHz) = ±50ps; DPLLx_FINE_PHASE_ADVANCE can define a positive phase move in a step size of 1/(4096 * 625MHz) = 0.391ps.

The maximum input TDC frequency can be up to 1GHz. The resolution as calculated above can get even finer.

Method 3: Output Phase Delay Adjustment

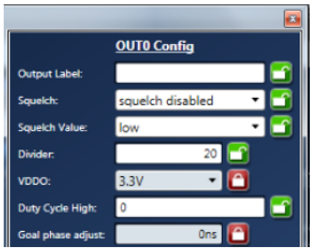
Output phase adjustment is managed at the integer divider using periods of the FoD clock, and therefore is quite coarse (1~2ns). The upside is that it can be done on a per-output basis.

A phase offset can be adjusted on any of the output clocks, differential or single-ended. The difference from the above two phase adjustment methods is that the output phase adjustment occurs at the integer output dividers after DPLL's FoD (see Figure 1). The register for the output phase offset adjustment is called OUTx_PHASE_ADJ, where x = 0…11. It is a signed 32-bit value in units of the FoD period (1nsec – 2nsec depending on FoD configuration) for the FoD driving this divider (for information on which FoD drives which output, see the device block diagram and Output Stages section of the device datasheet).

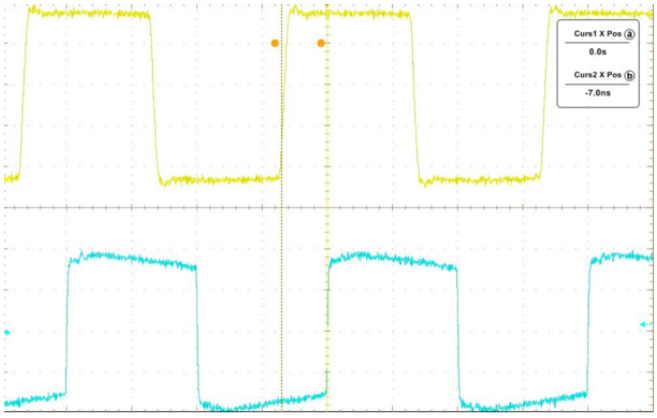
To configure a phase offset for an output, click on the output to open the OUT Configuration Window, and then enter the phase offset goal in the box. See Figure 5 – a -7ns phase offset is entered for OUT0 which is 125MHz divided from a FoD frequency of 500MHz. Please note output phase adjustment is both positive and negative. Refer to the sections above for how the clock moves with a positive and negative phase adjustment.

Figure 5. Phase Adjustment by Configuring OUT0_PHASE_ADJ

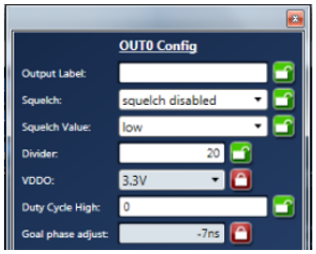
No input-to-output phase adjustment is configured, Input clock leads output clock by 7ns



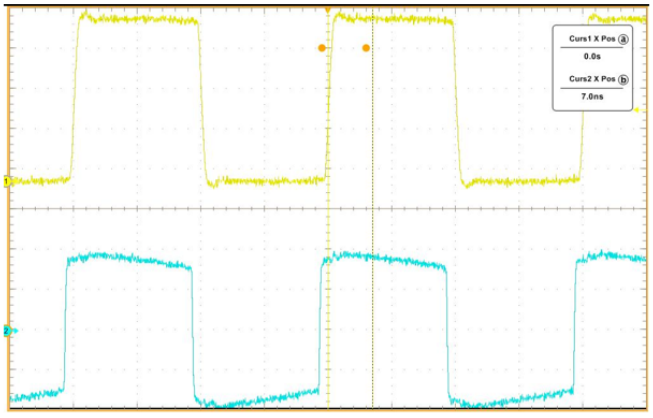
No output phase adjustment is configured. Input clock (yellow trace) is leading the output clock (blue trace) by 7ns



By configuring OUT0_PHASE_ADJ = -7ns, due to the resolution of 2ns, it's rounded up to -8ns. Thus the output clock is about 1ns leading the input clock.



By configuring OUT0_PHASE_ADJ = -7ns, the output clock (blue trace) is over adjusted by about 1ns due to the resolution of this adjustment.

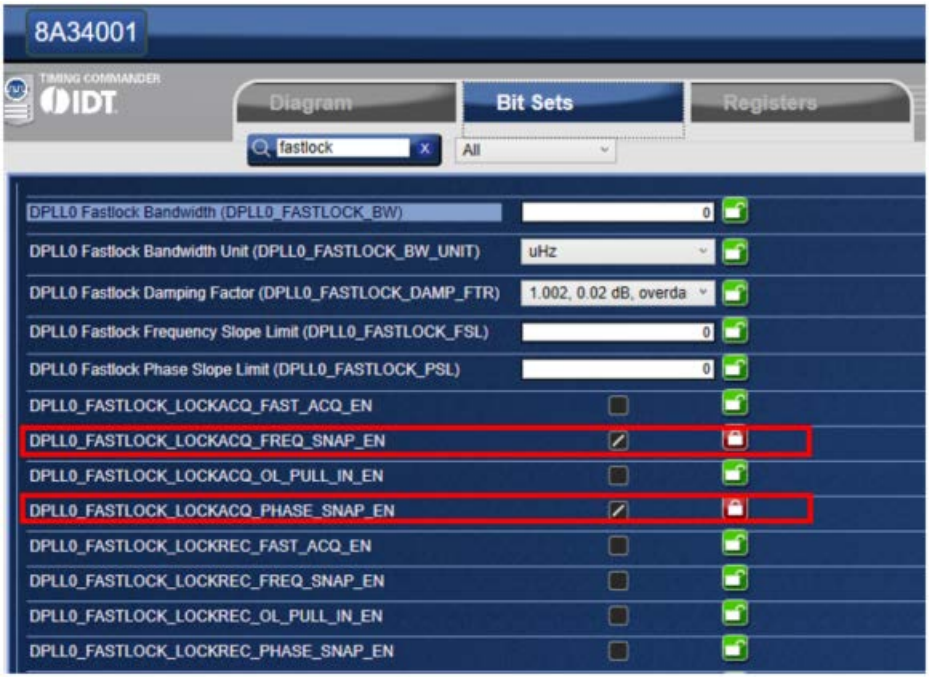


The resolution of output phase adjustment is based on the FoD frequency. In this example (Figure 5), DPLL0 FoD = 500MHz. The resolution is 2ns. By setting -7ns, the total phase adjustment is rounded up to -8ns. Therefore, the result is shown that the phase-adjusted output clock is about 1ns leading the input clock in the right-hand side portion of Figure 5.

Method 4: Frequency Snap and Phase Snap – 1PPS Snap

In an application when 1PPS or other frequencies are generated from a DPLL that is locked to a 1PPS input, a few special settings are needed to ensure that fast lock to 1PPS is achieved. Other than the bandwidth of the DPLL, when aiming to lock to 1PPS input mandatory to be set at 17mHz (≤ 1/60 of input frequency), frequency, and phase snap must be enabled. In Timing Commander, the snap can be enabled as shown in Figure 6.

Figure 6. Enabling Frequency and Phase Snap for DPLL0 to Fast Lock to 1PPS Input

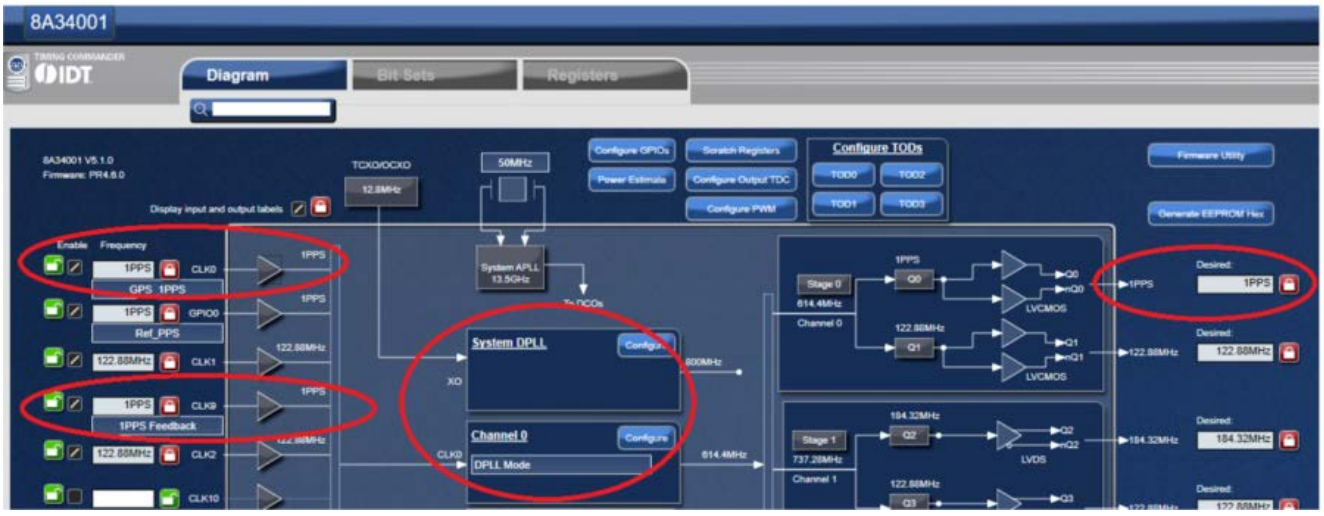


The above settings will enable “automatic” frequency/phase snap. Frequency and phase snap can also be initiated in “manual” mode. To start a manual frequency snap, write a Frequency Control Word (FCW) to DCO (i.e., in write-frequency mode); or write DCO using GPIO increment/decrement (GPIOx_DCO_INC_DEC_DPLL_INDEX) with a DCO step size (DPLLx_DCO_INC_DEC_SIZE). Manual phase snap can be triggered by writing a phase skew to Qn divider or by writing a ToD trigger source (ToDx_WRITE_REF_INDEX[3:0]. For more information, please contact IDT Support.

To adjust output phase alignment with respect to the input 1PPS when locking is achieved, the above three methods – input, input-to-output, and output phase adjustment, are applicable.

To compensate static phase offset inside the device, the external feedback can be used. In such a configuration, a 1PPS output is externally fed back into one of the inputs on top of the primary 1PPS input, as shown in the following Timing Commander configuration window.

Figure 7. Configuring 1PPS External Feedback



To enable external loopback or to select which input is used for the external loopback, further configurations are needed for DPLL1 as shown in Figure 8.

Figure 8. DPLL Configurations to Enable 1PPS External Feedback and INPUT9 is Selected

Please note that 1PPS frequency and phase snap are enabled (as shown in Figure 8) for the external feedback operations.

Summary

As shown in Figure 2 through Figure 8, the output phase adjustment can be implemented by input, input-to-output, and output phase adjustments. These methods can be used individually or in combination to achieve the desired applications goals in terms of phase alignment among outputs clocks or between an output and an input with a high degree of precision.

Frequency and phase snap are more often used to accelerate 1PPS locking, thus a phase alignment can be achieved more quickly.

References

1. *8A34001 Datasheet*, September 26, 2018
2. *8A3xxxx Family Programming Guide*, V4.7, September 12, 2018
3. *ClockMatrix GUI Step-by-Step Guide PR4.7*

Revision History

Revision Date	Description of Change
January 18, 2019	Initial release.

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