Introduction

ClockMatrix provides many tools for managing timing references. It has several different modes to align output clocks, control skew, measure clocks, select clock sources, and have independent timing paths for IEEE 1588 / Precision Time Protocol (PTP) and Synchronous Ethernet (SyncE) based clocks.

Typical large telecom system consists of Line Cards (LCs), Routing/Switching Processors (RSPs), Timing Cards (TCs), Fan Trays, back/mid-planes, and/or switching matrixes. Some of these functions can be combined in the same cards; for example, RSP can have TC functionality as well. If such system needs to participate in network timing distribution, then it is expected that they support SyncE and IEEE1588 standards. It is also expected that these system contribute very little constant Time Error (cTE) noise to the network clock.

This document addresses how to use ClockMatrix's reference monitors and independent System DPLL for applications that require nCXO (compensated XO) redundancy using ClockMatrix.

Why have nCXO Redundancy?

Most PLL architectures use a single nCXO for operation. This nCXO is not only for normal DPLL operation but used as a system clock to perform many of the other features required for today's sync applications, such as input reference monitoring and holdover.

For Telecom, the nCXO provides a stable frequency backup on the loss of network synchronization. For redundancy in chassis-based systems, the TC functionality is duplicated, thus, there would be a need for two nCXOs in the system to provide this backup. With OCXOs (Oven-Compensated XO) and their passive components, there is an increased chance of failure of the nCXO. For this reason, it is becoming desirable to use the alternate/secondary TC's nCXO as a backup to the local nCXO.

Because the local nCXO is also used for clock monitoring, with nCXO redundancy, it makes it very difficult to do the following:

- Detect if something is wrong with the local nCXO itself (i.e., single point of failure for the timing system)
- Switch, if one could detect such a failure, to a redundant nCXO with minimal impact to the rest of the system (e.g., no unnecessary transients/glitches on the other clock outputs)

With ClockMatrix's SysDPLL architecture, all of the above points can be addressed to provide nCXO redundancy within the system.

Per-Input Reference Monitors (REFMON)

The ClockMatrix Reference Monitor uses the SysDPLL as the measurement clock for the short-term (LOS), mid-term (activity) and long-term (frequency) monitors. Each of the sixteen CLKn inputs can have its own independent setting each monitor's threshold, along with independent masking of either monitor to determine if the input is qualified or disqualified. XO_DPLL is a clock input itself but there is not the same monitoring capability on this input, as discussed below.

REFMON Measurement Clock Source

The SysDPLL provides the measurement clock for the reference monitors. The SysDPLL typically locks to the XO_DPLL input, which is connected to a local nCXO – TCXO (Temperature-Compensated XO), OCXO, etc. – and provides a stable clock source for these measurements. As previously mentioned, there is no monitoring on the XO_DPLL pin, thus, the SysDPLL will track this clock as long as it is within its DCO range (±244PPM). If the clock at XO_DPLL is lost (squelched high/low or tri-stated), the SysDPLL will follow the last phase offset seen, thus, eventually rail at ~1.5%. Optionally, the SysDPLL can lock to any of the 16 input clocks, which would then allow the use of the reference monitor to qualify/disqualify the input. This is discussed more in the following sections.

nCXO Monitoring

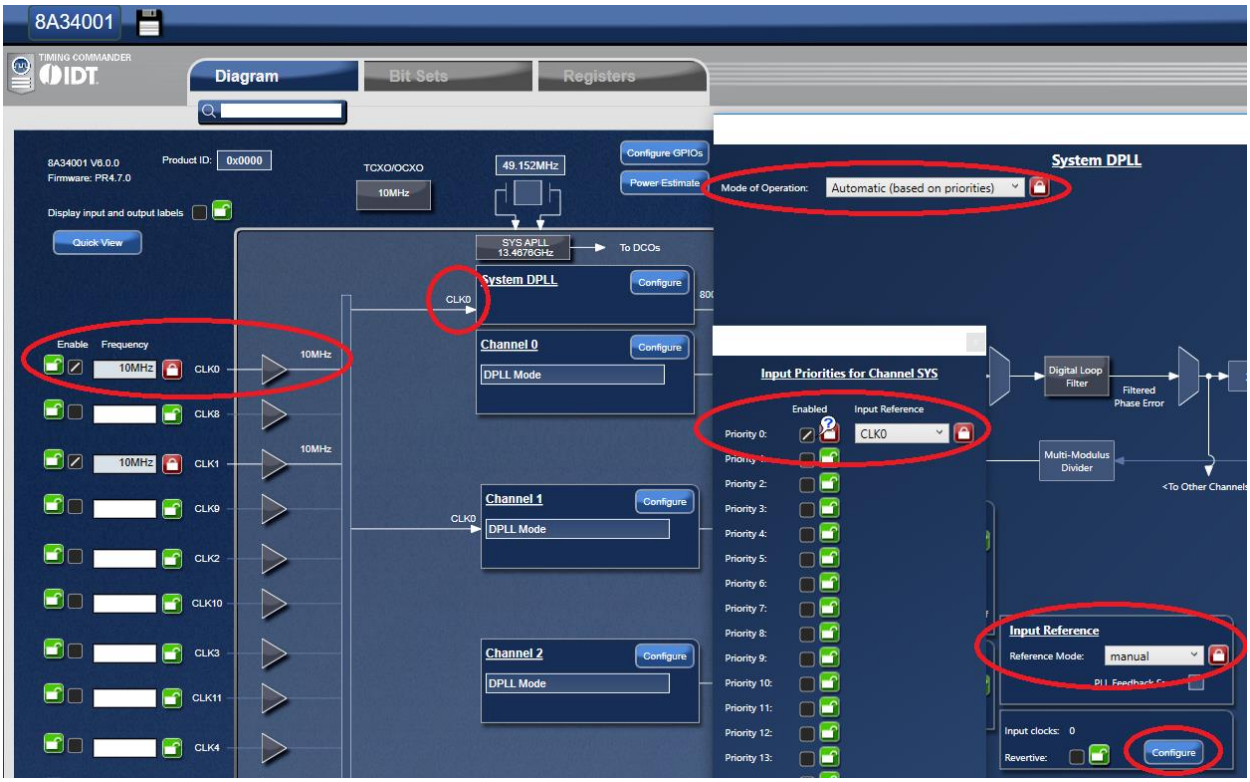
The simplest clock monitor is for LOS, but unfortunately XO_DPLL does not have LOS detection. If you want to avoid this limitation then it is recommended to put the local nCXO on a CLKn input so that it can use the available LOS monitoring. This will allow the SysDPLL to go into Holdover on LOS. See Figure 1 below. All other reference inputs should also use LOS monitors, or use an external LOS signal to trigger LOS via GPIO for the CLKn that is associated with that GPIO.

Activity monitoring is useful for identifying a toggling clock at the input; however, its precision is likely not enough to identify any failure of an nCXO (range is from 1000PPM down to 12PPM). For this reason, activity monitoring is best used to qualify recovered line clock sources (i.e., SyncE) or to detect large, quick FFO transients (i.e., > 12PPM in 1.25ms).

Frequency monitoring measures the FFO between the clock and the measurement source (SysDPLL). To acquire precision in this measurement, longer measurement windows are used (i.e., seconds). Since the maximum frequency accuracy of the nCXO is known, this can be used to determine if there is an unexpected offset detected. For example, if the nCXO is accurate to ±1.5PPM over 25 years and the backup has the same accuracy, then you know the FFO measured should always be between ±3PPM. By adding a second source, such as a SyncE clock traceable to PRC (10-11), you can use this to determine which nCXO is out of specification. Even if the second source is not traceable to PRC (Primary Reference Clock), its short-term accuracy should be sufficient (e.g., G.8262 option 1 is ±2PPM over 24hrs).

To simplify the above, the local nCXO can also be placed on a CLKn input. Although this would mean its FFO value would always be 0PPM, it may make the voting system easier as the relative offsets of all three sources would be easily calculable, even after a switch to the redundant nCXO or when adding additional monitoring sources (i.e., GNSS).

Figure 1. ClockMatrix GUI Showing Local nCXO on a CLKn Input



nCXO Error Detection

Since the SysDPLL is typically locked to the local nCXO via the XO_DPLL pin, it is difficult to detect if there is an issue with the nCXO connected to XO_DPLL. However, by comparing other sources in relation to the SysDPLL, such as a redundant nCXO or SyncE, you can determine if the nCXO is the source of the failure.

For example, let's say you have an alternative nCXO on CLK0 and a SyncE source on CLK1. Let's also assume both nCXOs have a long-term accuracy of ±4.6 PPM. Since the SysDPLL will be locked to the local nCXO on XO_DPLL, it will also have an accuracy of ±4.6 PPM. We can then use the Reference Monitors for CLK0 and CLK1. For CLK0, since the alternative nCXO has the same long-term accuracy, we would expect a value for the frequency (long-term) monitor to be < 9.2 PPM. For CLK1, since the SyncE source is traceable to PRC, we would expect a value for the frequency (long-term) monitor to be < 4.6 PPM. With these two values, a voting system can now be performed to detect if any of those monitors exceed an expected threshold. In addition, the LOS (short-term) monitor can be used to detect a loss of clock, along with the Activity (mid-term) monitor to detect any quick, large transients.

To determine if there is an issue with XO_DPLL, review both the CLK0 and CLK1 monitors. To simplify, you can bring the local nCXO to a clock input (i.e., CLK2) as displayed in Figure 2. This will allow you to complete three-way relative comparisons between the three (or more) clock sources. This will also allow you to take advantage of the LOS and Activity monitor on the local nCXO to quickly disqualify the clock to the SysDPLL.

In Table 1, the input frequency offset monitors are used to measure the Fractional Frequency Offset (FFO) for CLK0 (-4.6ppm), CLK1 (0ppm), and CLK2 (+4.6ppm) when CLK0 and then CLK2 are used as the SysDPLL source. As shown in the figure, the FFO is 0ppm for CLK0 when the SysDPLL has CLK0 as the source. The FFO is 0ppm for CLK2 when the SysDPLL has CLK2 as the source.

Figure 2. Test Setup for nCXO Error Detection

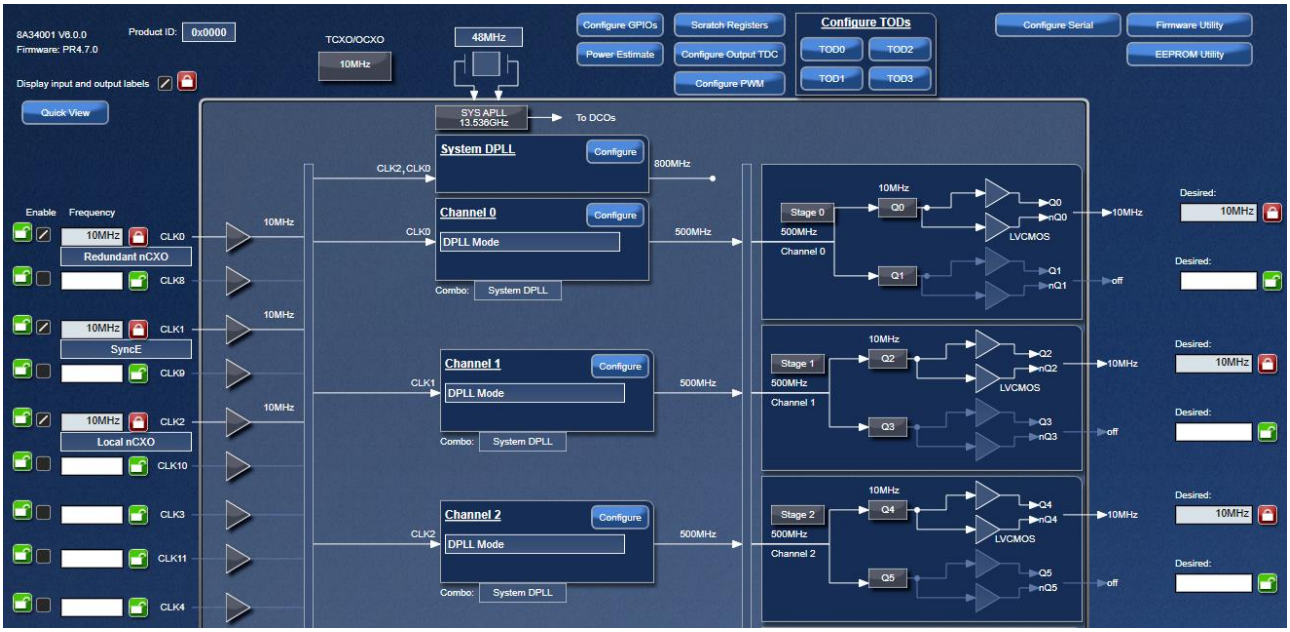


Table 1. Input Monitor Results

Input	FFO (ppb)	SYSDPLL Source		Input	FFO (ppb)	SYSDPLL Source
CLK0	0	CLK0		CLK0	-9200	CLK2
CLK1	4600			CLK1	-4600	
CLK2	9200			CLK2	0	

nCXO Error Recovery

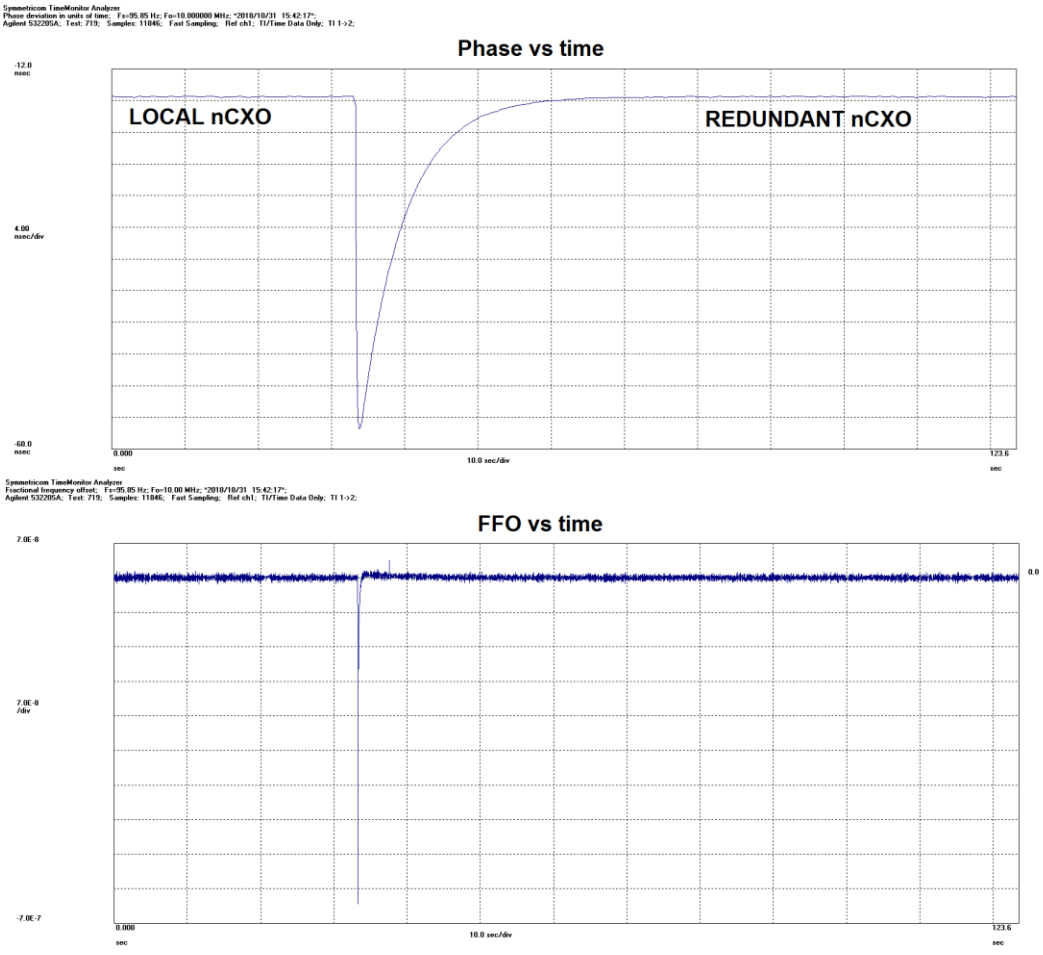
Once an error/failure is identified, that clock source can be immediately disqualified. If that clock source is the current SysDPLL source then the SysDPLL will go into Holdover. At this moment, any channel using the SysDPLL for stability will fall back on the XTAL (SysAPLL). For this reason it is important to switch very quickly to an alternate source.

To minimize impact to the other channels' outputs, you should not just switch to the redundant source. Even with hitless switch (i.e., to absorb the phase offset), there will be a frequency offset between the previous source and the new source (in the example above, it could be up to 3PPM). To manage this, there are a couple of options:

1. Use the ClockMatrix's fast frequency lock capability, which can perform a frequency slope (change) limit (ppb/s) when re-locking to the new source.
2. Use the combo bus filter when using the SysDPLL as a combo source.

IDT recommends to use the first option, as the latter will have an impact on the combined phase noise of the channel's outputs (since you are further filtering the SysDPLL, thus, losing the benefit of the nCXO's close-in PN). Figure 3 shows the impact of switching from a local nCXO (±4.6ppm) to a redundant nCXO (±4.6 ppm) for the clock source of SysDPLL using the suggestion in option 1. The SyncE output is monitored during the switch for G.8262 Option 1. The maximum ppm offset would be 9.2ppm but during the test it would be random. The displayed in the figure show a phase hit of less than 60ns for a random frequency offset between the local and redundant nCXO. If you have additional questions about device configurations, please contact IDT application support at support-sync@idt.com.

Figure 3: Phase/FFO Plots of Switching from Local nCXO to Redundant nCXO for the SyncE Output



Revision History

Revision Date	Description of Change
November 5, 2018	Initial release.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.