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SH7263/SH7203 Groups

10-Bit A/D Converter: Example of Settings for Conversion in Multi Mode

Introduction

This application note describes an example of settings for the 10-bit A/D converter in multi mode as an example of application of the A/D converter of the SH7263 and SH7203 Groups.

Target Devices

SH7263/SH7203

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1. Preface

1.1 Specifications

- A/D conversion in multi mode by the 10-bit A/D converter
- Three rounds of A/D conversion are performed on analog input channels 0 to 3 (AN0 to AN3), and the converted data are stored in RAM.

1.2 Module Used

- 10-bit A/D converter (10-bit A/D)

1.3 Applicable Conditions

- MCU SH7263/SH7203
- Operating frequency Internal clock: 200 MHz
Bus clock: 66.67 MHz
Peripheral clock: 33.3 MHz
- C compiler SuperH RISC Engine Family C/C++ Compiler Package Ver.9.01
from Renesas Technology
- Compiler options -cpu = sh2afpu -fpu = single -include = "\${WORKSPDIR}\inc"
-object = "\${CONFIGDIR}\\${FILELEAF}.obj" -debug -gbr = auto -chgincpath
-errorpath -global_volatile = 0 -opt_range = all -infinite_loop = 0
-del_vacant_loop = 0 -struct_alloc = 1 -nologo

1.4 Related Application Note

None

2. Description of the Sample Application

The sample program employs the multi mode of the 10-bit A/D converter to perform three rounds of A/D conversion on input channels 0 to 3 (AN0 to AN3), and then stores converted data in RAM.

2.1 Operational Overview of Module Used

The 10-bit A/D converter has three operating modes: single mode, multi mode, and scan mode. In multi mode, A/D conversion is performed once on one or more channels.

Table 1 gives an overview of the module used in this sample application (i.e. the A/D converter) and figure 1 is a block diagram of the 10-bit A/D converter. For details on the 10-bit A/D converter, see the section on the A/D converter in the *SH7263/SH7203 Group Hardware Manual*.

Table 1 Overview of the Module (A/D Converter) Used in the Sample Application

Item	Description
Resolution	10 bits
Minimum conversion time	3.9 μ s per channel ($P\phi = 33$ MHz operation)
Number of modules	1
Input channels	8
Operating modes	Single mode Multi mode Scan mode
Sample-and-hold function	Common to all channels: 1 circuit
Sources for activation of A/D conversion	Software: Setting of the ADST bit Timer: TRGAN, TRG0N, TRG4AN, and TRG4BN signals from the MTU2 module External trigger: \overline{ADTRG}

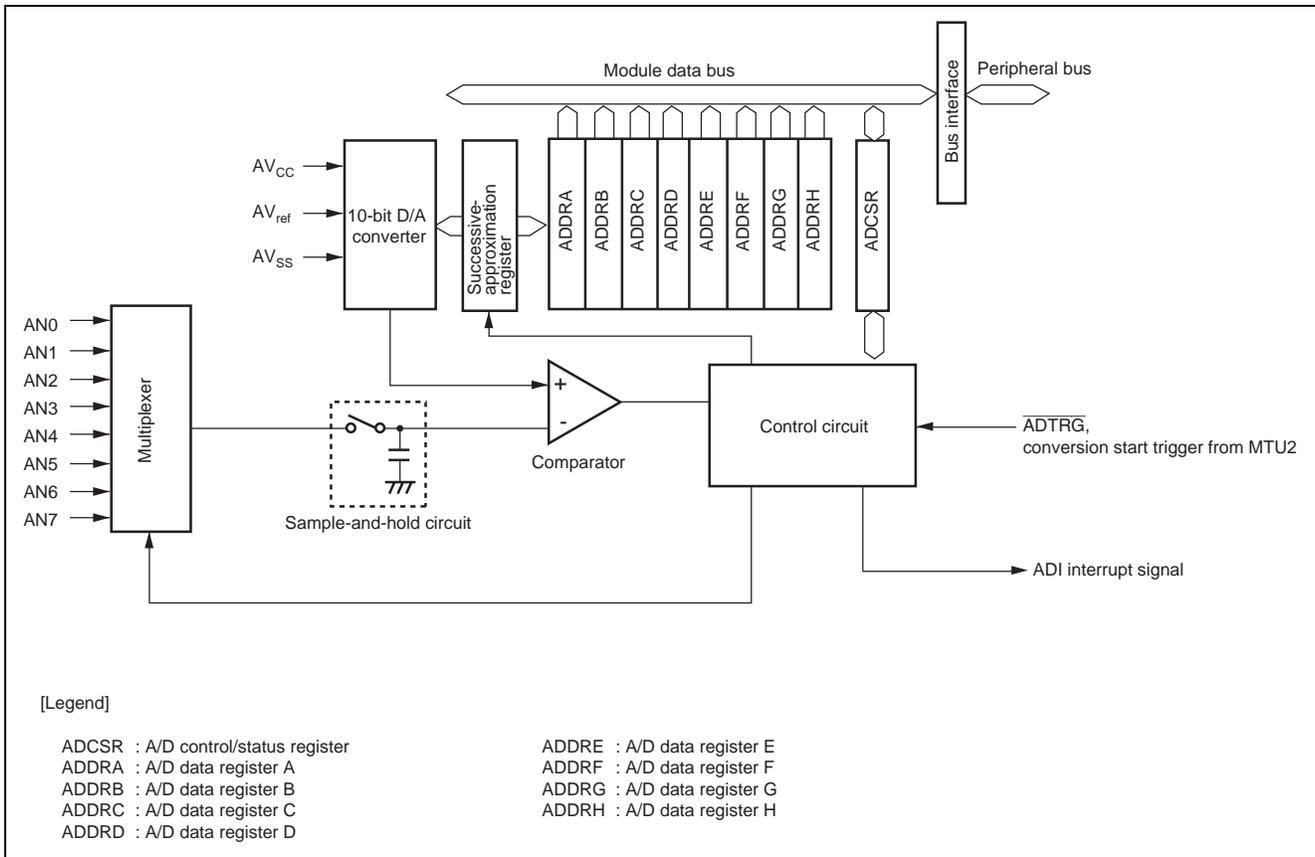


Figure 1 Block Diagram of the 10-Bit A/D Converter

2.2 Procedure for Setting Module Used

Figure 2 shows an example of the initialization sequence for A/D conversion in multi mode. For details on the settings of individual registers, see the *SH7263/SH7203 Group Hardware Manual*.

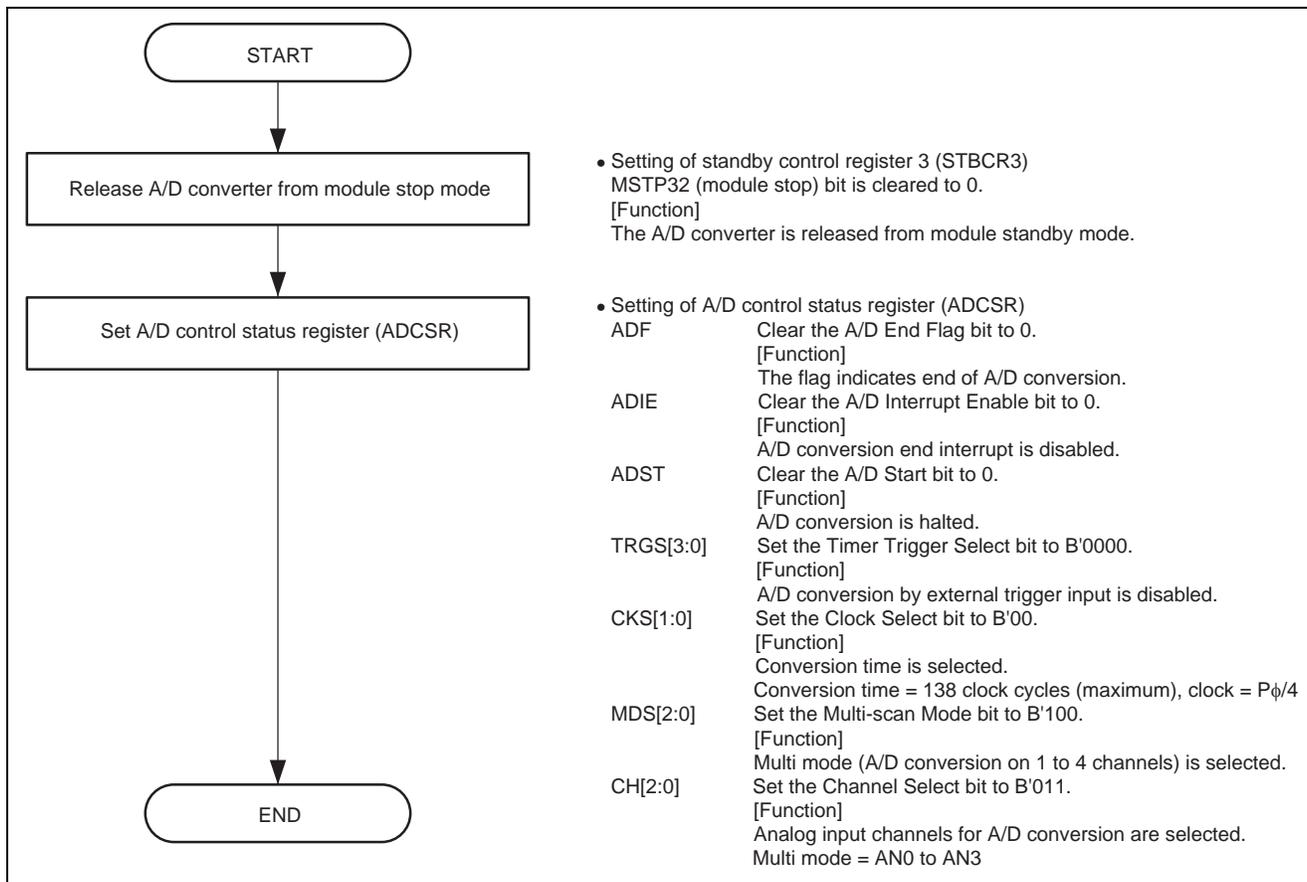


Figure 2 Initialization Sequence for 10-Bit A/D Conversion

General input pin functions, analog-input pin functions for the A/D converter, analog-output pin functions for the D/A converter (pins PA6 and PA7 only) are multiplexed on the general input pins for port A. These pin functions are changed automatically, so the pin function controller (PFC) does not have a register for settings to control them.

The general input function of the PA7 to PA0 pins is only enabled while the A/D and D/A converters are halted.

When port A data register L (PADRL) is read during operation of the A/D or D/A converter, values of bits corresponding to pins that are in use for conversion become undefined.

2.3 Operation of the Sample Program

In this sample program, A/D conversion in multi mode is performed on channels 0 to 3 (AN0 to AN3). The A/D converter is activated by software and converted data are stored in RAM. This processing is repeated three times.

Table 2 gives a description of RAM usage in this sample program.

Table 2 Variable Used in the Sample Program

Variable Name	Description	Area	Name of Employing Module
unsigned short AD_data[AD][CH]	Array for storing A/D-converted data (2 bytes/datum)	On-chip RAM	io_ad_multi_scan (unsigned short*ad_buf)

2.4 Sequence of Processing by the Sample Program

Table 3 gives settings for a register used in the sample program and figure 3 shows the flow of handling the sample program.

Table 3 Register Settings Used in the Sample Program

Register Name	Address	Setting	Description
A/D control status register (ADCSR)	H'FFFE5820	H'0023	ADIE = 0: Disables A/D conversion end interrupt ADST = 0: Halts A/D conversion TRGS[3:0] = B'0000: Disables start of A/D conversion by external trigger input CKS[1:0] = B'00: Operating clock = P ϕ /4 MDS[2:0] = B'100: Single mode CH[2:0] = B'011: AN0 to AN3
		H'2023	ADST = 1: Starts A/D conversion

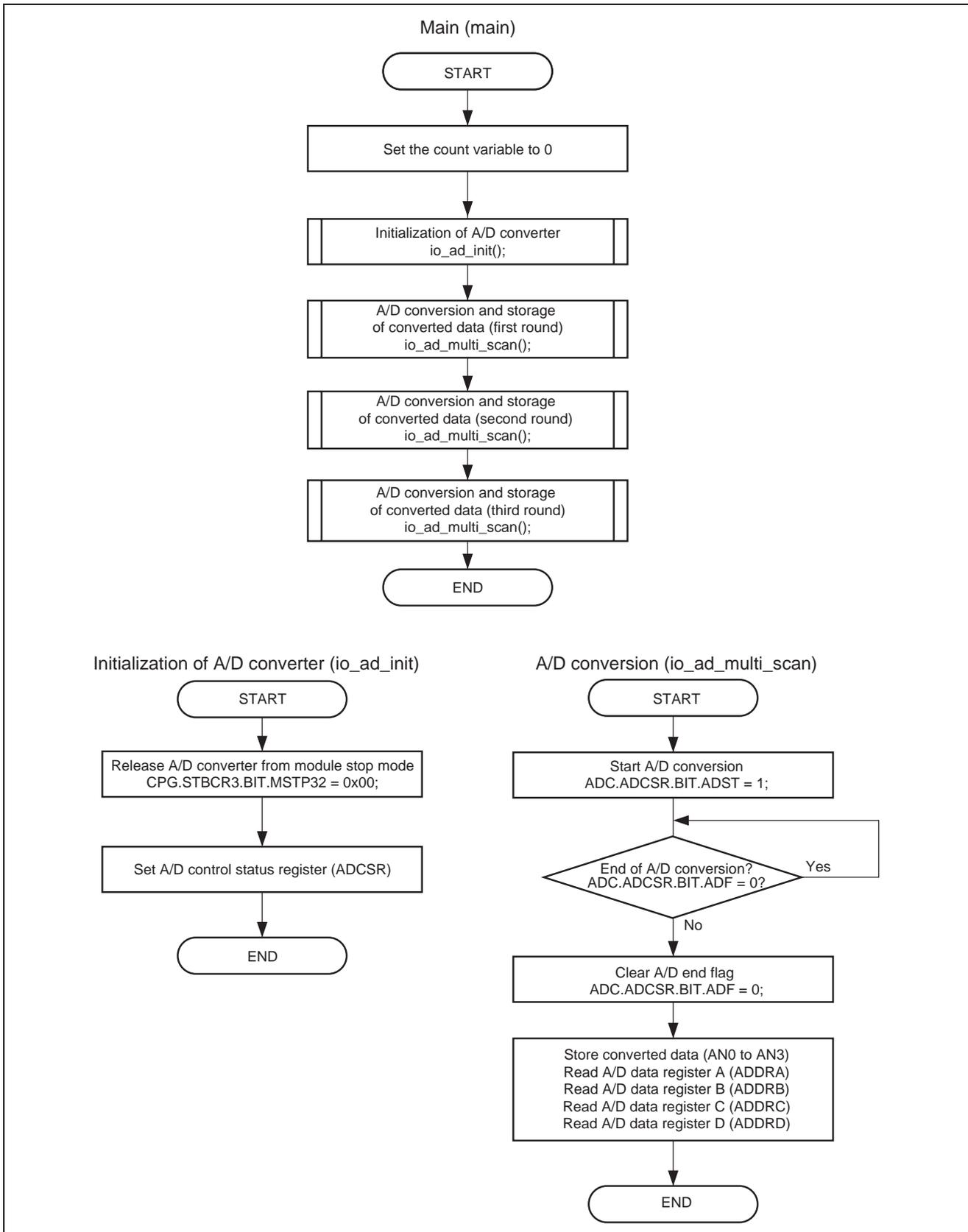


Figure 3 Flow of Handling the Sample Program

3. Listing of Sample Program

1. Sample Program Listing: "main.c" (1)

```

1 /*"FILE COMMENT"*****
2 *
3 *      System Name : SH7203 Sample Program
4 *      File Name   : main.c
5 *      Contents    : Sample program for A/D conversion in multi mode
6 *      Version     : 1.00.00
7 *      Model       : M3A-HS30
8 *      CPU         : SH7203
9 *      Compiler    : SHC9.1.1.0
10*      note        : A/D conversion in multi mode is performed by the A/D converter.
11*                   Three rounds of A/D conversion on channels 0 to 3 (AN0 to AN3)
12*                   proceed, and the converted data are stored in RAM.
13*
14*      The information described here may contain technical inaccuracies or
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19*      Copyright (C) 2008 Renesas Technology Corp. All Rights Reserved
20*      AND Renesas Solutions Corp. All Rights Reserved
21*
22*      history      : 2008.01.09 ver.1.00.00
23* "FILE COMMENT END"*****/
24 #include <machine.h>
25 #include "iodefine.h"          /* SH7203 iodefine */
26
27
28 /* ==== prototype declaration ==== */
29 void main(void);
30 void io_ad_init(void);
31 void io_ad_multi_scan(unsigned short *ad_buf);
32
33 /* ==== symbol definition ==== */
34 #define AD 3
35 #define CH 4
36
37 /* ==== RAM allocation variable declaration ==== */
38 unsigned short Ad_data[AD][CH];
39

```

2. Sample Program Listing: "main.c" (2)

```

40 /*"FUNC COMMENT"*****
41 * Outline      : main
42 *-----
43 * Include      : #include "iodefine.h"
44 *              : #include <machine.h>
45 *-----
46 * Declaration  : void main(void);
47 *-----
48 * Function     : A/D conversion with multi mode
49 *-----
50 * Argument     : void
51 *-----
52 * Return Value : none
53 *-----
54 * Notice      :
55 * "FUNC COMMENT END"*****/
56 void main(void)
57 {
58     unsigned char count;
59     count = 0;
60
61     /* ==== Initial Setting of ADC ==== */
62     io_ad_init();
63
64     /* ==== A/D conversion ==== */
65     io_ad_multi_scan(&Ad_data[count][0]);
66     count++;
67     io_ad_multi_scan(&Ad_data[count][0]);
68     count++;
69     io_ad_multi_scan(&Ad_data[count][0]);
70
71     while(1){
72         /* loop */
73     }
74 }

```

3. Sample Program Listing: "main.c" (3)

```

75 /*"FUNC COMMENT"*****
76 * Outline      : Initial setting of ADC
77 *-----
78 * Include      : #include "iodefine.h"
79 *-----
80 * Declaration  : void io_ad_init(void);
81 *-----
82 * Function     : Initial setting of ADC
83 *-----
84 * Argument     : void
85 *-----
86 * Return Value : void
87 *-----
88 * Notice       : non
89 /*"FUNC COMMENT END"*****/
90 void io_ad_init(void)
91 {
92     /* ==== Setting of power down mode(ADC) ==== */
93     CPG.STBCR3.BIT.MSTP32 = 0x00;
94
95     /* ==== Setting of ADC ==== */
96     /* ---- A/D Control/Status Register(ADCSR) ---- */
97     ADC.ADCSR.WORD = 0x0023;
98     /* 15 = b'0      : A/D End Flag */
99     /* 14 = b'0      : A/D end interrupt request (ADI) is disabled */
100    /* 13 = b'0      : A/D conversion is stopped */
101    /* 12 = b'0      : reserve */
102    /* 11-8 = b'0000 : Start of A/D conversion by
103                       external trigger input is disabled */
104    /* 7-6 = b'00    : clock = Pφ/4 */
105    /* 5-3 = b'100   : Multi mode */
106    /* 2-0 = b'011   : Channel Select AN0-AN3 */
107
108    /* ---- A/D Status Register(ADSR) ---- */
109    ADC.ADCSR.BIT.ADF = 0; /* ADF clear */
110
111 }
112 /*"FUNC COMMENT"*****
113 * Outline      : A/D conversion
114 *-----
115 * Include      : #include "iodefine.h"
116 *-----
117 * Declaration  : void io_ad_multi_scan(unsigned short *ad_buf);
118 *-----
119 * Function     : Clearing of A/D end flag (ADF), and storing of conversion data
120 *-----
121 * Argument     : unsigned short *ad_buf : Buffer
122 *-----
123 * Return Value : none
124 *-----
125 * Notice       :
126 /*"FUNC COMMENT END"*****/
127 void io_ad_multi_scan(unsigned short *ad_buf)
128 {
129     ADC.ADCSR.BIT.ADST = 1; /* A/D conversion start */
130     while(ADC.ADCSR.BIT.ADF == 0){ /* A/D conversion completion waiting */
131     }
132     ADC.ADCSR.BIT.ADF = 0; /* ADF clear */
133     *ad_buf++ = ADC.ADDRA.WORD; /* AN0 */
134     *ad_buf++ = ADC.ADDRB.WORD; /* AN1 */
135     *ad_buf++ = ADC.ADDRC.WORD; /* AN2 */
136     *ad_buf++ = ADC.ADDRD.WORD; /* AN3 */
137 }
138 /* End of File */

```

4. Documents for Reference

- Software Manual
SH-2A/SH2A-FPU Software Manual
The most up-to-date version of this document is available on the Renesas Technology Website.
- Hardware Manual
SH7203 Group Hardware Manual
SH7263 Group Hardware Manual
The most up-to-date versions of the documents are available on the Renesas Technology Website.

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