

White Paper

Digital Power Module Enables Fast Load Transient POL with Simple Cooling Design

Introduction

The ever-increasing demands of FPGAs, processors and ASICs are pushing point-of-load (POL) power converters to the limit. Not only do they occupy more motherboard real estate, but they also require much higher input current and lower input voltage than last year's POL power supply designs. Providing higher current POL seated next to an advanced FPGA, processor or ASIC requires higher power density, fast load transient response and much better thermal performance.

This article examines an 80A digital power module's thermally enhanced, encapsulated package with a single layer copper lead-frame that houses the controller, FETs, passives and 3D stackable inductor structure. A thermal design example with a topside heatsink is provided, and achieving fast transient response through digital control is discussed.

Enabled with advanced 3D integration and packaging technologies, integrated power module solutions can achieve much greater performance over discrete solutions in terms of efficiency, thermal management and power density. This gives designers the advantage of faster time to market, and more margin for their power design.

Moving the Heat Out

Thermal management is arguably the greatest high power (greater than 100W) module design challenge. Footprint and power rating at high ambient temperature are guided by the module's electrical and mechanical design. Using thermally efficient packages that can move the heat out of the package enables a module to deliver superior thermal performance. In a highly integrated device such as a power module, the electrical and mechanical design is interdependent.

Power modules are typically built upon a package substrate on which the semiconductor die and other electronic components are mounted and inter-connected. Several types of package substrates are used in power modules. A dual layered printed circuit board (PCB) in a land grid array (LGA) power module provides a substrate with good routing capability and straightforward electrical interconnections. However, the LGA has low thermal conductivity and penalizes the module's thermal performance. Another module type uses a metal lead frame on a quad flat no-leads (QFN) package, which provides very good thermal conductivity but lacks the ease of routing capability. While the QFN can be modified for improved routing, this technique often results in higher package costs.

The best solution is the High Density lead-frame Array (HDA), which combines thermal conductivity and routing capability in a single-layer conductive package substrate. This substrate comprises a peripheral and an interior portion. The peripheral portion includes contact pads used for surface mount on a motherboard while the interior portion includes floating contact pads coupled to internal components and electrically isolated from the peripheral contact pads. The peripheral and interior contact pads of the HDA lead-frame allow the HDA power module to provide excellent PCB trace routing capabilities, similar to that of a dual-layered PCB, as well as excellent thermal conductivity to dissipate heat because of the single conductive layer of copper material.

3D Stacking for Space Efficiency

Another critical piece of the electrical-mechanical design is inductor design. Inductors must be designed large enough to achieve low DC resistance (DCR) copper loss and core loss, while maintaining a practical operating temperature. Unfortunately, many telecom and datacom applications have limited space on the motherboard forcing designers to use an undersized inductor. As a result, a bulky heat sink is used, or designers must settle for a hot spot and poor efficiency.

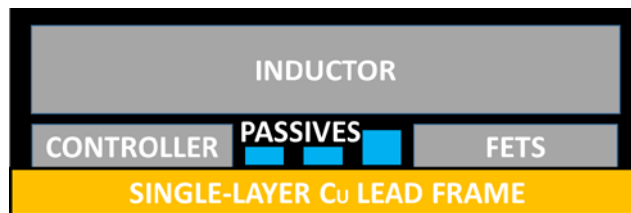
A good solution is the 3D stackable inductor structure, which addresses both space and efficiency constraints. In this structure, the inductor is nearly as large as the entire power module footprint and installed over the other components. This design significantly reduces the substrate area compared to a side-by-side mounting method, at the expense of package height. Thanks to the adequate budget of the inductor size, achieving much smaller DC resistance loss and core loss is easy.

Figure 1 illustrates the cross-sectional view of two types of power module structures. In Figure 1(A), a multi-layer PCB is used as the package substrate to provide flexibility of electrical interconnections and routings; the inductor is mounted side-by-side from the other components (controller, FETs, and passives). In this structure, and as noted earlier, the heat transfer efficiency can be poor due to the low thermal conductivity of the multi-layer substrate. With limited footprint space, it is forced to use an undersized inductor. Since the inductor height dominates the module dimension in the Z-axis, any saving from the inductor's X-Y dimensions could result in an increase of the inductor height and thus a waste of module form factor.

The concentrated inductor structure also prevents efficient top and bottom side cooling. The advantage of the HDA power module structure with 3D inductor integration is illustrated in Figure 1(B). The single-layer copper lead-frame with both peripheral and interior portions (not shown) offers similar routing capabilities to a dual-layer PCB and much higher thermal conductivity. By installing the inductor on top of other components, the space along the Z-axis is efficiently used. The module footprint is reduced and the inductor DCR and core loss is minimized. Additionally, heat concentration is avoided at the inductor because of reduced inductor loss and a larger effective heat dissipation area.



A. Power module structure with multi-layer substrate and side-by-side inductor mount



B. HDA power module using single-layer substrate and 3D inductor integration

Figure 1. Cross-sectional view of two types of power module structures

Design Example: 80A Digital PMBus Power Module

The ISL8273M is an 80A step-down PMBus-compliant digital power module, which offers the industry's highest current capacity from a compact (18mm x 23mm x 7.5mm) HDA package. Dual phases are

connected in parallel to deliver current through a single output. Figure 2 shows the typical 80A application diagram using the ISL8273M.

The ISL8273M dual-phase inductor has a proprietary design using the 3D integration technology. Two windings are built on a single core such that the magnetic flux of the two windings are partially cancelled, thus reducing both the inductor size and core loss. Phase interleaving allows further reduction of input capacitors and output voltage ripples. Figure 3 shows the high efficiency performance of this structure.

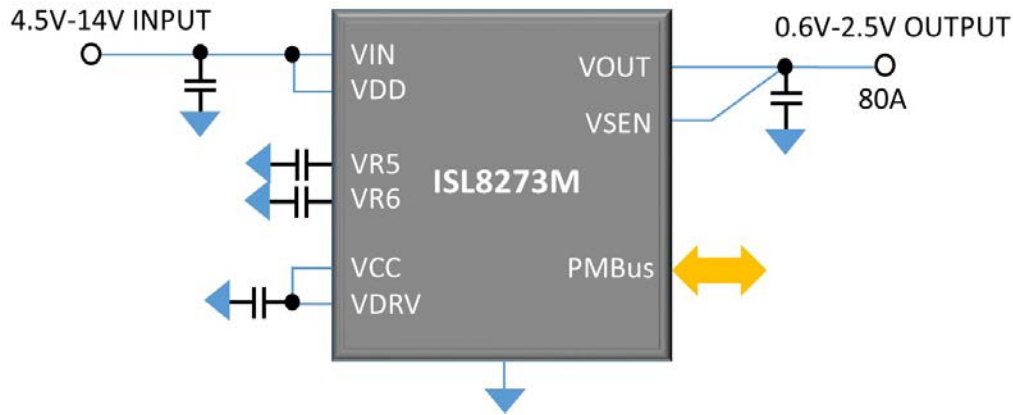


Figure 2. Typical 80A application diagram of the ISL8273M

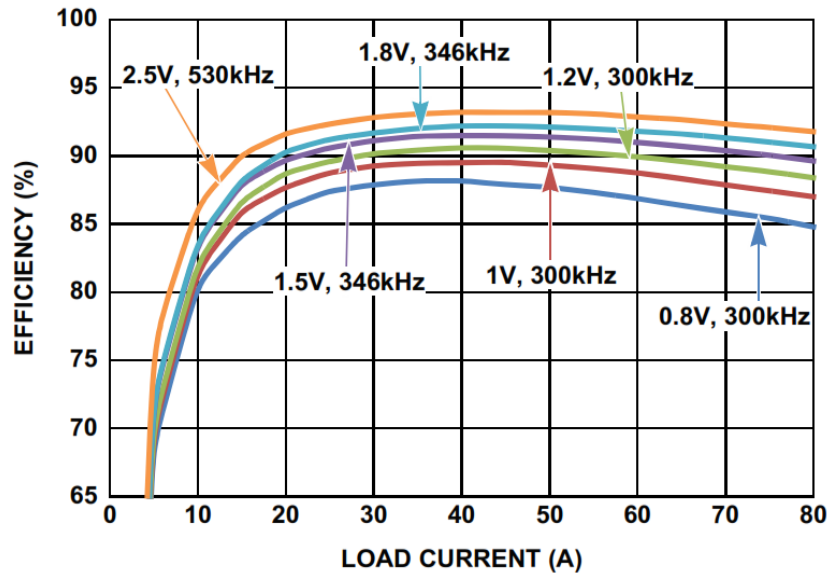
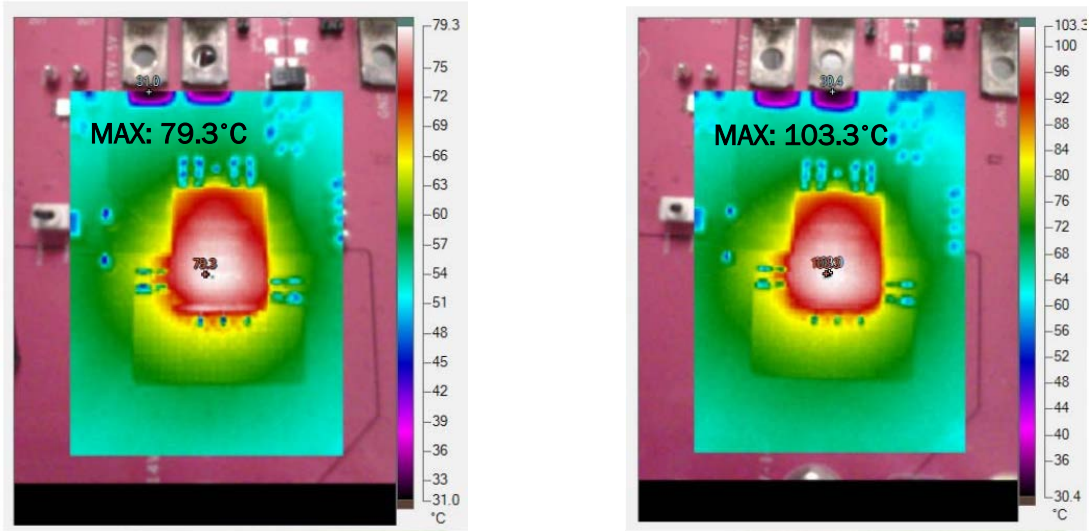


Figure 3. ISL8273M efficiency curves at $V_{IN}=12V$ for various output voltages

In typical applications, ISL8273M can operate under harsh conditions, including no airflow and no heat sink. Thermal images of the ISL8273M encapsulated digital power module running a continuous 80A load are shown in Figure 4. Mounted on a 2oz. 8-layer FR4 4.7 inch x 4.8 inch board, the ISL8273M performs exceptionally in a thermal test, providing a non-derated 80A capacity even under the worst-case condition at a 2.5V output voltage. The module achieves an ultra-high power density of $>1055W/in^3$.



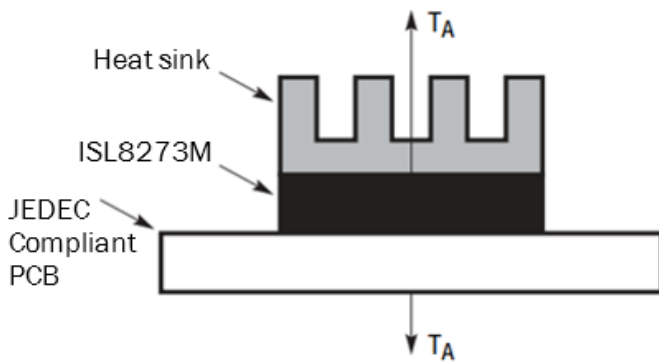
A. $V_{IN}=12V$, $V_{OUT}=1V$, $I_{OUT}=80A$, $F_{SW}=300kHz$, $T_A=25^\circ C$, OLFM (no airflow)

B. $V_{IN}=12V$, $V_{OUT}=2.5V$, $I_{OUT}=80A$, $F_{SW}=450kHz$, $T_A=25^\circ C$, OLFM (no airflow)

Figure 4. Thermal images of the ISL8273M

Design Example: Topside Heat Sink

In challenging operating environments, customers have limited solutions to improve system-cooling conditions and maintain a high current supply. A topside heat sink might cool the module enough to meet design specs, but they take up valuable space. The ISL8273M can operate with no airflow and no heat sink and its thermal performance can be further enhanced with a small heat sink attached to its top case. As shown in Figure 5, a heat sink is attached to the ISL8273M's top case. A thermal adhesive material is used between the heat sink and module top case to improve the heat transfer and reduce thermal resistance.



A. Assembly structure with a heat sink attached to the top case of ISL8273M



B. Heat sink dimension: 23mm x 23mm x 18mm (AAVID Thermalloy # 374124B00035G)

Figure 5. Heat sink application example

If a system board following JEDEC specs is used as shown in Figure 5(A), we can run a thermal simulation to understand the heat transfer and thermal performance improvement. The system board size is 76.2mm x 114.3mm x 1.6mm and it is a 4-layer board with top and bottom at 2oz copper and inner second and third layers at 1oz copper. The thermal simulation is run at 400LFM airflow with about 10W power loss dissipated from the ISL8273M at room temperature.

As shown in Table 1, with a simple heat sink attachment, the thermal resistance can be improved by up to 12.2%. About 33% of the power loss is dissipated from top side through the heat sink compared to only 6% power loss from the top side with no heat sink on top case. The junction temperature can be lowered by about 8°C. With different adhesive material for HS1 and HS2, the thermal results are very similar.

Table 1. Thermal performance improvement with a simple heat sink attachment

Model Name	HS Mount Adhesive			Theta-ja, C/W	% Theta-ja improvement (vs. no heatsink)	Heat dissipated from top	Percentage of heat dissipated from top
	Name	Tkn (mm)	k (W/mK)				
No HS (ref)	---	---	---	6.81	---	0.60 W	6%
HS1	Chomerics T411	0.28	0.5	6.08	10.7%	3.05 W	31%
HS2	Loctite 3875	0.28	1.75	5.98	12.2%	3.27W	33%

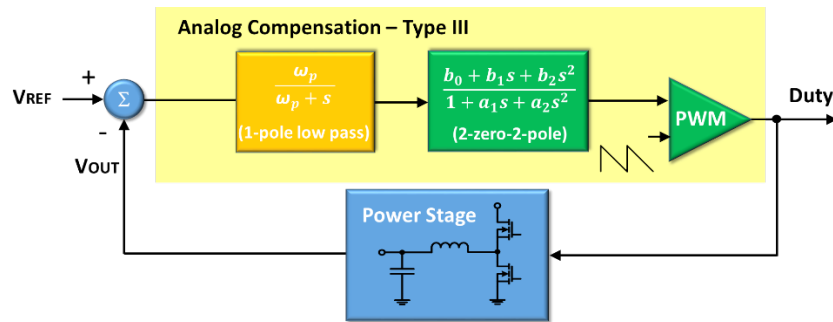
Fast Digital Control Enables Fast Transient Capability

Digital power management equips systems with real-time intelligence and flexibility. It allows automatic compensation for changes in load and temperature, dynamic voltage scaling, and frequency shifting. It also provides full telemetry and monitoring of the system operating parameters.

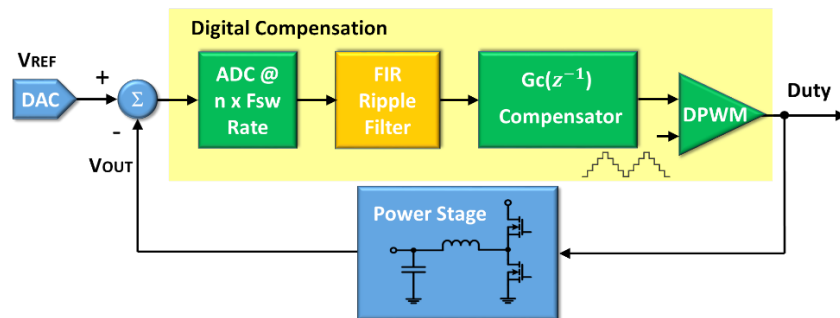
Most importantly, the PWM, loop control and feedback can be implemented digitally. Analog signals are converted to digital through analog-to-digital converters (ADCs) such that the PWM and feedback loops can be handled by digital-signal processors or computational state machines. This important differentiation from pure analog control offers the advantages of maintaining stability without compromising the lack of responsiveness analog control suffers. Therefore, the output capacitance required for handling transient load events can be reduced with a fast digital control loop, further strengthening the system power density.

Although digital control offers advantages in the fast loop design, many manufacturers are not taking full advantage of what the technology offers and have simply implemented the core analog PWM techniques in digital form. Digital control makes it possible to build far more flexible control loops by incorporating $n \times F_{sw}$ (switching frequency) oversampling, multi-rate sampling, various types of digital filters for notching and phase shaping, and Fourier transform. These features associated with complex digital signal processing are often not feasible with traditional analog control techniques.

In Figure 6, the control block diagrams of a typical Type III analog compensation and a fast response digital compensation are illustrated for comparison.



A. Type III analog compensation with leading-edge modulator



B. Digital compensation using fast sampling and FIR ripple filter with dual-edge modulator

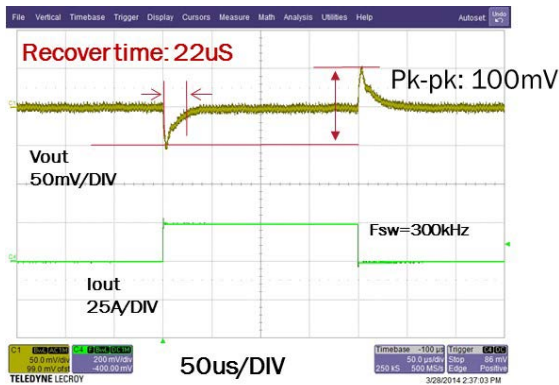
Figure 6. Analog vs. digital compensations for voltage mode controlled buck converter

Type III analog compensation in voltage-mode controlled buck converters is widely adopted in the industry. Typically, the core of a Type III compensator is a transfer function with two zeros and three poles. As we know, the first pole near origin forms a high gain at low frequency for steady state regulation, while the second pole is to compensate the output capacitor ESR zero, and the third pole is to provide more attenuation for the high-frequency noises caused by switching ripples. Meanwhile, the two zeroes are used to shape the loop gain at cross over and boost phase to make the loop stable. Figure 6(A) shows the third pole separating from the rest of the Type III compensator.

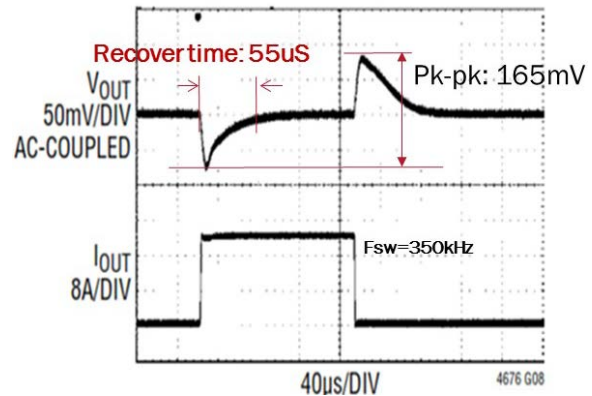
The one-pole low pass filter removes the switching ripple noises from the PWM modulator to main stability. However, on the other side, it inevitably introduces extra phase lag to the loop, limiting the loop bandwidth and response speed in order to have sufficient phase margin. The only way to achieve further improvement with this analog architecture is to employ variable-frequency switching techniques, using higher frequency when the voltage is changing rapidly. Nevertheless, this is undesirable for many systems that have stringent electromagnetic compatibility (EMC) demands. Fixed-frequency operation is required in such systems so that the noise spectrum can be tightly controlled.

An example of a fast response digital compensation architecture is shown in Figure 6(B). In this control loop, the ADC is over sampling at a frequency of $n \times F_{sw}$, where $n > 1$. Therefore, the phase lag or group delay introduced by the analog-to-digital conversion is negligible for the loop stability. Because of the over sampling, it is feasible to design the core compensator $G_c(z^{-1})$ to have a similar frequency response to the two-zero two-pole compensator in Figure 6(A) in terms of loop gain and phase. But most importantly, the filter employed to attenuate the high frequency switching ripple noises can be designed uniquely by digital means and completely differentiated from the analog compensator's single-pole low-pass filter in Figure 6(A). Benefiting from the advantages of digital signal processing, a low-latency FIR ripple filter can be easily incorporated to reject all repetitive ripple elements. All that remains are the non-periodic elements in the

waveform, including transient steps with little or no delay. This results in more than 20dB of ripple reduction without a significant time delay, thus allowing higher gains and higher bandwidths. Load transient performance is significantly improved.



A. Transient response of the ISL8273M (0 to 25A, >200A/us slew rate)



B. Transient response of a competitor's module (0 to 20A, 20A/us slew rate)

Figure 7. Transient performance comparison

The fast transient performance of the ISL8273M is demonstrated in Figure 7. ISL8273M is compared to one competitor's 26A module with similar output caps and operating conditions. With load current slew rate at >200A/us, ISL8273M shows the peak-to-peak deviation at only 100mV and recover time at 22uS, while this competitor's module shows a much larger deviation at 165mV and recover time at 55uS with only 20A/us current slew rate. The ISL8273M delivers much better performance with small deviations and much faster recover time.

Conclusion

Intersil's ISL8273M digital PMBus power module can deliver large current up to 320A (multiphase current sharing of four paralleled power modules) to meet fast transient POL applications while requiring very simple electric and thermal designs. Technology innovations such as 3D module structure and fast digital control allow system designers to rethink their POL design trade-offs so they can achieve the higher power density, thermal performance and improved efficiency advanced systems require.

Next Steps

- [Learn more about the ISL8273M](#)
- [Watch an overview video](#)
- [Download the datasheet](#)
- [Get the ISL8273MEVAL1Z eval board](#)

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