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**ISL70062SEH, ISL73062SEH****Total Dose Test Report**

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**Introduction**

This report provides results of a Low Dose Rate (LDR) and High Dose Rate (HDR) total gamma-ray dose test of the [ISL70062SEH](#) and [ISL73062SEH](#) NMOS load switches. The test was conducted to characterize the total dose sensitivity and dose rate or bias sensitivity of the parts. The test also performed biased high temperature anneals after the completion of irradiation at both dose rates to evaluate time-dependent effects. The testing was carried out on ISL70062SEH samples; the results apply to both parts.

**Part Description**

The ISL70062SEH and ISL73062SEH are radiation hardened single-channel load switches featuring low ON-resistance and fixed, controlled rise time. The parts use a NMOS pass device as the main switch, with an operating voltage of 0V to (VCC -2V), maximum continuous current of 10A and maximum ON-resistance of 16mΩ (5.5V) and 18mΩ (3.0V). Simple ON/OFF digital control inputs allow direct interface with low voltage control signals from an FPGA, MCU, or processor. Additional features include Reverse Current Protection (RCP) to stop current from flowing toward the input when the switch output (SWO) voltage exceeds the switch input (SWI) voltage, a 100Ω on-chip MOSFET to discharge the output when the switch is OFF and Undervoltage Lockout (UVLO) protection that keeps the switch OFF when the supply voltage is too low. To minimize inrush current, the parts feature internally controlled switching with a fixed rise time of 2.2ms at 5.5V supply. The ISL70062SEH and ISL73062SEH operate across the military temperature range from -55°C to +125°C and are available in a 14 Ld hermetically sealed Ceramic Dual Flatpack (CDFP) package or in die form. A block diagram is shown in [Figure 1](#).

The ISL70062SEH is specified in the SMD (5962-19212) to a total dose (TID) rating of 100krad(Si) at high (50 - 300rad(Si)/s) dose rate and to 50krad(Si) at low (<0.01rad(Si)/s) dose rate, while the ISL73062SEH is specified in the SMD to a total dose (TID) rating of 50krad(Si) at low (<0.01rad(Si)/s) dose rate. The ISL70062SEH is specified in the Renesas datasheet and acceptance tested on a wafer-by-wafer basis to 75krad(Si) at LDR and 100krad(Si) at HDR, while the ISL73062SEH is specified in the datasheet and acceptance tested on a wafer-by-wafer basis to 75krad(Si) at LDR only. The discrepancy between the SMD and datasheet LDR specifications can be attributed to the absence of a 75krad(Si) total dose RHA level in MIL-PRF-38535.

Both parts are rated to 86 MeV•cm<sup>2</sup>/mg for Single-Event Effects (SEE), including single-event latch-up, single-event burnout (both at a supply voltage of 6.7V), and single-event transient.

The ISL70062SEH and ISL73062SEH are implemented in a submicron BiCMOS process optimized for power management applications. The process is in volume production under MIL-PRF-38535 certification and is used for a wide range of power management devices. Specifications for radiation hardened QML devices are controlled by the Defense Logistics Agency, Land and Maritime (DLA) in Columbus, OH. SMD 5962-19212 is the controlling document and should be cited when ordering.

**Related Literature**

For a full list of related documents, visit our website:

- [ISL70062SEH](#), [ISL73062SEH](#) device pages
- MIL-STD-883G test method 1019

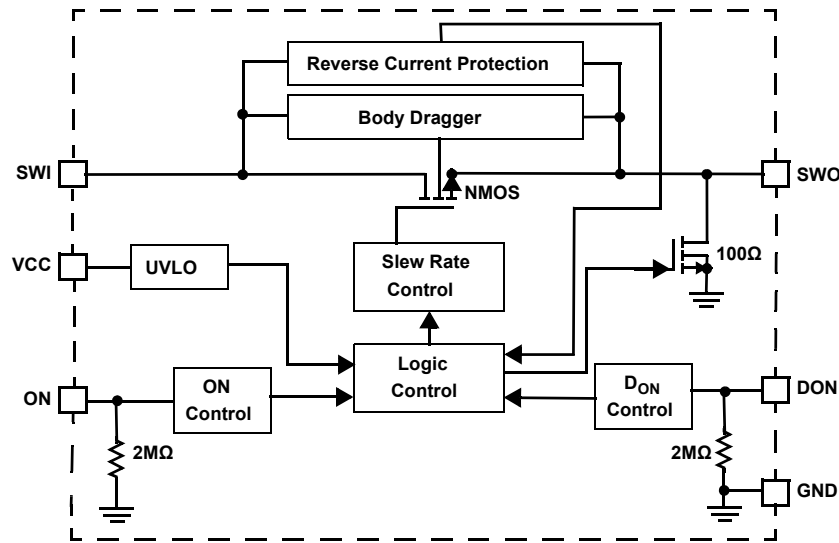


Figure 1. ISL70062SEH Block Diagram

## 1. Test Description

### 1.1 Irradiation Facilities

HDR testing of ISL70062SEH samples was performed at 72rad(Si)/s using a Gammacell 220 irradiator located in the Palm Bay, Florida Renesas facility. LDR testing was performed at 0.010rad(Si)/s using a Hopewell Designs N40 LDR irradiator also located in Palm Bay. Both irradiators use PbAl spectrum hardening filters to shield the test fixture and samples against low energy secondary gamma radiation. The 168-hour post-irradiation anneals used the same bias configuration as the biased irradiation (Figure 2) and were performed at 100°C using a small temperature chamber.

### 1.2 Test Fixturing

Figure 2 shows the configuration used for biased irradiation and anneal.

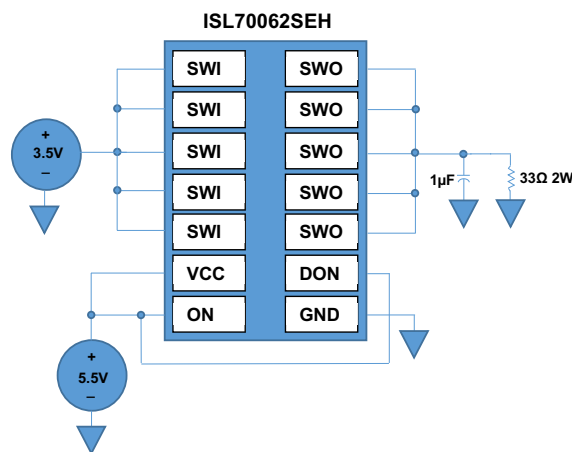


Figure 2. Irradiation and Anneal Bias Configuration for the ISL70062SEH

### 1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the Palm Bay production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

## 1.4 Experimental Matrix

Testing proceeded per the LDR sensitivity diagnostic protocol outlined in MIL-STD-883 Test Method 1019. The experimental matrix consisted of six samples irradiated at HDR with all pins grounded, six samples irradiated at HDR under bias, six samples irradiated at LDR with all pins grounded and six samples irradiated at LDR under bias. A biased anneal at 100°C for 168 hours was performed following all irradiations to evaluate the Time-Dependent Effect (TDE) characteristics of the part. Several control units were used to ensure repeatable ATE data.

Samples of the ISL70062SEH were drawn from fabrication lot 2CC8B and were packaged in the production hermetic 14 Ld ceramic flatpack. Samples were processed through the standard QML-V burn-in screens of 180 hours dynamic burn-in and 72 hours static burn-in before irradiation, as required by MIL-STD-883, and were screened to the SMD 5962-19212 SMD limits at room, low, and high temperatures before the start of total dose testing.

## 1.5 Downpoints

The LDR downpoints were 0, 10, 30, 50, 75, and 100krad(Si) and the HDR downpoints were 0, 30, 50, 100, and 150krad(Si). The biased anneals were performed at 100°C for 168 hours.

## 2. Results

Total dose testing of the ISL70062SEH showed no rejects after biased or grounded irradiation at either dose rate or after anneal, screening to the SMD post-radiation limits at all downpoints.

### 2.1 Attributes Data

Table 1. Attributes Data

Part	Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass (Note 1)	Fail
ISL70062SEH	0.01	Biased	6	Pre-irradiation	6	0
				10krad(Si)	6	0
				30krad(Si)	6	0
				50krad(Si)	6	0
				75krad(Si)	6	0
				100krad(Si)	6	0
				Anneal	6	0
ISL70062SEH	0.01	Grounded	6	Pre-irradiation	6	0
				10krad(Si)	6	0
				30krad(Si)	6	0
				50krad(Si)	6	0
				75krad(Si)	6	0
				100krad(Si)	6	0
				Anneal	6	0
ISL70062SEH	72	Biased	6	Pre-irradiation	6	0
				30krad(Si)	6	0
				50krad(Si)	6	0
				100krad(Si)	6	0
				150krad(Si)	6	0
				Anneal	6	0

**Table 1. Attributes Data (Continued)**

Part	Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass (Note 1)	Fail
ISL70062SEH	72	Grounded	6	Pre-irradiation	6	0
				30krad(Si)	6	0
				50krad(Si)	6	0
				100krad(Si)	6	0
				150krad(Si)	6	0
				Anneal	6	0

**Note:**

1. A pass indicates a sample that passes all post-irradiation SMD limits.

**2.2 Variables Data**

Figures 3 through 13 show data for key parameters at all downpoints. The plots show the parameter median as a function of total dose for each of the irradiation conditions and the subsequent anneal. All samples showed excellent stability over irradiation and anneal, with no observed dose rate or bias sensitivity. We elected to plot the 3.0V/3.6V and 5.5V supply cases on the same set of axes, as there was little difference between the two.

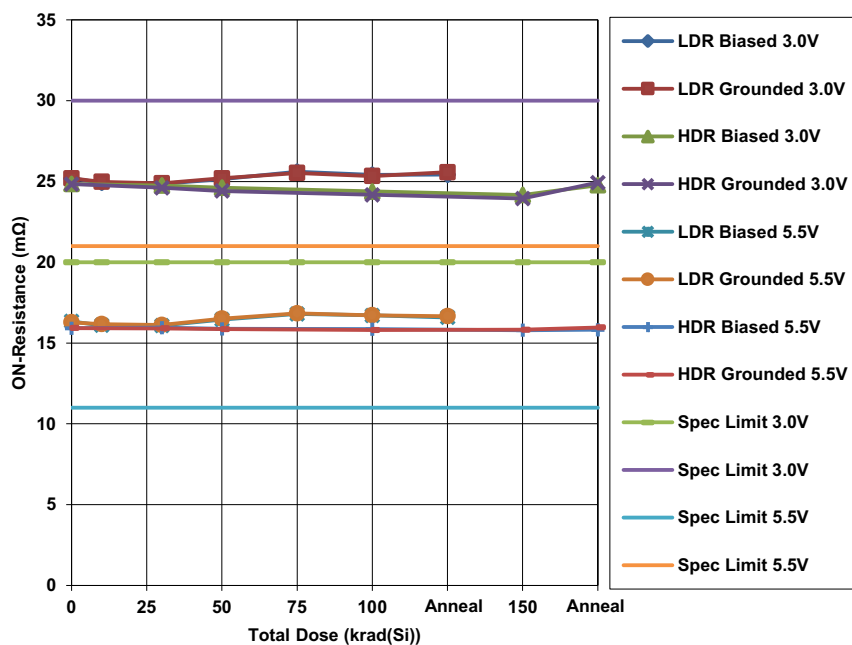


Figure 3. ISL70062SEH switch ON-resistance, 3.0V and 5.5V supply voltage,  $V_{SW1} = 1.0V$ , as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in Table 1. The post-irradiation SMD limits are 20mΩ to 30mΩ (3.0V supply) and 11mΩ to 21mΩ (5.5V supply).

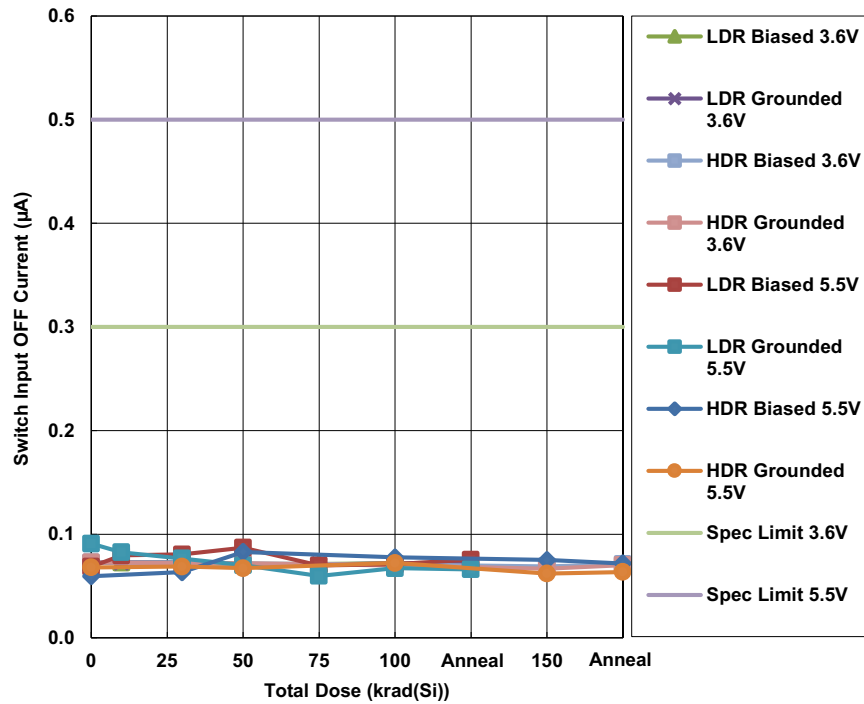


Figure 4. ISL70062SEH switch input OFF current, 3.6V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are 0.3µA maximum (3.6V supply) and 0.5µA maximum (5.5V supply).

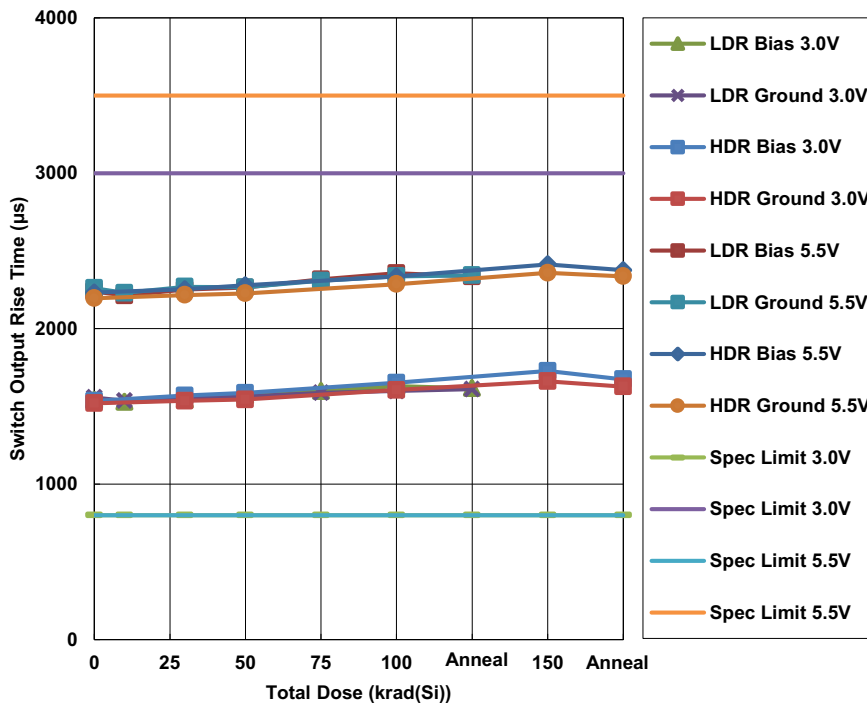


Figure 5. ISL70062SEH switch output rise time, 3.0V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are 800µs to 3000µs (3.0V supply) and 800µs to 3500µs (5.5V supply).

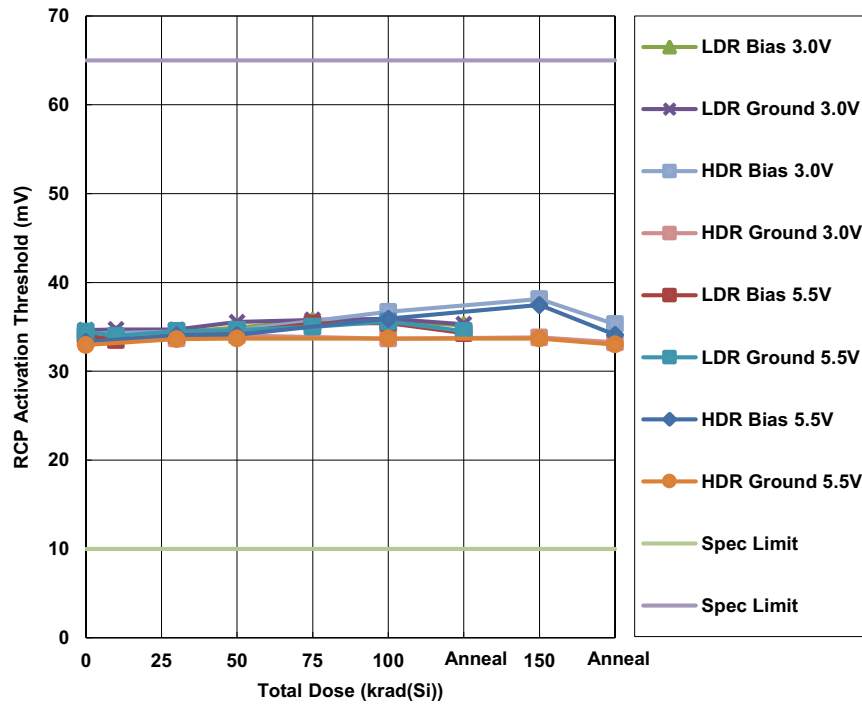


Figure 6. ISL70062SEH Reverse Current Protection (RCP) activation threshold, 3.0V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are 10mV to 65mV for both parameters.

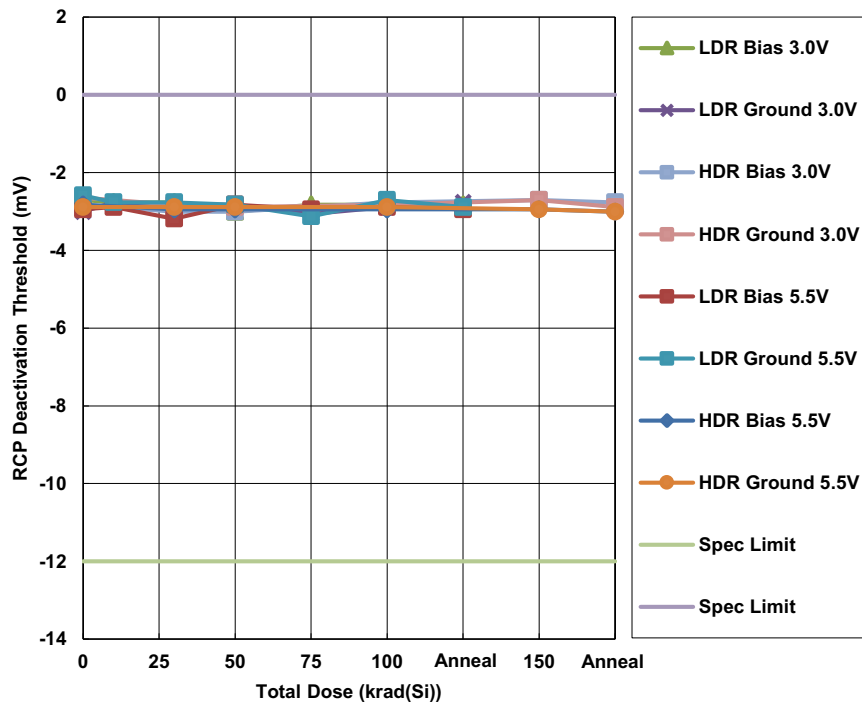


Figure 7. ISL70062SEH Reverse Current Protection (RCP) deactivation threshold, 3.0V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are -12mV to 0mV for both parameters.

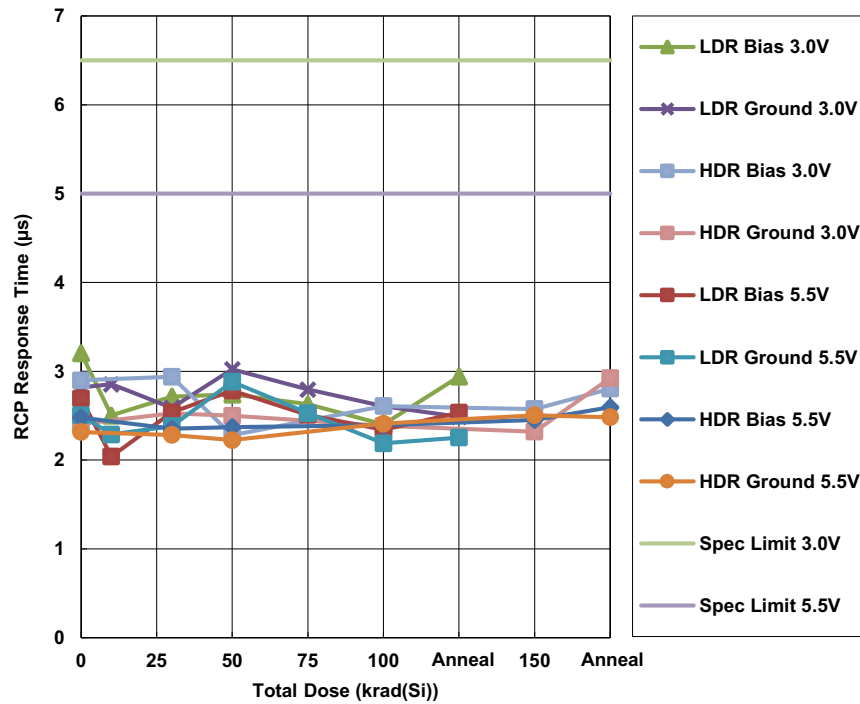


Figure 8. ISL70062SEH Reverse Current Protection (RCP) response time, 3.0V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are 6.5µs maximum (3.0V supply) and 5.0µs maximum (5.5V supply).

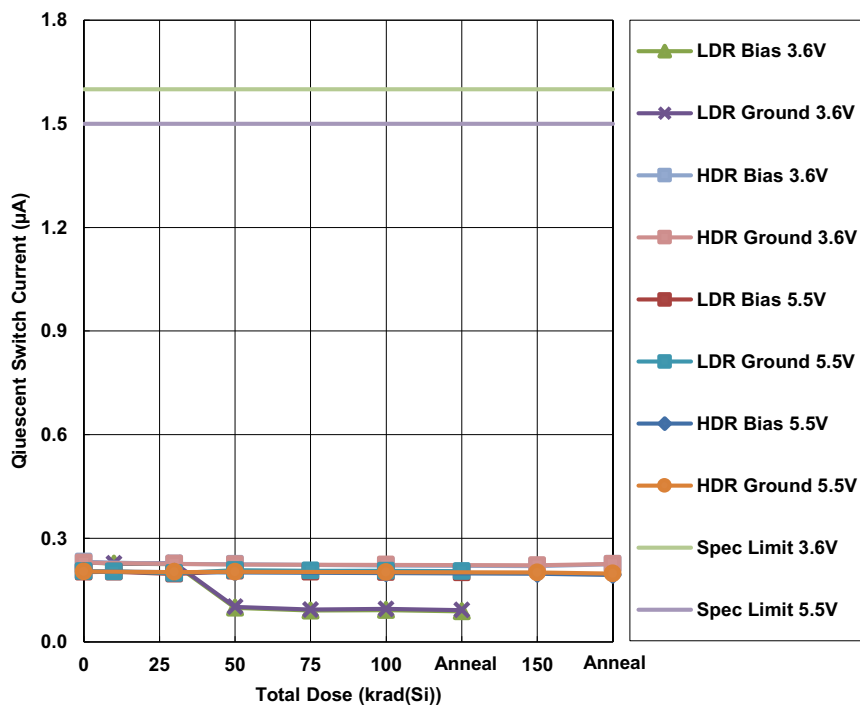


Figure 9. ISL70062SEH quiescent switch current, 3.6V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are 1.6µA maximum (3.6V supply) and 1.5µA maximum (5.5V supply).

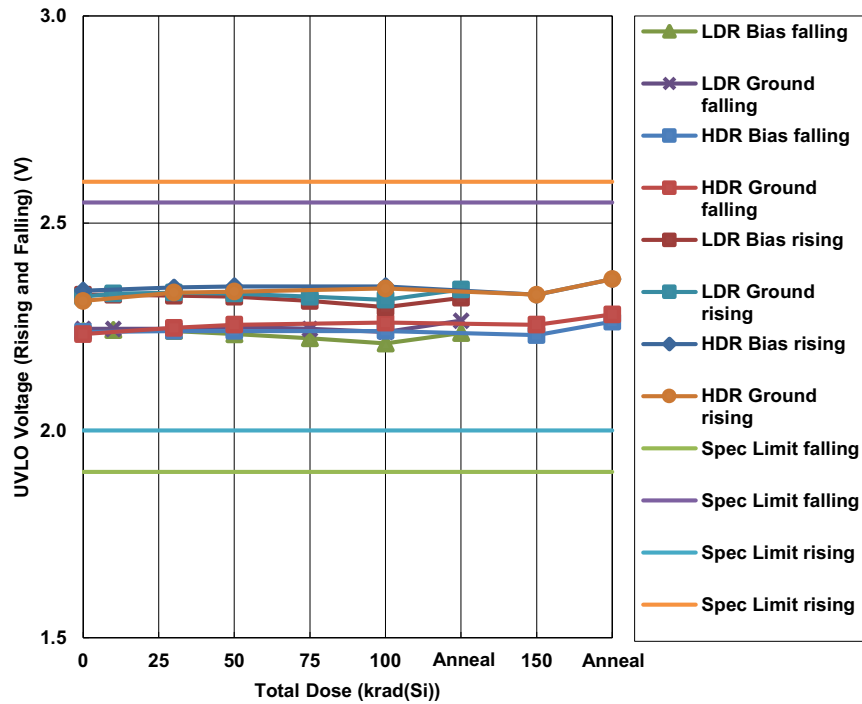


Figure 10. ISL70062SEH Undervoltage Lockout (UVLO) rising and falling threshold voltage as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are 1.9V to 2.55V (falling) and 2.0V to 2.6V (rising).

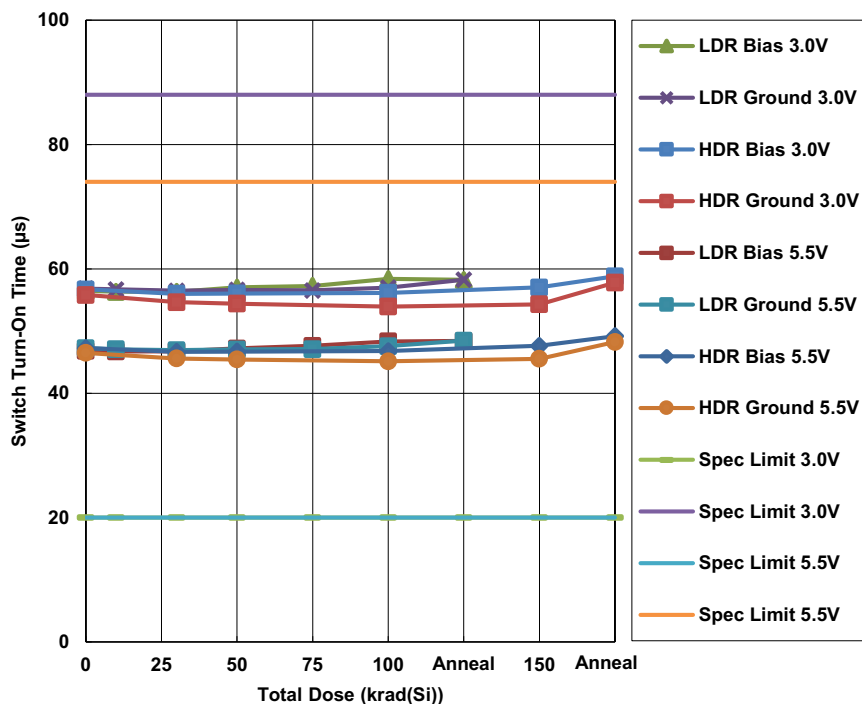


Figure 11. ISL70062SEH switch turn-on time, 3.0V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are 20µs to 88µs (3.0V supply) and 20µs to 74µs (5.5V supply).



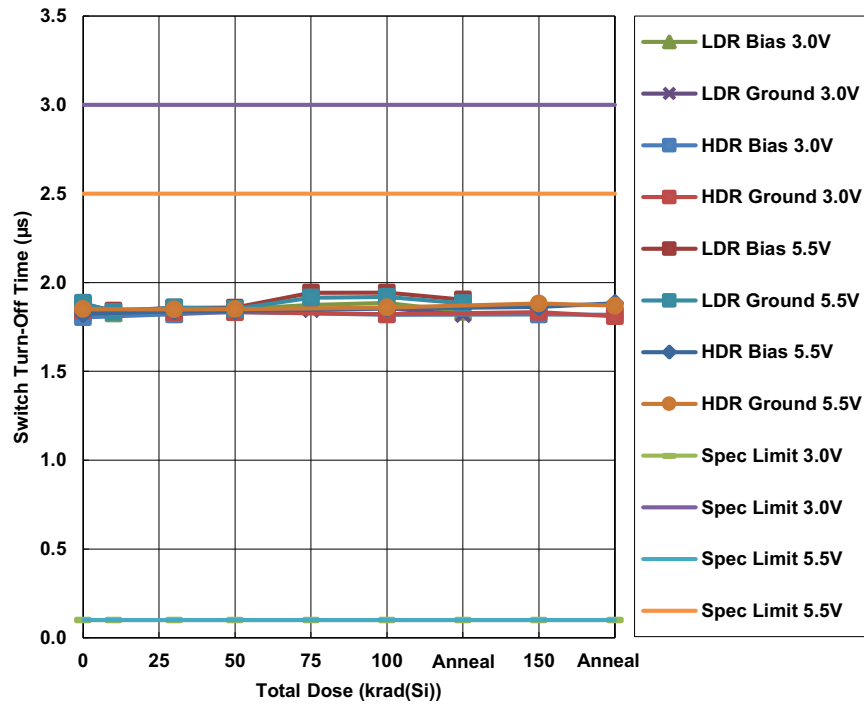


Figure 12. ISL70062SEH switch turn-off time, 3.0V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are 0.1µs to 3.0µs (3.0V supply) and 0.1µs to 2.5µs (5.5V supply).

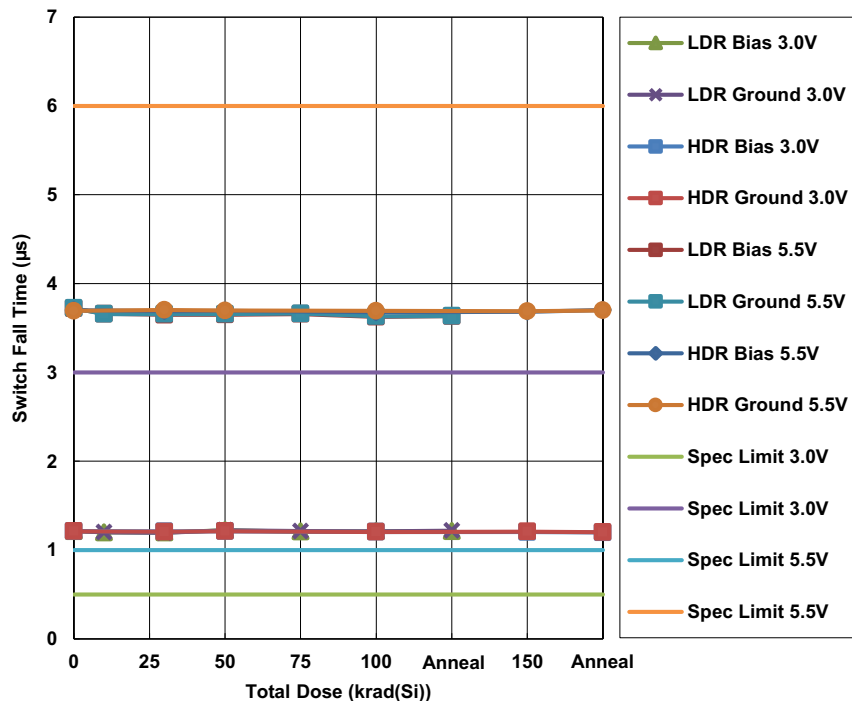


Figure 13. ISL70062SEH switch fall time, 3.0V and 5.5V supply voltage, as a function of total dose irradiation at LDR and HDR for the biased and unbiased cases. The irradiations were followed by a high temperature biased anneal at 100°C for 168 hours. The LDR was 0.01rad(Si)/s and the HDR was 72rad(Si)/s. Sample sizes are given in [Table 1](#). The post-irradiation SMD limits are 0.5µs to 3.0µs (3.0V supply) and 1.0µs to 6.0µs maximum (5.5V supply).

## 2.3 Discussion and Conclusion

This document reports the results of total dose characterization testing of the ISL70062SEH and ISL73062SEH NMOS load switches. Samples were tested at LDR and HDR under biased and unbiased conditions, as outlined in MIL-STD-883 Test Method 1019, to a total dose of 100krad(Si) at LDR and 150krad(Si) at HDR. All irradiations were followed by a 100°C biased high temperature anneal for 168 hours.

All samples showed good stability over irradiation and anneal, with no observed LDR sensitivity (or HDR sensitivity, for that matter). No differences between biased and unbiased irradiation were noted, and the part is not considered bias sensitive. A detailed discussion of the TID response of the plotted parameters is omitted as a quick inspection of the figures shows that there was very little change. For that same reason we elected to plot the 3.0V/3.6V and 5.5V supply cases on the same set of axes, as there was little difference between the two.

## 3. Appendix

**Table 2. Reported Parameters with Corresponding SMD Post-Irradiation Limits**

Fig.	Parameter	Low Limit	High Limit	Units	Notes
3	Switch ON-Resistance	20	30	mΩ	3.0V supply
		11	21	mΩ	5.5V supply; V <sub>SWI</sub> = 1.0V
4	OFF Switch Current	-	0.3	μA	3.6V supply
		-	0.5	μA	5.5V supply
5	Switch Output Rise Time	800	3000	μs	3.0V supply
		800	3500	μs	5.5V supply
6	Reverse Voltage Threshold, Enter	10	65	mV	3.0V supply
		10	65	mV	5.5V supply
7	Reverse Voltage Threshold, Exit	-12	0	mV	3.0V supply
		-12	0	mV	5.5V supply
8	Reverse Current Response Time	-	6.5	μs	3.0V supply
		-	5.0	μs	5.5V supply
9	Quiescent Switch Current	-	1.6	μA	3.6V supply
		-	1.5	μA	5.5V supply
10	UVLO Threshold	1.9	2.55	V	Falling threshold
		2.0	2.6	V	Rising threshold
11	Switch Turn-On Time	20	88	μs	3.0V supply
		20	74	μs	5.5V supply
12	Switch Turn-Off Time	0.1	3.0	μs	3.0V supply
		0.1	2.5	μs	5.5V supply
13	Switch Fall Time	0.5	3.0	μs	3.0V supply
		1.0	6.0	μs	5.5V supply

## 4. Revision History

Rev.	Date	Description
1.00	Dec.2.19	Initial release

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(Rev.1.0 Mar 2020)

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