
HS-303AEHTotal Dose Test Report

Introduction

This report shows the results of a Low Dose Rate (LDR) total dose test of the [HS-303AEH](#) dual SPDT analog switch. The data for this report was obtained from wafer-by-wafer total dose acceptance testing of the part. Samples were irradiated at LDR (<0.01rad(Si)/s) under bias and with all pins grounded.

The HS-303AEH is acceptance-tested on a wafer-by-wafer basis to 300krad(Si) at High Dose Rate (HDR) (50-300rad(Si)/s) and to 50krad(Si) at LDR (0.01rad(Si)/s), ensuring product hardness to the specified level for both dose rates.

The part effectively met the SMD post-radiation specification limits at all downpoints. No significant differences in the total dose response were noted for any parameters between the biased and grounded irradiation or the two switches.

Product Description

The HS-303AEH dual SPDT analog switch is fabricated using dielectrically isolated BiCMOS technology for latch-up free operation. The parts offer low-resistance switching performance for analog voltages up to the supply rails. Switch ON-resistance is low and stays reasonably constant over operating voltage, switch current, and total dose irradiation. The ON-resistance is typically 50Ω pre-rad and 60Ω post 300krad(Si) at HDR. The device provides break-before-make switching with controlled, specified break-before-make delay. The HS-303ARH should be operated with nominal ±15V supplies.

Specifications for radiation hardened MIL-PRF-38535 (QML) devices are controlled by the Defense Logistics Agency, Land and Maritime (DLA), Columbus, OH. Detailed electrical specifications for the HS-303AEH are contained in SMD [5962-95813](#).

Related Literature

For a full list of related documents, visit our website:

- [HS-303AEH](#) device page

1. Test Description

1.1 Irradiation Facilities

LDR irradiation was performed at 0.01rad(Si)/s using the Renesas Palm Bay N40 panoramic irradiator.

1.2 Test Fixturing

Biased irradiation was performed in accordance with the internally specified irradiation diagram. Grounded irradiation was performed with all pins hardwired to ground.

1.3 Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using the production Automated Test Equipment (ATE) with data logging at each downpoint. Downpoint electrical testing was performed at room temperature.

1.4 Experimental Matrix

The experimental matrix consisted of 34 samples irradiated at LDR under bias and 34 samples irradiated at LDR with all pins grounded. The irradiations were carried out as part of the wafer-by-wafer Radiation Lot Acceptance Testing (RLAT) of fabrication lot DWP3TEH. Samples were assembled in hermetic 14 Ld flatpacks, processed through the standard burn-in cycle, and screened to the room temperature ATE limits prior to the acceptance test.

1.5 Downpoints

Downpoints were 0, 50, and 100krad(Si).

2. Results

2.1 Attributes Data

Table 1. HS-303AEH LDR Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint (krad(Si))	Pass	Fail
0.01	Biased	34	0	34	0
			50	34	0
			100	34	0
0.01	Grounded	34	0	34	0
			50	34	0
			100	34	0

Note: 'Pass' indicates a device that passes all post-radiation SMD limits.

2.2 Variables Data

The plots in [Figures 1](#) through [15](#) show data at all three downpoints for key parameters. The plots show the response to total dose irradiation at LDR for the biased (per SMD) and unbiased (all pins grounded) cases. We chose to plot the average for these parameters due to the relatively large sample sizes, and showed minimum and maximum error bars as well. In most cases, the figures plot the average of two switches or of two address inputs. No differences in total dose response were noted between biased and grounded irradiation for any parameter, and no channel sensitivity was observed.

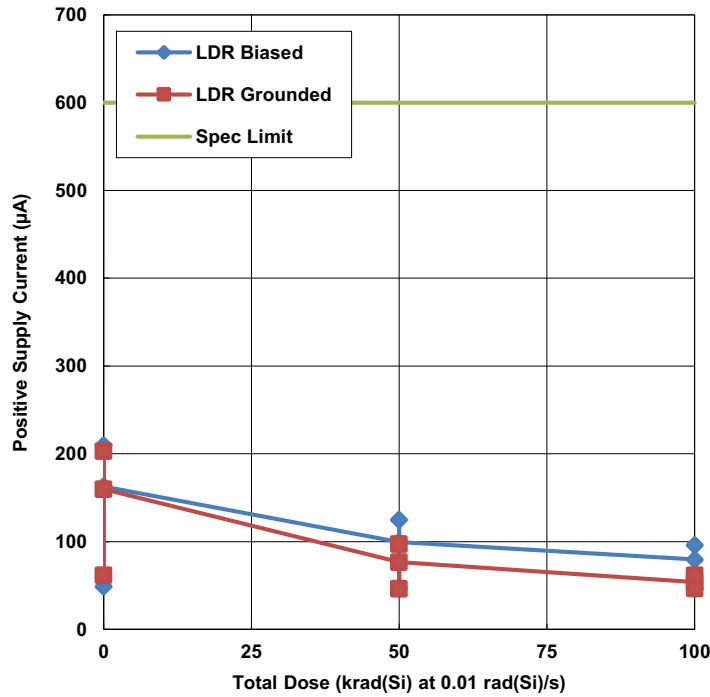


Figure 1. HS-303AEH positive power supply current as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limit is 600µA maximum.

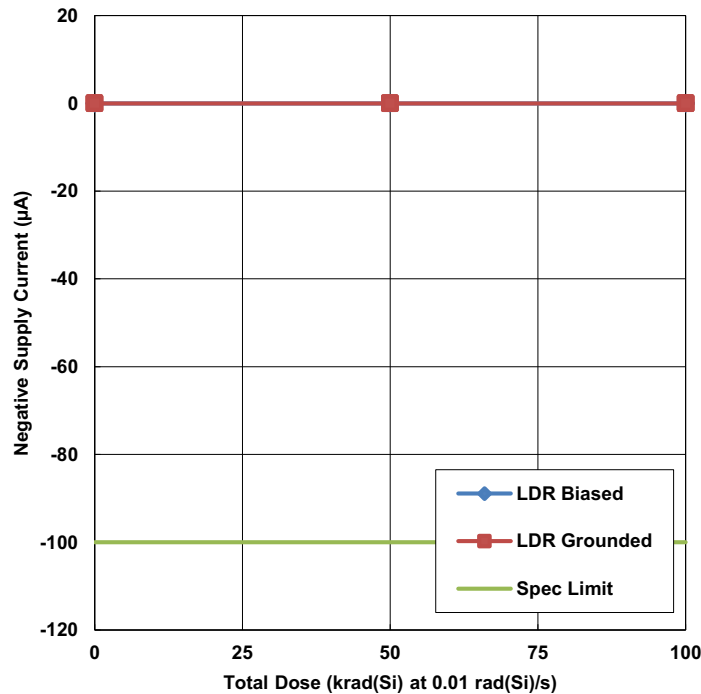


Figure 2. HS-303AEH negative power supply current as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limit is -100µA minimum.

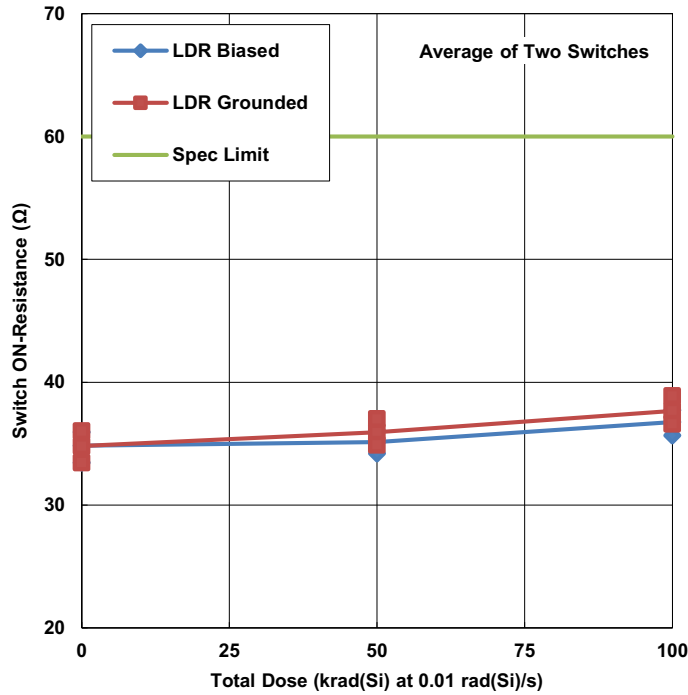


Figure 3. HS-303AEH switch ON-resistance, drain voltage 10V, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limit is 60Ω maximum.

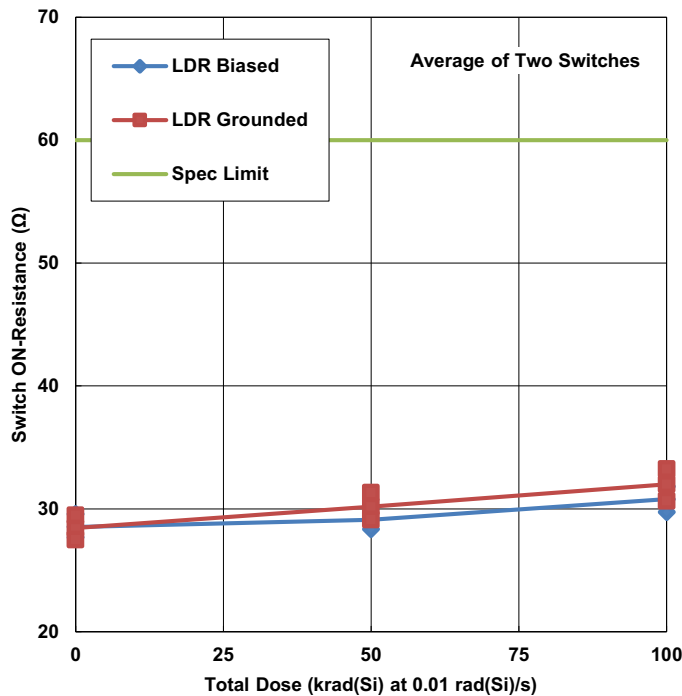


Figure 4. HS-303AEH switch ON-resistance, drain voltage -10V, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limit is 60Ω maximum.

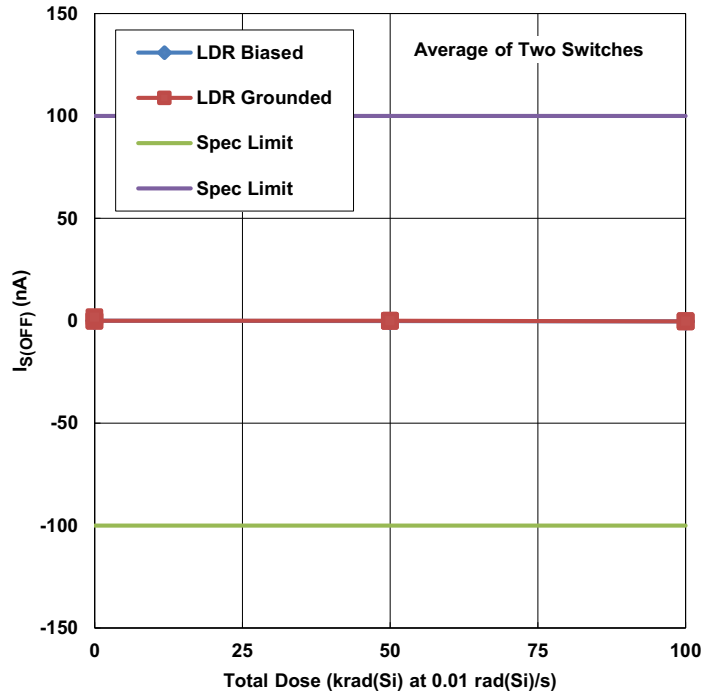


Figure 5. HS-303AEH leakage current into the source terminal of an OFF switch, source voltage +14V and drain voltage -14V, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limits are -100nA to 100nA.

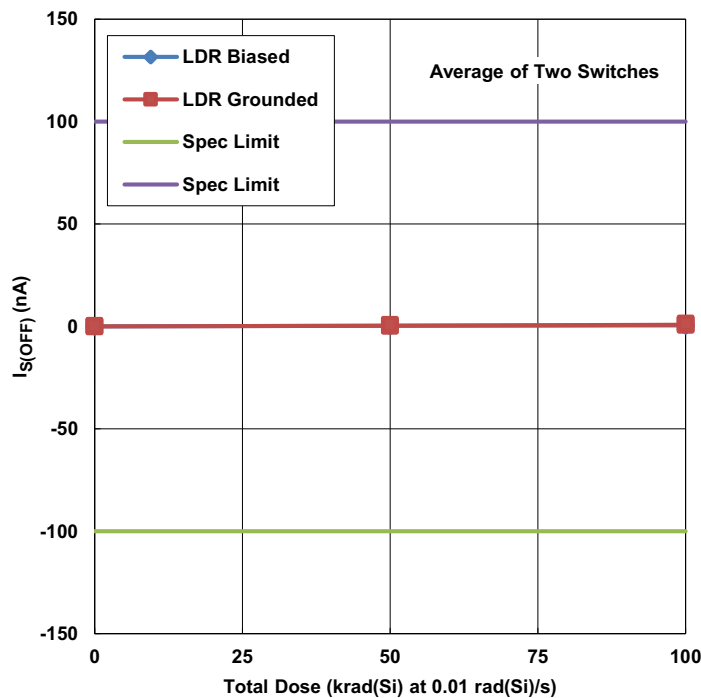


Figure 6. HS-303AEH leakage current into the source terminal of an OFF switch, source voltage -14V and drain voltage +14V, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limits are -100nA to 100nA.

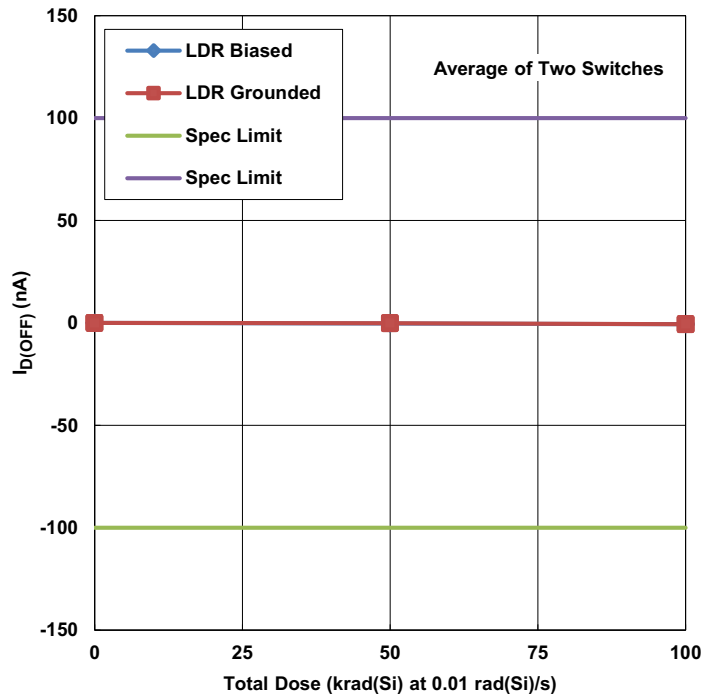


Figure 7. HS-303AEH leakage current into the drain terminal of an OFF switch, source voltage +14V and drain voltage -14V, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limits are -100nA to 100nA.

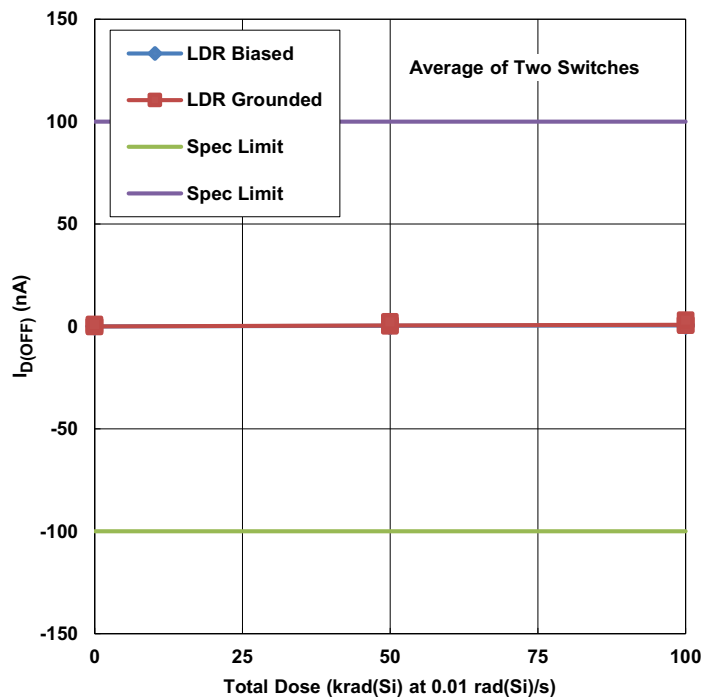


Figure 8. HS-303AEH leakage current into the drain terminal of an OFF switch, source voltage -14V and drain voltage +14V, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limits are -100nA to 100nA.

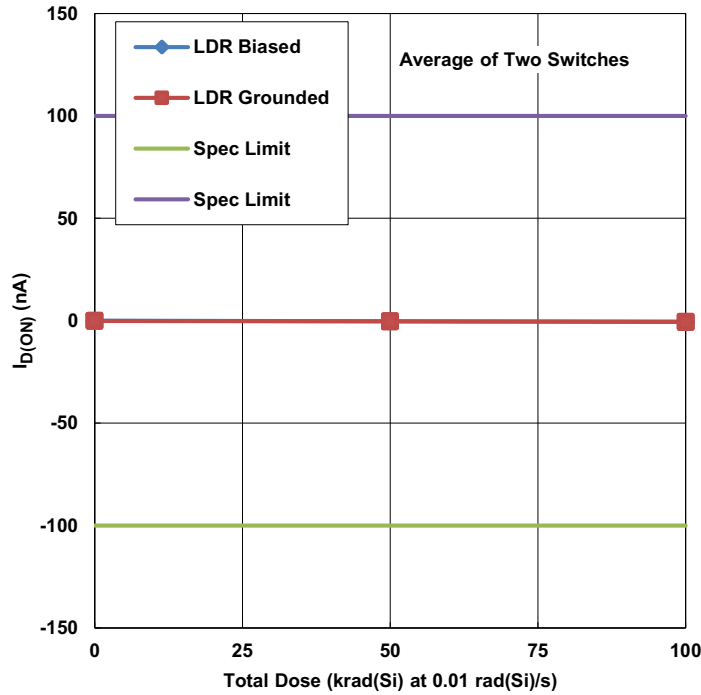


Figure 9. HS-303AEH leakage current into the drain and source terminals of an ON switch, source and drain tied together at +14V, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The SMD limits are -100nA to 100nA.

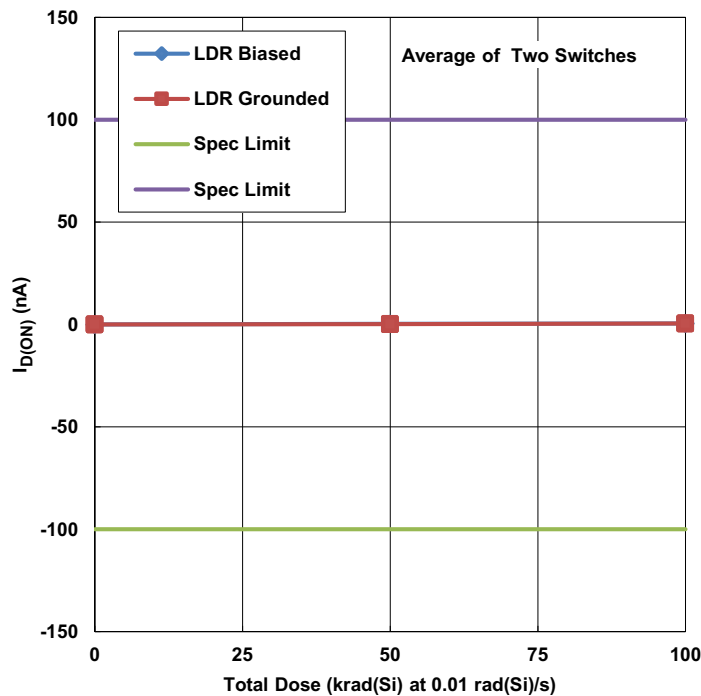


Figure 10. HS-303AEH leakage current into the drain and source terminals of an ON switch, source and drain tied together at -14V, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The SMD limits are -100nA to 100nA.

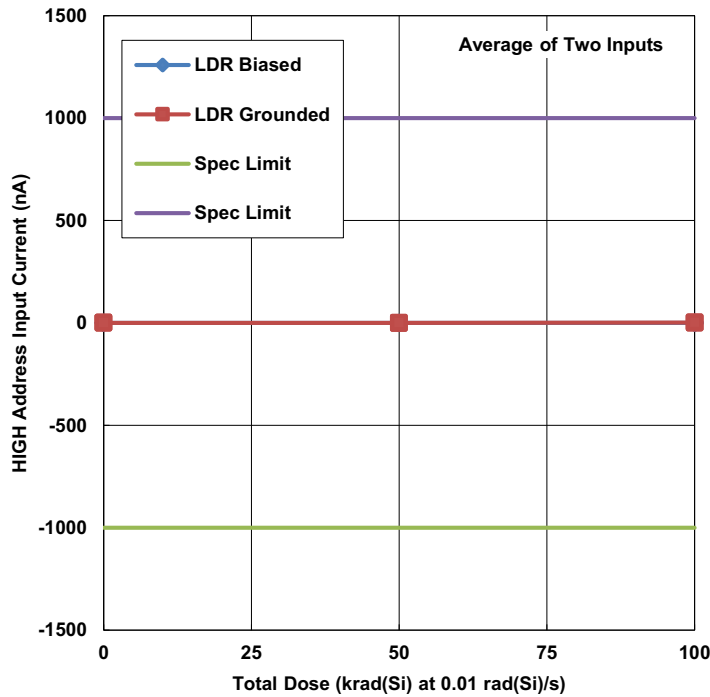


Figure 11. HS-303AEH HIGH level address input current, average of two address inputs, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limits are -1000nA to 1000nA.

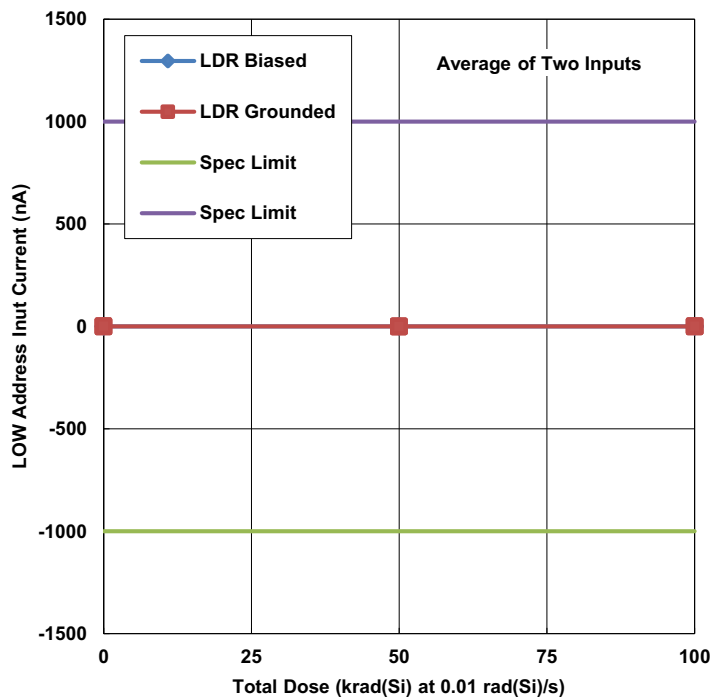


Figure 12. HS-303AEH LOW level address input current, average of two address inputs, as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limits are -1000nA to 1000nA.

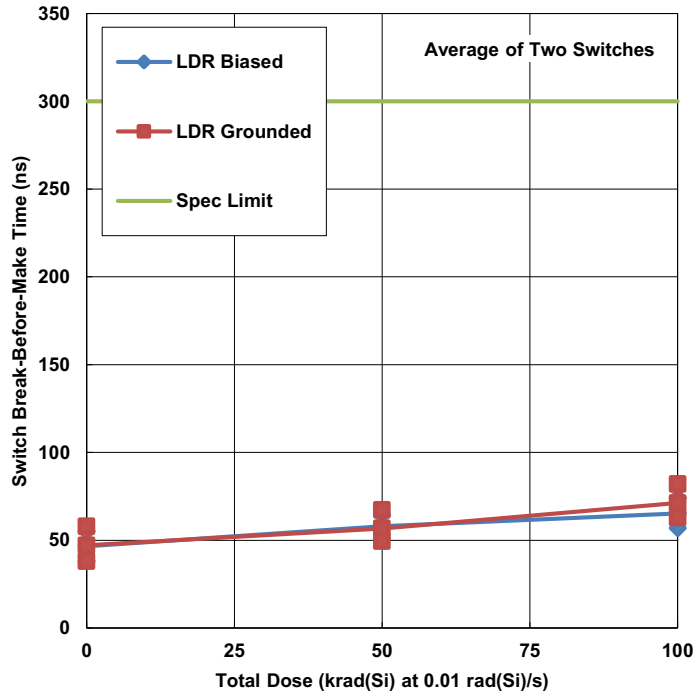


Figure 13. HS-303AEH switch break-before-make time as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limit is 300ns maximum.

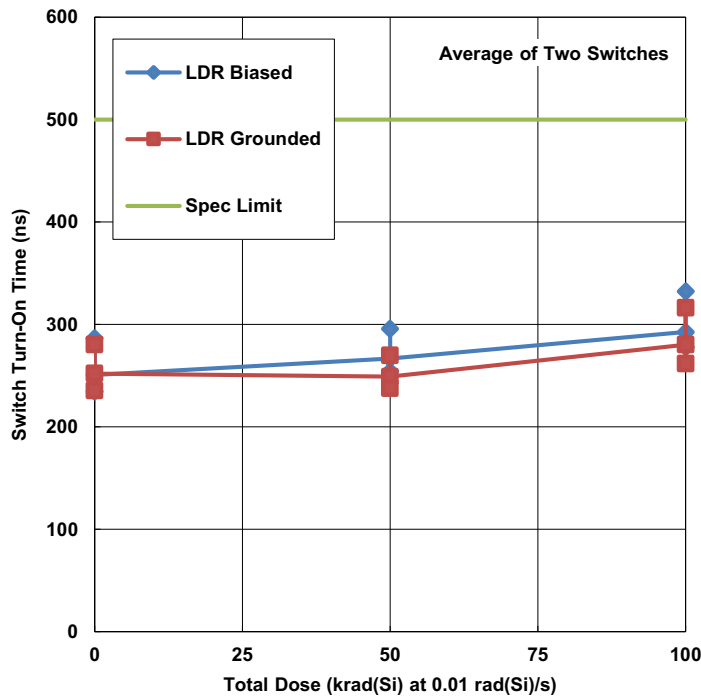


Figure 14. HS-303AEH switch turn-on time as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limit is 500ns maximum.

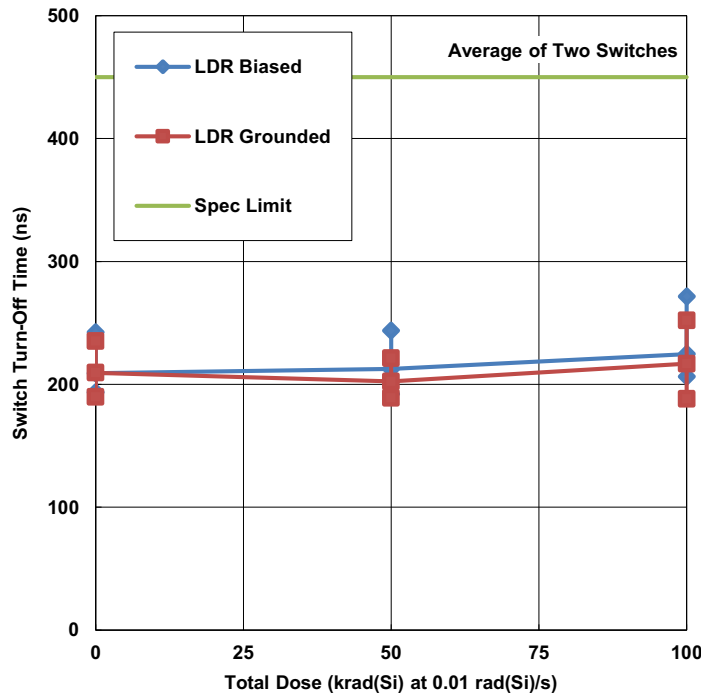


Figure 15. HS-303AEH switch turn-off time as a function of total dose irradiation for the biased and unbiased cases. The dose rate was 0.01rad(Si)/s and the sample size was 34 for each cell. The post-radiation SMD limit is 450ns maximum.

3. Discussion and conclusion

The report show the results of a Low Dose Rate (LDR) total dose test of the HS-303AEH dual SPDT analog switch. The data for this report was obtained from wafer-by-wafer acceptance testing of the part. Samples were irradiated at 0.01rad(Si)/s under bias and with all pins grounded. All parameters remained within the SMD and ATE post-radiation limits at all downpoints. The results have been summarized in a [Table 1 on page 2](#) followed by a limited number of curves of interest ([Figures 1](#) through [15](#)).

The part is acceptance tested on a wafer-by-wafer basis to 300krad(Si) at High Dose Rate (HDR) (50-300rad(Si)/s) and to 50krad(Si) at LDR (0.01rad(Si)/s), ensuring hardness to the specified level for both dose rates. No significant differences in LDR response were noted between biased and grounded irradiation for any parameters. Additionally, no channel-to-channel differences were noted, either in the pre-radiation data or in the total dose response of the parts.

4. Appendix

Table 2. Reported Parameters and Their Post-Radiation SMD Limits

Figure	Parameter	Low Limit	High Limit	Units	Notes
1	Positive Power Supply Current	-	600	μA	
2	Negative Power Supply Current	-100	-	μA	
3	ON-Resistance, +10V	-	60	Ω	Average of 2 switches
4	ON-Resistance, -10V	-	60	Ω	Average of 2 switches
5	Source OFF Leakage, ±14V	-100	100	nA	Average of 2 switches
6	Source OFF Leakage, ±14V	-100	100	nA	Average of 2 switches
7	Drain OFF leakage, ±14V	-100	100	nA	Average of 2 switches
8	Drain OFF leakage, ±14V	-100	100	nA	Average of 2 switches
9	Drain and Source ON Leakage, +14V	-100	100	nA	Average of 2 switches
10	Drain and Source ON Leakage, -14V	-100	100	nA	Average of 2 switches
11	High Level Address Input Current	-1000	1000	nA	Average of 2 inputs
12	Low Level Address Input Current	-1000	1000	nA	Average of 2 inputs
13	Switch Break-Before-Make Time	-	300	ns	Average of 2 switches
14	Switch Turn-On Time	-	500	ns	Average of 2 switches
15	Switch Turn-Off Time	-	450	ns	Average of 2 switches

5. Revision History

Rev.	Date	Description
0.00	Apr.8.19	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.