ISL72814SEH, ISL73814SEH

Total Dose Test Report

Introduction

This report documents the results of low and high dose rate total dose testing of the ISL72814SEH and ISL73814SEH 16-channel current drivers. The results also include post-irradiation high temperature biased annealing. The tests were conducted to provide an assessment of the total dose hardness of the parts and to determine any dose rate, bias or anneal sensitivity. Parts were irradiated under bias and with all pins grounded at Low Dose Rate (LDR) to 100krad(Si) and at High Dose Rate (HDR) to 150krad(Si). Both irradiations were followed by high temperature biased anneal. The ISL72814SEH is rated at 100krad(Si) at HDR (50 - 300rad(Si)/s) and at 75krad(Si) at LDR (0.01rad(Si)/s) and is acceptance tested on a wafer-by-wafer basis to the SMD limits. The ISL73814SEH is rated at 75krad(Si) at LDR (0.01rad(Si)/s) and is acceptance tested on a wafer-by-wafer basis to the SMD limits.

Part Description

The ISL72814SEH and ISL73814SEH (ISL7x814SEH) are radiation hardened, high-voltage, high-current, driver circuit ICs fabricated using the Renesas proprietary PR40 Silicon-On-Insulator (SOI) process technology to mitigate single event effects. The devices integrate 16 driver channels that feature a high-voltage (42V), high-current (700mA) open-emitter PNP output stage.

To further reduce solution size, the ISL7x814SEH integrates a 4-bit, 16-channel decoder with Enable. This conveniently allows you to select 1 of 16 available driver channels or disable all channels. The inputs to the decoder are TTL and CMOS compatible to allow an easy interface to FPGAs and microprocessors.

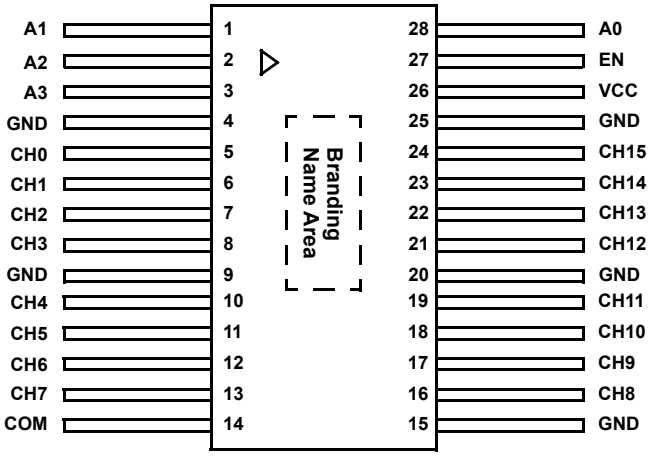
The ISL7x814SEH devices operate across the military temperature range from -55°C to +125°C and are available in a 28 Ld hermetically sealed Ceramic Dual Flatpack (CDFP) package or die.

Related Literature

For a full list of related documents, visit our website:

- ISL72814SEH, ISL73814SEH device pages

28 Ld CDFP
Top View



Note: The ESD triangular mark is indicative of Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

Figure 1. ISL7x814SEH Pinout Configuration

Table 1. ISL7x814SEH Pin Descriptions

Pin Number	Pin Name	Description
1-3, 28	Ax	Address lines for the decoder.
4, 9, 15, 20, 25	GND	Supply and output driver ground. Connect this pin to the PCB ground plane.
5-8, 10-13, 16-19, 21-24	CHx	Channels 0 through 15 open emitter PNP outputs.
14	COM	ESD Clamp rail. It can be used to terminate inductances connected to the CHx pins and should be tied to the highest relay coil supply rail in the system. When not switching inductive loads, tie it to the supply rail of the CHx channel with the highest voltage.
26	VCC	Bias supply for the decoder and the level shift circuit. Connect to a voltage between 3V to 13.2V.
27	EN	Active high enable input to the decoder.
-	Package lid	Internally connected to GND (Pin 15).

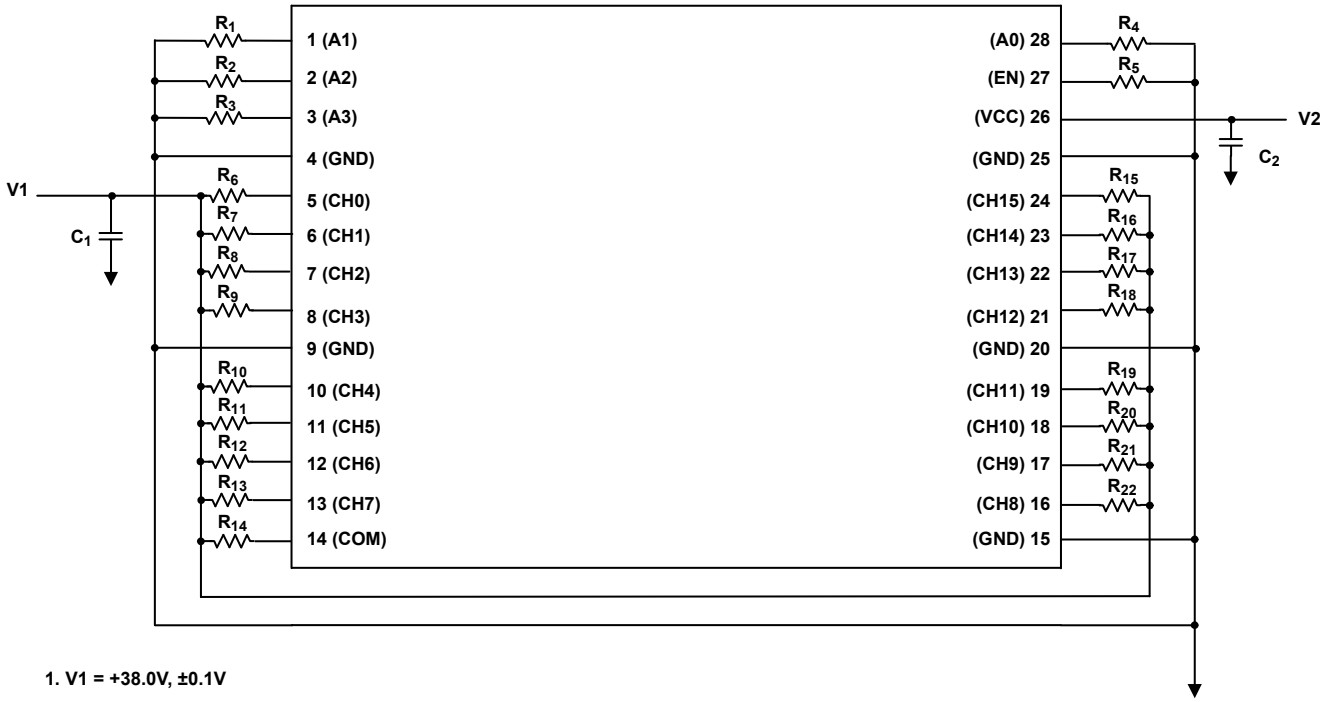
1. Test Description

1.1 Irradiation Facilities

High Dose Rate (HDR) testing was performed at 187.16rad(Si)/s using a Gammacell 220 industry standard irradiator located in the Renesas facility in Palm Bay, Florida. Low Dose Rate (LDR) testing was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic irradiator. The LDR irradiator uses PbAl spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation. Half of the samples were biased and half had all pins grounded during irradiation. Samples from both dose rates underwent post-irradiation anneal at +100°C for 168 hours in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configuration used for biased irradiation at both dose rates and the biased anneal. Note that the part is biased at V_{CC} = 13.2V with the channels biased at 38V.



1. V1 = +38.0V, ±0.1V
2. V2 = +13.2V, ±0.1V
3. R1 - R5 = 1kΩ, ±5%, 1/4 Watt (per socket)
4. R6 - R22 = 38k, ±5%, 1/4 Watt
5. Socket is 28 Ld Pin Flatpack (Sensata 628-0282315)

Figure 2. ISL7x814SEH TID Bias Schematic

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator using production Automated Test Equipment (ATE) with data-logging at each downpoint.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 10 samples irradiated at LDR under bias and 10 samples irradiated at LDR with all pins grounded; and 6 samples irradiated at HDR under bias and 6 samples irradiated at HDR with all pins grounded. All 20 LDR samples underwent biased anneal samples. Due to board size limitations, only six samples from the HDR matrix could be annealed at a time, so four biased and two unbiased samples were randomly chosen to include in the biased anneal. Three control units were used for both types of irradiation.

The ISL7x814SEH samples were from wafer lots XCT0D and XCP6D. All samples were packaged in the 28 Ld ceramic flatpack package (package code K28.A). Samples were processed through the standard burn-in cycle before irradiation.

1.5 Downpoints

Downpoints for the LDR tests were 0, 10, 30, 50, 75, and 100krad(Si). Downpoints for the HDR tests were 0, 30, 50, 100, and 150krad(Si). Both exposures were followed by a 168 hour +100°C anneal under bias.

2. Test Results

2.1 Attributes Data

Total dose testing of the ISL7x814SEH is complete. All tested parameters passed the SMD limits. Table 2 summarizes the results.

Table 2. ISL7x814SEH Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass (Note 1)	Fail
0.01	Biased (Figure 2)	10	Pre-irradiation	10	0-
			10krad(Si)	10	0
			30krad(Si)	10	0
			50krad(Si)	10	0
			75krad(Si)	10	0
			100krad(Si)	10	0
			Anneal	10	0
0.01	Grounded	10	Pre-irradiation	10	
			10krad(Si)	10	0
			30krad(Si)	10	0
			50krad(Si)	10	0
			75krad(Si)	10	0
			100krad(Si)	10	0
			Anneal	10	0
187.16	Biased (Figure 2)	6	Pre-irradiation	6	
			30krad(Si)	6	0
			50krad(Si)	6	0
			100krad(Si)	6	0
			150krad(Si)	6	0
			Anneal	4	0
187.16	Grounded	6	Pre-irradiation	6	
			30krad(Si)	6	0
			50krad(Si)	6	0
			100krad(Si)	6	0
			150krad(Si)	6	0
			Anneal	2	0

Note:
1. ‘Pass’ indicates a sample that passes all SMD limits.

2.2 Key Parameter Listing

Table 3 lists the SMD parameters that are considered indicative of part performance. These parameters are plotted in Figures 3 through 20. All limits are taken from the ISL7x814SEH SMD; see the SMD 59102-18221 for further detail on test conditions.

Table 3. ISL7x814SEH SMD Total Dose Parameters (T_A = +25°C)

Figure	Parameter	Symbol	Limit (Low)	Limit (High)	Unit
3	Supply current	I_{CC}	4.5	8.5	mA
4	Quiescent supply current	I_{CCQ}	350	800	µA
5	Single channel leakage current	I_{CHLK}	-25	25	nA
6	All channels + COM leakage current	$I_{TOTCHLK}$	-30	100	nA
7	Output channel saturation voltage (I_{CHx} = 700mA)	$V_{CH(SAT)}$	0.85	1.5	V
8	Output channel saturation voltage (I_{CHx} = 600mA)		0.8	1.4	
9	Output channel saturation voltage (I_{CHx} = 500mA)		0.65	1.35	
10	Output channel saturation voltage (I_{CHx} = 350mA)		0.6	1.3	
11	Output channel saturation voltage (I_{CHx} = 200mA)		0.5	1.2	
12	COM to CHx Inductive kickback clamp diode forward voltage (I_{CHx} = 200mA)	V_F	0.85	1.3	V
13	COM to CHx Inductive kickback clamp diode forward voltage (I_{CHx} = 700mA)		1.0	2.25	
14	COM to CHx inductive kickback clamp diode leakage current	I_R	-15	15	nA
15	High logic level voltage	V_{IH}	2	-	V
16	Low logic level voltage	V_{IL}	-	0.8	V
17	Input high current	I_{IH}	-250	250	nA
18	Input low current	I_{IL}	-250	250	nA
19	Enable Turn-On Time	t_{EN}	-	5	µs
20	Disable Turn-Off Time	t_{DIS}	-	15	µs

2.3 Key Parameter Variables Data

The plots in Figures 3 through 20 illustrate the TID response of the SMD parameters outlined in Key Parameter Listing. The plots show the average tested values of the parameters as a function of total dose for each of the irradiation conditions, biased and grounded, at LDR and HDR. For example, the legend HDR_Bias indicates the average HDR response for biased parts. On the x-axis, along with the total dose, PA_L and PA_H represent the post-anneal LDR and HDR points, respectively. The plots also include error bars at each downpoint that represent the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible due to their values compared to the scale of the graph.

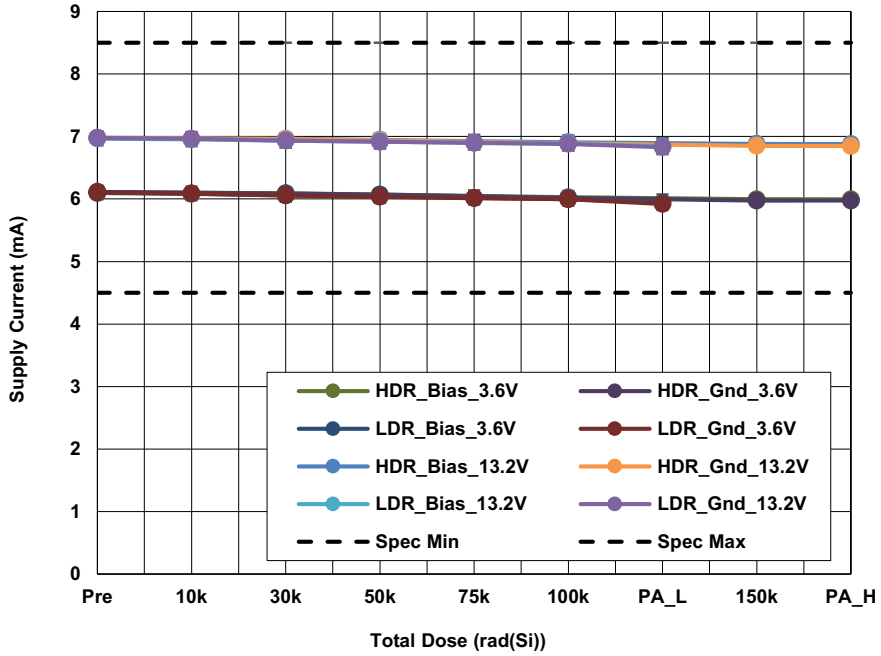


Figure 3. ISL7x814SEH supply current (I_{CC}) at V_{CC} = 3.6V and 13.2V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are 4.5mA minimum and 8.5mA maximum.

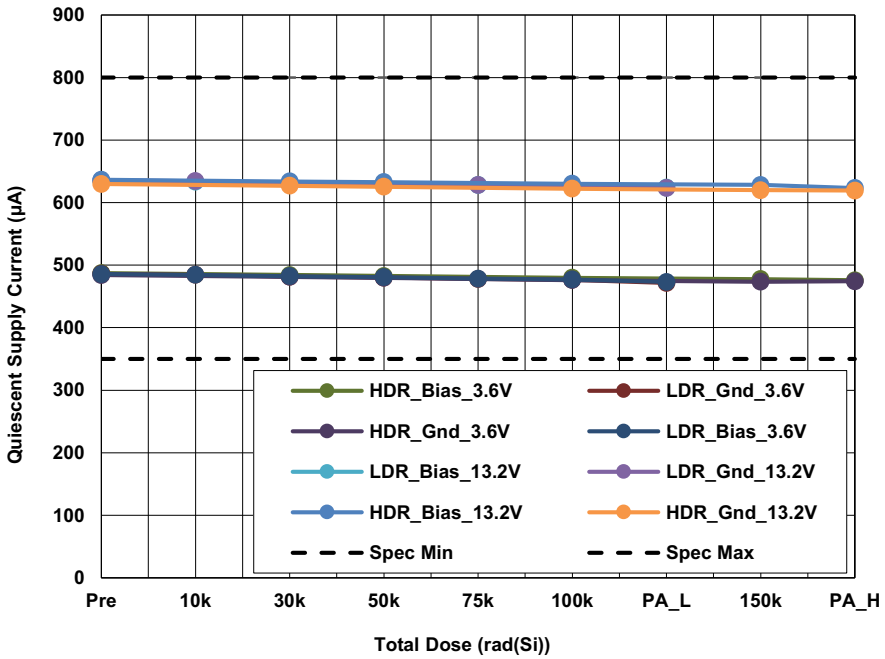


Figure 4. ISL7x814SEH quiescent supply current (I_{CCQ}) at V_{CC} = 3.6V and 13.2V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are 350µA minimum and 800µA maximum.

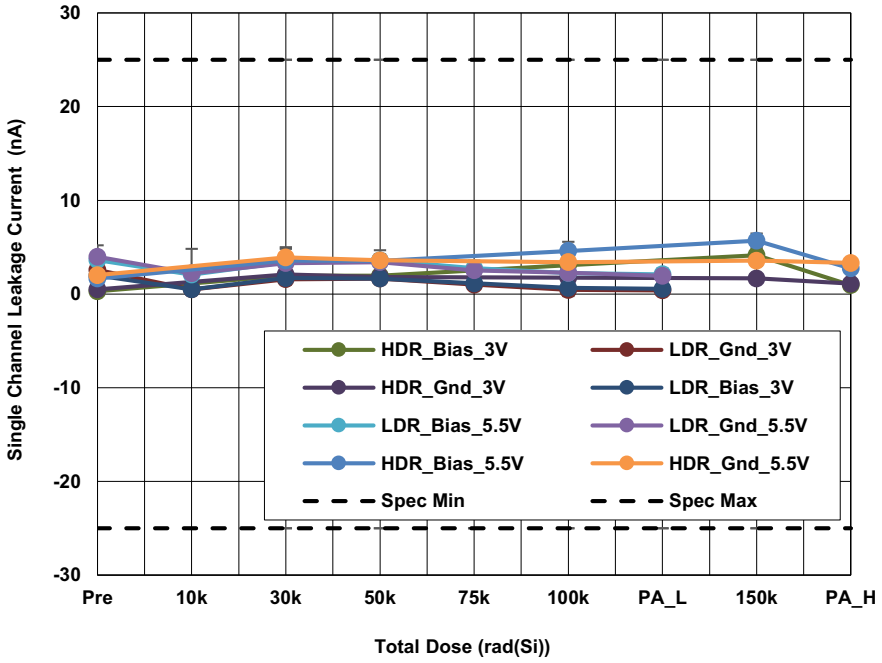


Figure 5. ISL7x814SEH single channel leakage current (I_{CHLK}) at V_{CC} = 3V and 5.5V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are -25nA minimum and 25nA maximum.

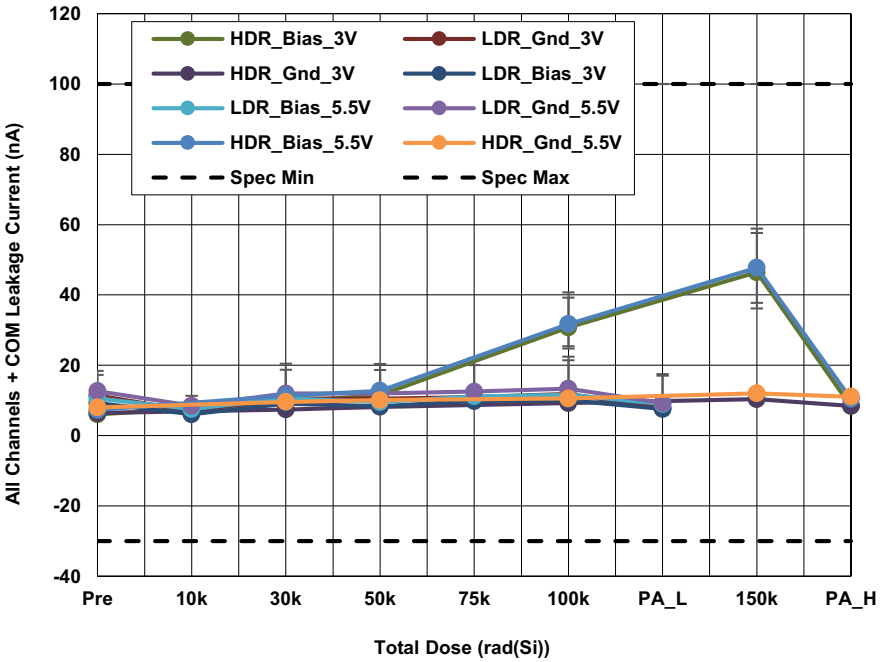


Figure 6. ISL7x814SEH all channels + COM leakage current ($I_{TOTCHLK}$) at V_{CC} = 3V and 5.5V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are -30nA minimum and 100nA maximum.

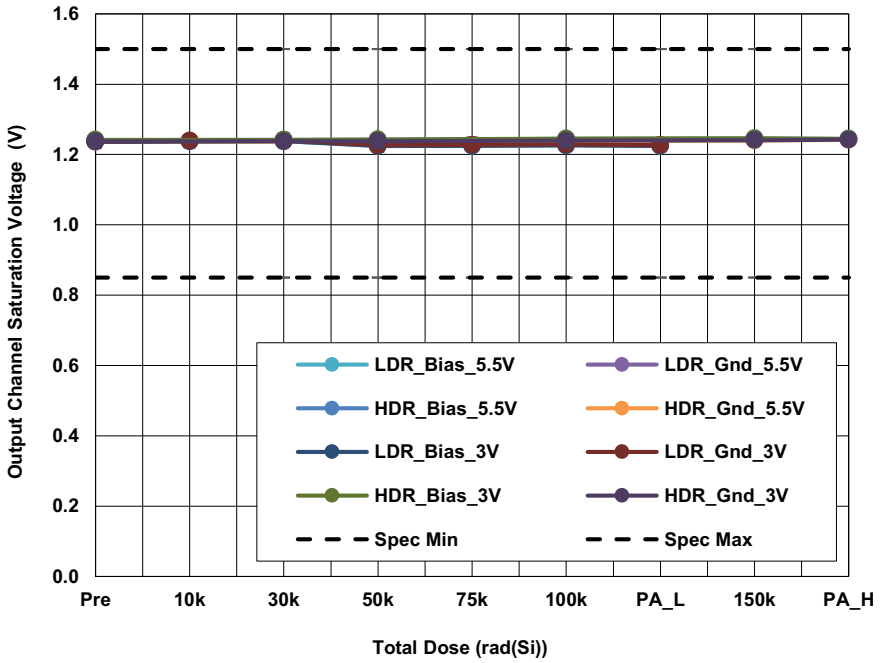


Figure 7. ISL7x814SEH output channel saturation voltage ($V_{CH(Sat)}$) at V_{CC} = 3V and 5.5V, with I_{CHx} = 700mA, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.85V minimum and 1.50V maximum.

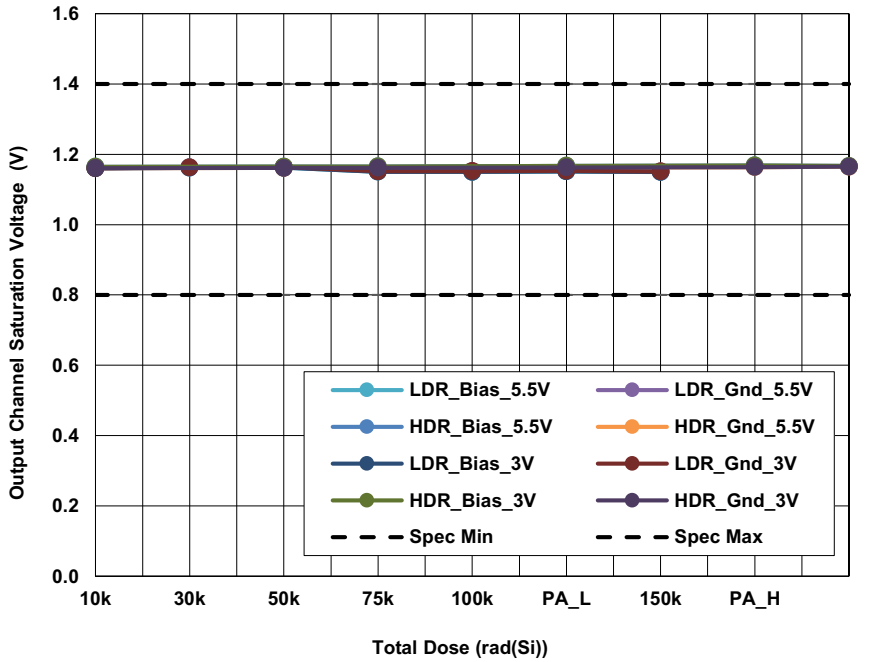


Figure 8. ISL7x814SEH output channel saturation voltage ($V_{CH(Sat)}$) at V_{CC} = 3V and 5.5V, with I_{CHx} = 600mA, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.80V minimum and 1.40V maximum.

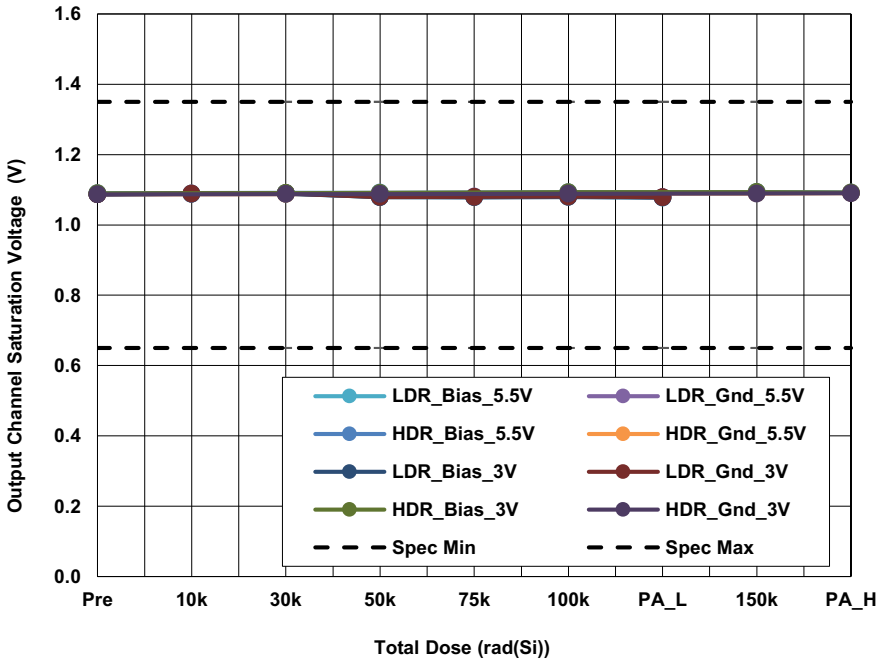


Figure 9. ISL7x814SEH output channel saturation voltage ($V_{CH(Sat)}$), at V_{CC} = 3V and 5.5V, with I_{CHx} = 500mA, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.65V minimum and 1.35V maximum.

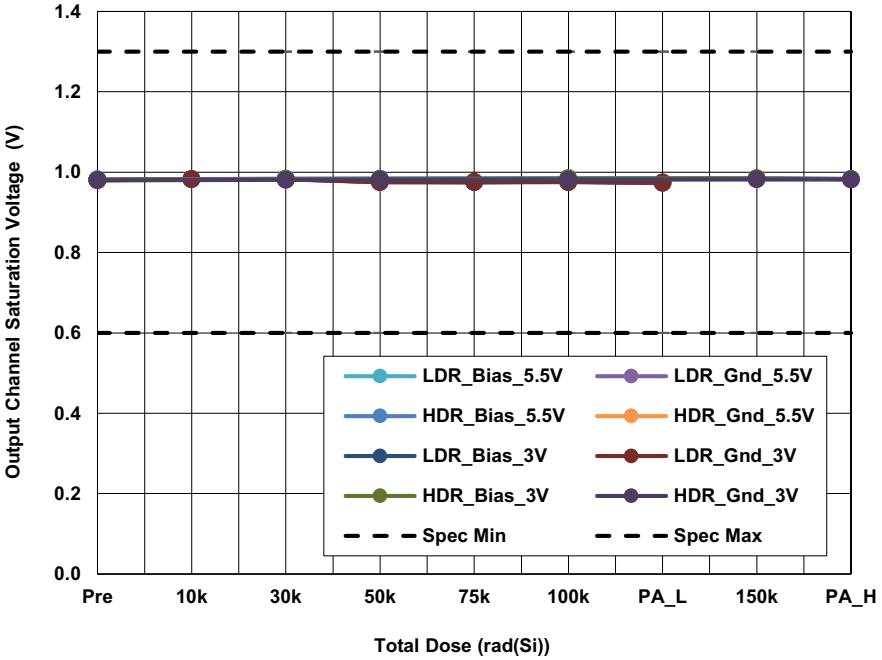


Figure 10. ISL7x814SEH output channel saturation voltage ($V_{CH(Sat)}$), at V_{CC} = 3V and 5.5V, with I_{CHx} = 350mA, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.60V minimum and 1.30V maximum.

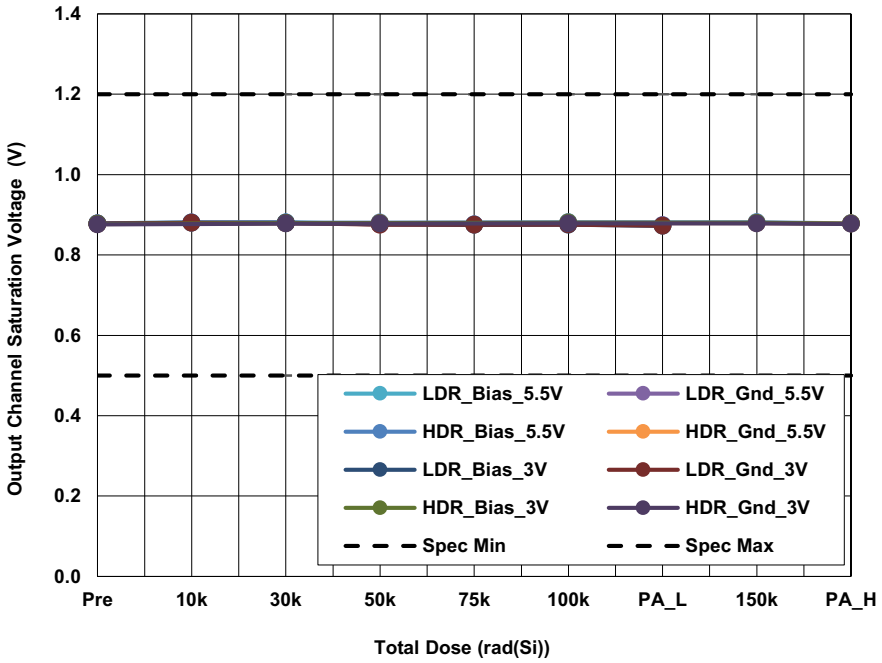


Figure 11. ISL7x814SEH output channel saturation voltage ($V_{CH(Sat)}$), at V_{CC} = 3V and 5.5V, with I_{CHx} = 200mA, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.50V minimum and 1.20V maximum.

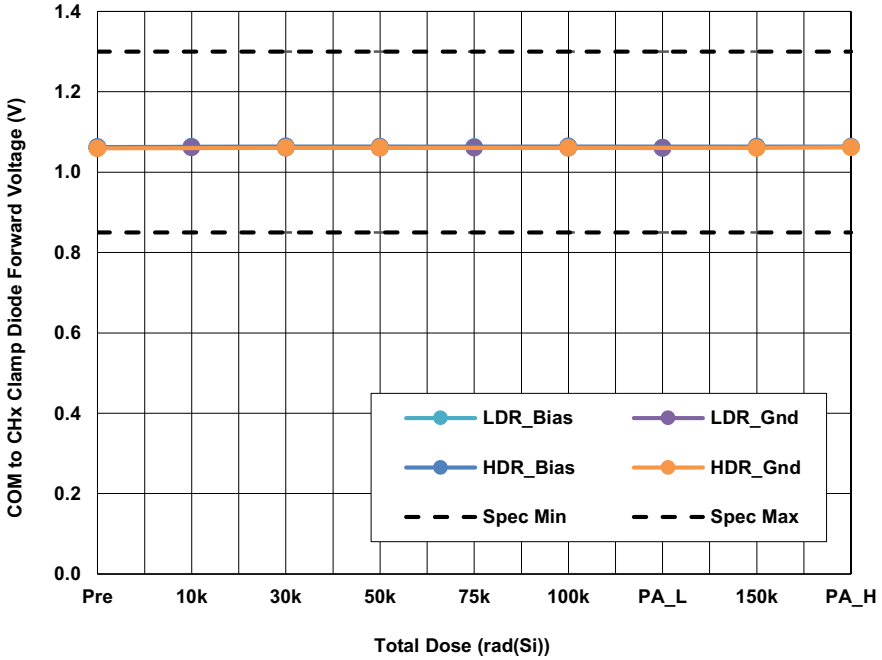


Figure 12. ISL7x814SEH COM to CHx clamp diode forward voltage (V_F), with I_{CHx} = 200mA, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.85V minimum and 1.30V maximum.

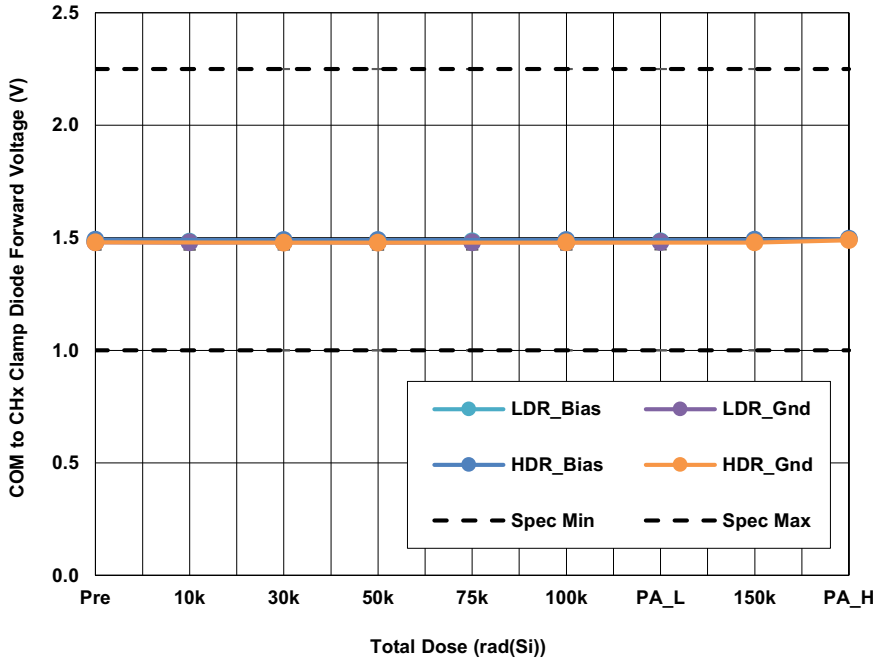


Figure 13. ISL7x814SEH COM to CHx clamp diode forward voltage (V_F) with I_{CHx} = 700mA, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.0V minimum and 2.25V maximum.

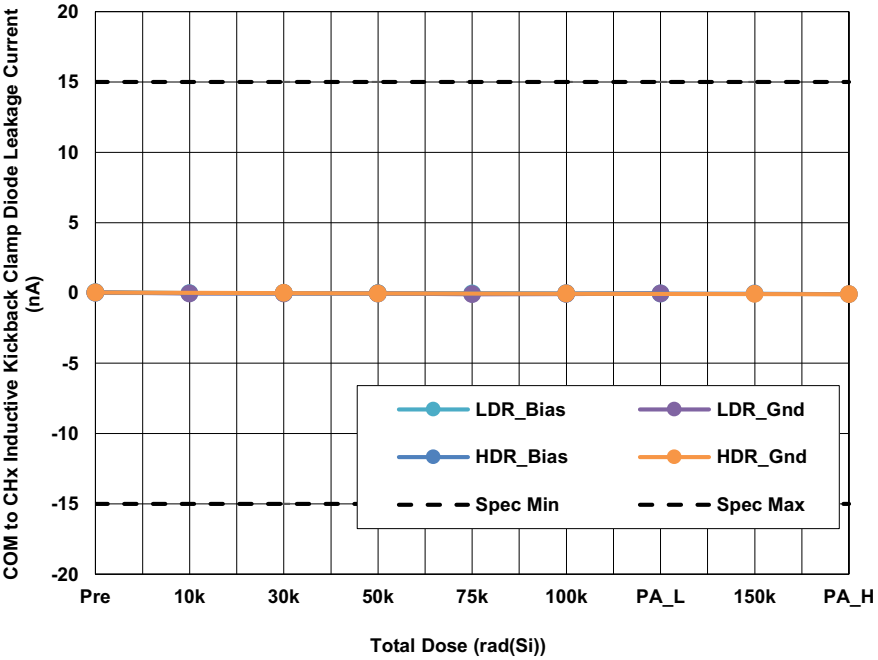


Figure 14. ISL7x814SEH COM to CHx inductive kickback clamp diode leakage current (I_R) as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are -15nA minimum and 15nA maximum.

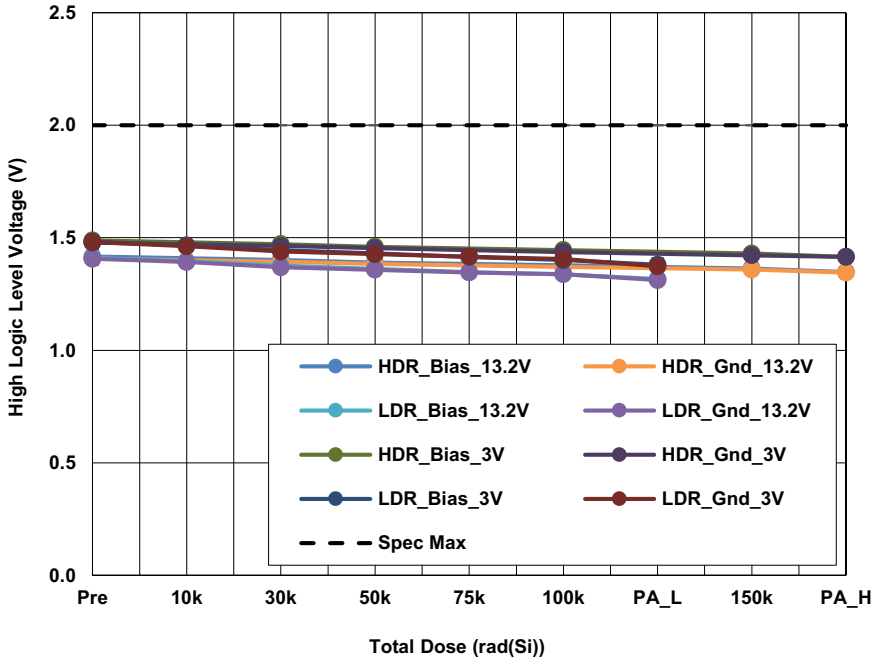


Figure 15. ISL7x814SEH high logic level voltage (V_{IH}) at V_{CC} = 3V and 13.2V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limit is 2.0V minimum.

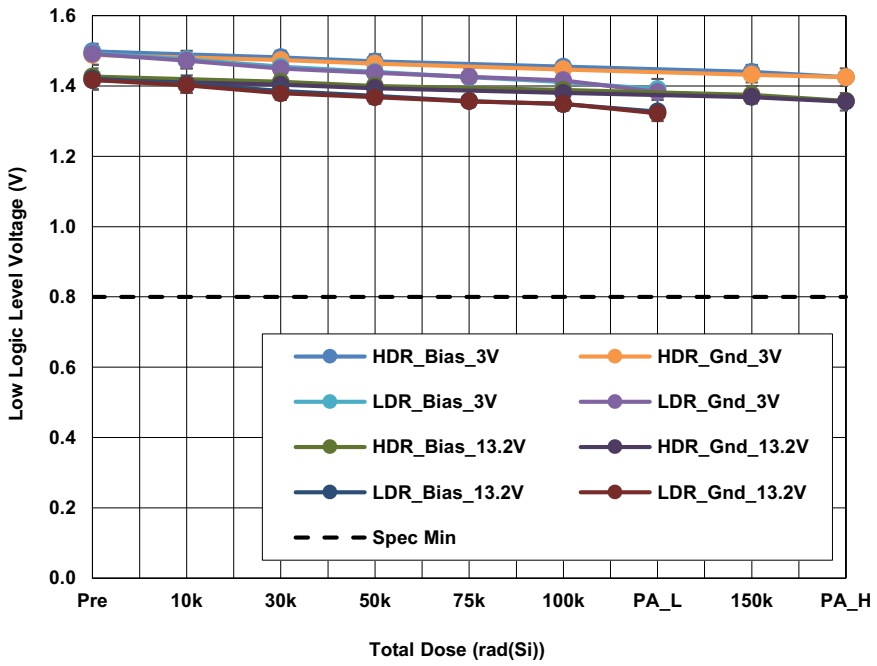


Figure 16. ISL7x814SEH low logic level voltage (V_{IL}) at V_{CC} = 3V and 13.2V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limit is 0.8V maximum.

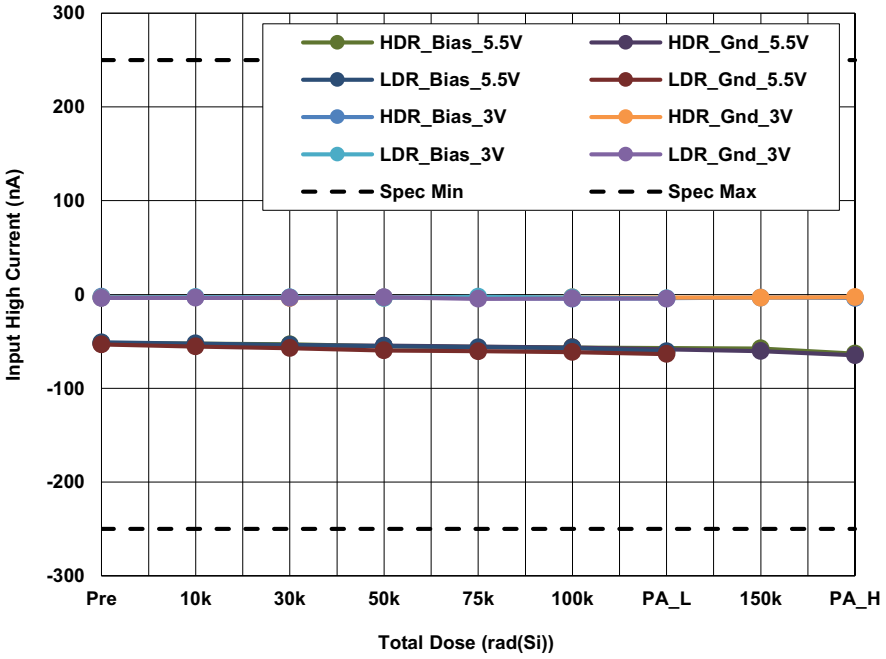


Figure 17. ISL7x814SEH input high current (I_{IH}) at V_{CC} = 3V and 5.5V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are -250nA minimum and 250nA maximum.

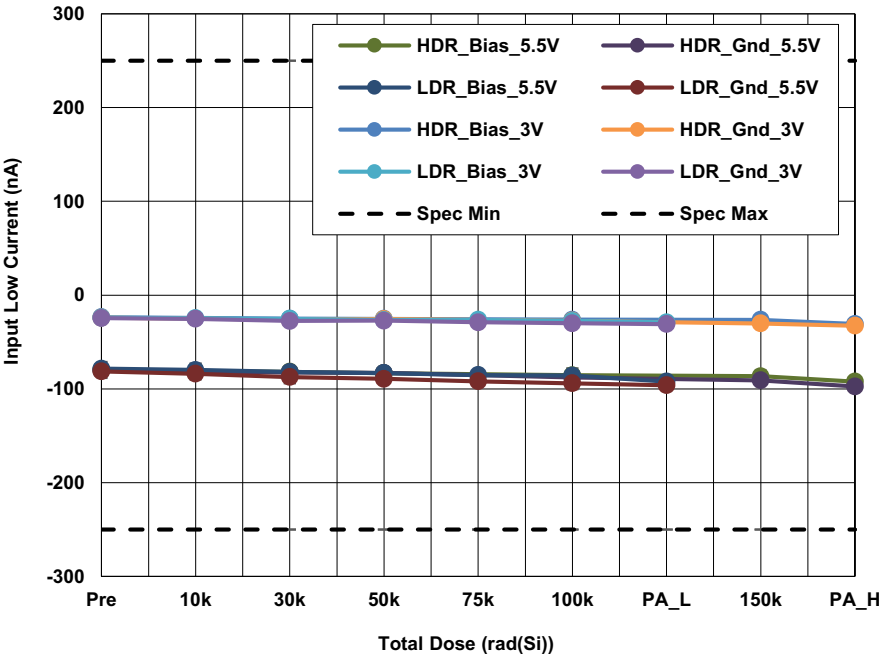


Figure 18. ISL7x814SEH input low current (I_{IL}), at V_{CC} = 3V and 5.5V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limits are -250nA minimum and 250nA maximum.

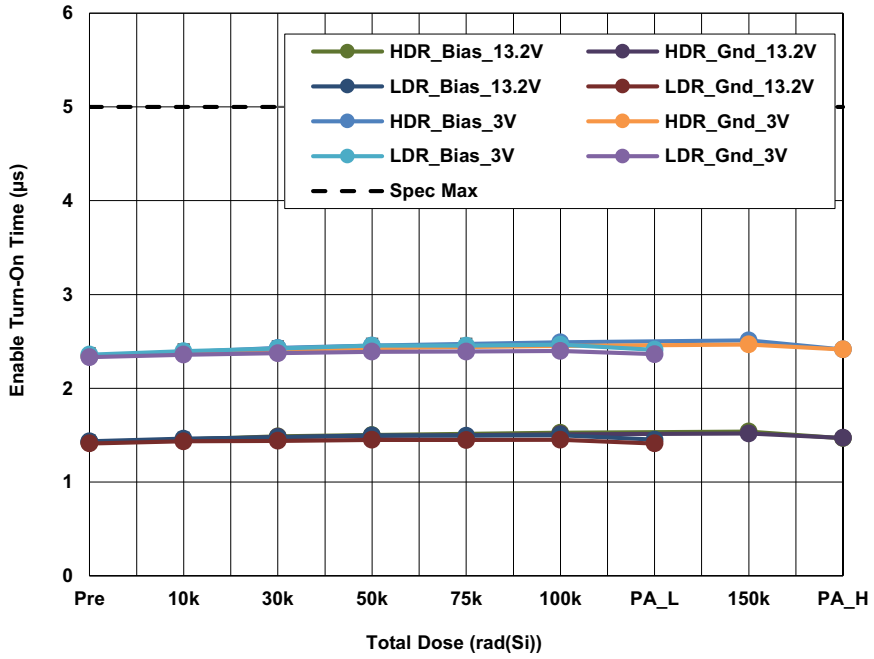


Figure 19. ISL7x814SEH enable turn-on time (t_{EN}) at V_{CC} = 3V and 13.2V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limit is 5µs maximum.

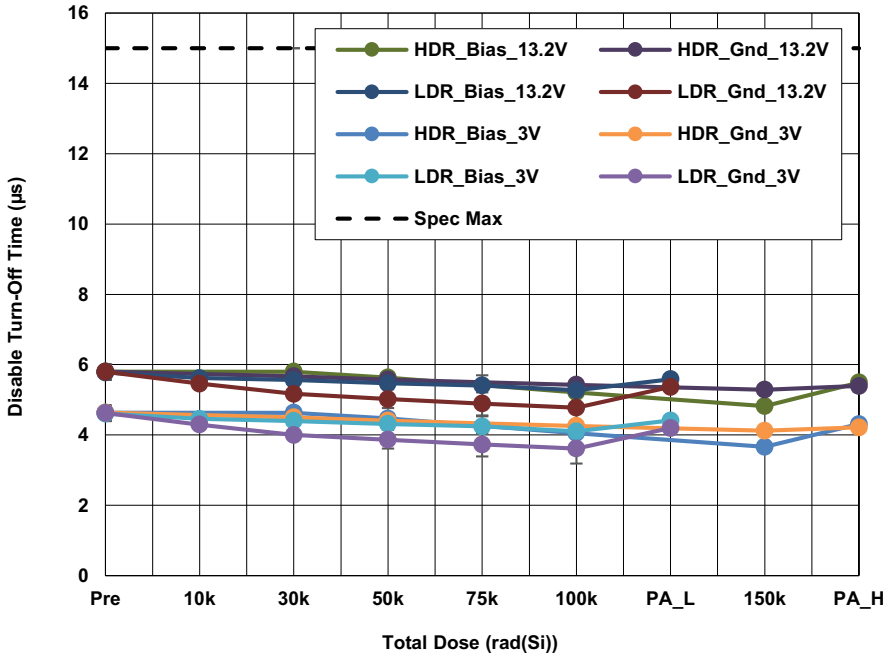


Figure 20. ISL7x814SEH disable turn-off time (t_{DIS}), at V_{CC} = 3V and 13.2V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations. The error bars (if visible) represent the minimum and maximum measured values. The post-irradiation SMD limit is 15µs maximum.

3. Discussion and Conclusion

We report the results of LDR and HDR total dose tests of the ISL7x814SEH 16 Channel Current Driver. Both irradiations were followed by a 168-hour anneal at +100°C under bias. All tested SMD parameters passed at all downpoints. No dose rate, bias, or anneal sensitivity was observed, although, as can be seen in Figure 6 on page 7, the total off-channel leakage current does increase after 50krad(Si) for the biased samples. However, the 150krad(Si) value is well below the 100nA limit and it returns to normal after the anneal. “Attributes Data” on page 4 summarizes the attributes data for the test. “Key Parameter Listing” on page 5 reviews the SMD parameters for the part. Finally “Key Parameter Variables Data” on page 5 provides plots of the total dose response for the selected parameters.

4. Revision History

Rev.	Date	Description
0.00	Mar.8.19	Initial release

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers skilled in the art designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only for development of an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising out of your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Rev.1.0 Mar 2020)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit:
www.renesas.com/contact/

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.