ISL75051ASEH

Total Dose Test Report

TR066
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Introduction

This report documents the results of Low Dose Rate (LDR) and High Dose Rate (HDR) total dose testing of the ISL75051ASEH low dropout regulator. The results also include post-irradiation high temperature biased annealing. The tests were conducted to assess the total dose hardness of the part and to determine any dose rate, bias, or anneal sensitivity. Parts were irradiated under bias and with all pins grounded - at LDR to 100krad(Si) and at HDR to 150krad(Si), followed by high temperature biased anneals. The ISL75051ASEH is rated at 100krad(Si) at high dose rate (50-300rad(Si)/s) and at 50krad(Si) at LDR (0.01rad(Si)/s) and is acceptance tested on a wafer-by-wafer basis to these limits.

Product Description

The ISL75051ASEH is a radiation hardened, low voltage, high current single output Low Dropout (LDO) linear voltage regulator specified for a 3.0A continuous output current. The device operates over an input voltage range of 2.2V to 6.0V and provides output voltages of 0.8V to 5.0V, with the output voltage adjusted by an external resistor divider network. Dropout voltages as low as 65mV can be achieved using the device.

The OCP pin allows the short-circuit output current limit threshold to be programmed by a resistor from the OCP pin to GND. The OCP setting range is 0.5A minimum to 8.5A maximum. The resistor sets the constant current threshold for the output under fault conditions. The thermal shutdown disables the output if the device temperature exceeds the specified value. It subsequently enters an ON/OFF cycle until the fault is removed. The ENABLE feature allows the part to be placed into a low current shutdown mode that typically draws about 10µA.

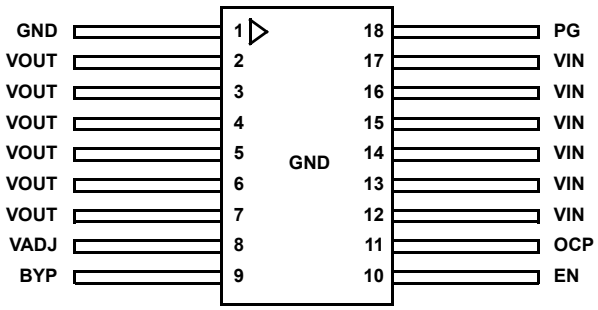
The ISL75051ASEH is implemented in the submicron P6 power management process, with 0.6µm minimum ground rules and three layers of interconnect. Active devices include low voltage CMOS and high voltage DMOS devices as well as complementary bipolar junction transistors. This process is in volume production under MIL-PRF-38535 certification and is used for a wide range of commercial power management devices.

The pinout configuration for the ISL75051ASEH is shown in Figure 1 on page 2, with the pin descriptions shown in Table 1 on page 2. The part is available in an 18 Ld CDFP package.

Related Literature

For a full list of related documents, visit our website

- ISL75051ASEH product page
- MIL-STD-883 Test Method 1019



Note: The ESD triangular mark indicates Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

Figure 1. ISL75051ASEH Pin Configuration

Table 1. ISL75051ASEH Pin Descriptions

Pin Number	Pin Name	Description
1	GND	GND pin.
2, 3, 4, 5, 6, 7	VOUT	Output voltage pins.
8	VADJ	The VADJ pin allows V_{OUT} to be programmed with an external resistor divider.
9	BYP	To filter the internal reference, connect a 0.1µF capacitor from the BYP pin to GND.
10	EN	V_{IN} independent chip enable. TTL and CMOS compatible.
11	OCP	Allows the current limit to be programmed with an external resistor.
12, 13, 14, 15, 16, 17	VIN	Input supply pins.
18	PG	V_{OUT} in regulation signal. Logic low defines when V_{OUT} is not in regulation. Must be grounded if not used.
Top Lid	GND	The top lid is connected to the GND pin of the package.
Bottom Metal	-	The bottom E-pad is available only on the K18.E package and is not electrically connected.

1. Test Description

1.1 Irradiation Facilities

High dose rate testing was performed at 187.6rad(Si)/s using a Gammacell 220 industry standard irradiator located in the Renesas facility in Palm Bay, Florida. Low dose rate testing was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic irradiator. Both irradiators use PbAl spectrum hardening filters to shield the test board and devices under test against low energy secondary gamma radiation. Half of the samples were irradiated under bias and the other half were grounded during irradiation. Samples from both dose rates underwent post-irradiation anneal at 100°C for 168 hours in a small temperature chamber.

1.2 Test Fixturing

Figure 2 shows the configuration used for biased irradiation at both dose rates. Note that the part is biased at 6V.

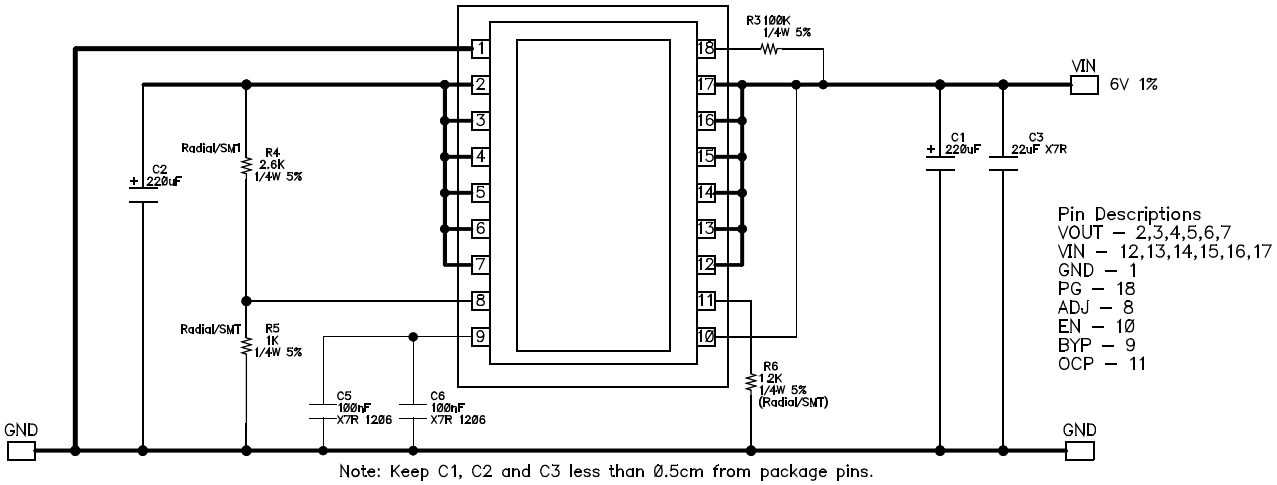


Figure 2. ISL75051ASEH TID Bias Schematic

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with data-logging at each downpoint.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 24 samples irradiated at low dose rate under bias, 24 samples irradiated at low dose rate with all pins grounded, 12 samples irradiated at high dose rate under bias, and 12 samples irradiated at high dose rate with all pins grounded. All anneal samples were biased. Due to oven size limitations, only 24 samples could be annealed at a time, so 12 biased and 12 unbiased samples were randomly chosen from the LDR matrix to include in the biased anneal. Three control units were used for both types of irradiation.

The ISL75051ASEH samples were from wafer lot 1JLUB. All samples were packaged in the 18 lead ceramic flatpack package (package code K18.D). Samples were processed through the standard burn-in cycle before irradiation.

1.5 Downpoints

Downpoints for the LDR tests were 0, 10, 30, 50, 75, and 100krad(Si). Downpoints for the HDR tests were 0, 30, 50, 100, and 150krad(Si). Both exposures were followed by a 168 hour high temperature anneal at 100°C under bias.

2. Test Results

2.1 Attributes Data

Total dose testing of the ISL75051ASEH is complete. All tested parameters passed the SMD limits. Table 2 summarizes the results.

Table 2. ISL75051ASEH Total Dose Test Attributes Data

Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass (Note 1)	Fail
0.01	Biased (Figure 2 on page 3)	24	Pre-irradiation	24	0
			10krad(Si)	24	0
			30krad(Si)	24	0
			50krad(Si)	24	0
			75krad(Si)	24	0
			100krad(Si)	24	0
			Anneal	12	0
0.01	GND	24	Pre-irradiation	24	
			10krad(Si)	24	0
			30krad(Si)	24	0
			50krad(Si)	24	0
			75krad(Si)	24	0
			100krad(Si)	24	0
			Anneal	12	0
167.5	Biased (Figure 2)	12	Pre-irradiation	12	
			30krad(Si)	12	0
			50krad(Si)	12	0
			100krad(Si)	12	0
			150krad(Si)	12	0
			Anneal	12	0
167.5	GND	12	Pre-irradiation	12	
			30krad(Si)	12	0
			50krad(Si)	12	0
			100krad(Si)	12	0
			150krad(Si)	12	0
			Anneal	12	0

Note:
1. ‘Pass’ indicates a sample that passes all SMD limits.

2.2 Key Parameter Listing

Table 3 lists 35 key selected parameters that indicate part performance. These parameters are plotted in Figures 3 through 37 (starting on page 6). All limits are taken from the ISL75051ASEH SMD; see the SMD 5962-11212 for further detail.

Table 3. ISL75051ASEH SMD Total Dose Key SMD Parameters (T_A = +25°C)

Figure	Parameter	Symbol	Limit, Low	Limit, High	Unit
3	DC output voltage accuracy, 0.52V out, 2.2V in, no load	V_{OUT}	0.512	0.528	V
4	DC output voltage accuracy, 0.52V out, 2.2V in, 3A load	V_{OUT}	0.512	0.528	V
5	DC output voltage accuracy, 0.52V out, 3.6V in, no load	V_{OUT}	0.512	0.528	V
6	DC output voltage accuracy, 0.52V out, 3.6V in, 3A load	V_{OUT}	0.512	0.528	V
7	DC output voltage accuracy, 0.52V out, 5.5V in, no load	V_{OUT}	0.512	0.528	V
8	DC output voltage accuracy, 1.5V out, 2.2V in, no load	V_{OUT}	1.478	1.522	V
9	DC output voltage accuracy, 1.5V out, 2.2V in, 3A load	V_{OUT}	1.478	1.522	V
10	DC output voltage accuracy, 1.5V out, 3.6V in, no load	V_{OUT}	1.478	1.522	V
11	DC output voltage accuracy, 1.5V out, 3.6V in, 3A load	V_{OUT}	1.478	1.522	V
12	DC output voltage accuracy, 1.5V out, 5.5V in, no load	V_{OUT}	1.478	1.522	V
13	DC output voltage accuracy, 1.8V out, 2.2V in, no load	V_{OUT}	1.773	1.827	V
14	DC output voltage accuracy, 1.8V out, 2.2V in, 3A load	V_{OUT}	1.773	1.827	V
15	DC output voltage accuracy, 1.8V out, 3.6V in, no load	V_{OUT}	1.773	1.827	V
16	DC output voltage accuracy, 1.8V out, 3.6V in, 3A load	V_{OUT}	1.773	1.827	V
17	DC output voltage accuracy, 1.8V out, 5.5V in, no load	V_{OUT}	1.773	1.827	V
18	DC output voltage accuracy, 5.0V out, 5.4V in, no load	V_{OUT}	4.925	5.075	V
19	DC output voltage accuracy, 5.0V out, 5.4V in, 3A load	V_{OUT}	4.925	5.075	V
20	DC output voltage accuracy, 5.0V out, 6.0V in, no load	V_{OUT}	4.925	5.075	V
21	DC output voltage accuracy, 5.0V out, 6.0V in, 3A load	V_{OUT}	4.925	5.075	V
22	Feedback pin, 1.5V out, 2.2V in, no load	V_{ADJ}	514.8	525.2	mV
23	Feedback pin, 1.5V out, 6.0V in, no load	V_{ADJ}	514.8	525.2	mV
24	DC input line regulation, 1.5V out			3.50	mV
25	DC input line regulation, 1.8V out			3.50	mV
26	DC input line regulation, 5.0V out			20.0	mV
27	DC output load regulation, 1.5V out		-4.00	-0.10	mV
28	DC output load regulation, 1.8V out		-4.80	-0.05	mV
29	DC output load regulation, 5.0V out		-15.0	-0.05	mV
30	Feedback input current, V_{ADJ} = 0.5V			1.00	µA
31	Ground pin current, 1.5V out, 2.2V in, no load	I_Q		13.0	mA
32	Ground pin current, 5.0V out, 6.0V in, no load	I_Q		19.0	mA
33	Ground pin current, 1.5V out, 2.2V in, 3A load	I_Q		14.0	mA
34	Ground pin current, 5.0V out, 6.0V in, 3A load	I_Q		20.0	mA
35	Dropout voltage, 2.5V out, 1A load	V_{DO}		100	mV
36	Dropout voltage, 2.5V out, 2A load	V_{DO}		200	mV
37	Dropout voltage, 2.5V out, 3A load	V_{DO}		300	mV

2.3 Key Parameter Variables Data

The plots in Figures 3 through 37 illustrate the TID response of key selected SMD parameters outlined in "Key Parameter Listing" on page 5. The plots show the average tested values of the parameters as a function of total dose and high temperature biased anneal for each of the irradiation conditions, Biased and Grounded, at Low Dose Rate (LDR) and High Dose Rate (HDR). For example, the legend LDR_Bias indicates the average LDR response for Biased parts. On the x-axis, along with the total dose, PA_L and PA_H represent the Post-Anneal LDR and HDR points, respectively. The plots also include error bars at each downpoint, representing the minimum and maximum measured values of the samples, although in some plots the error bars might not be visible due to their values compared to the scale of the graph.

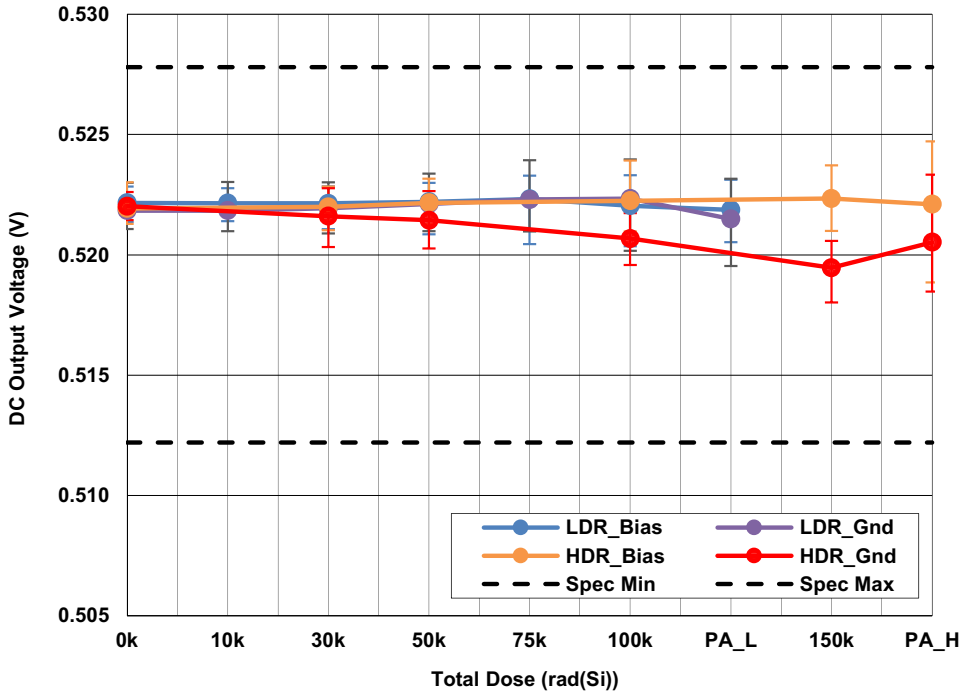


Figure 3. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 0.52V output, 2.2V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.512V minimum and 0.528V maximum.

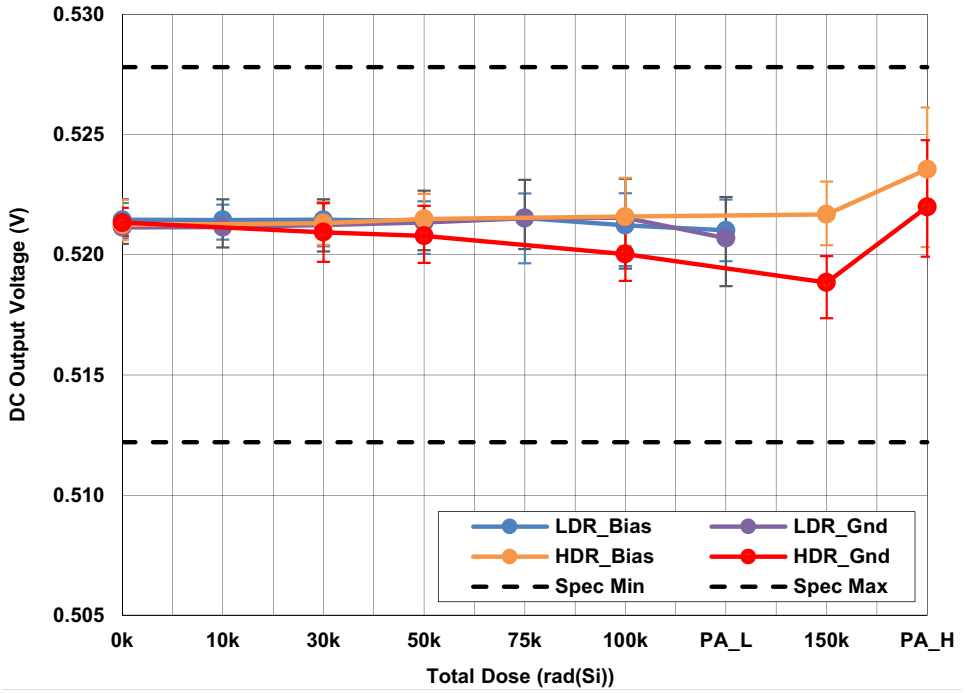


Figure 4. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 0.52V output, 2.2V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.512V minimum and 0.528V maximum.

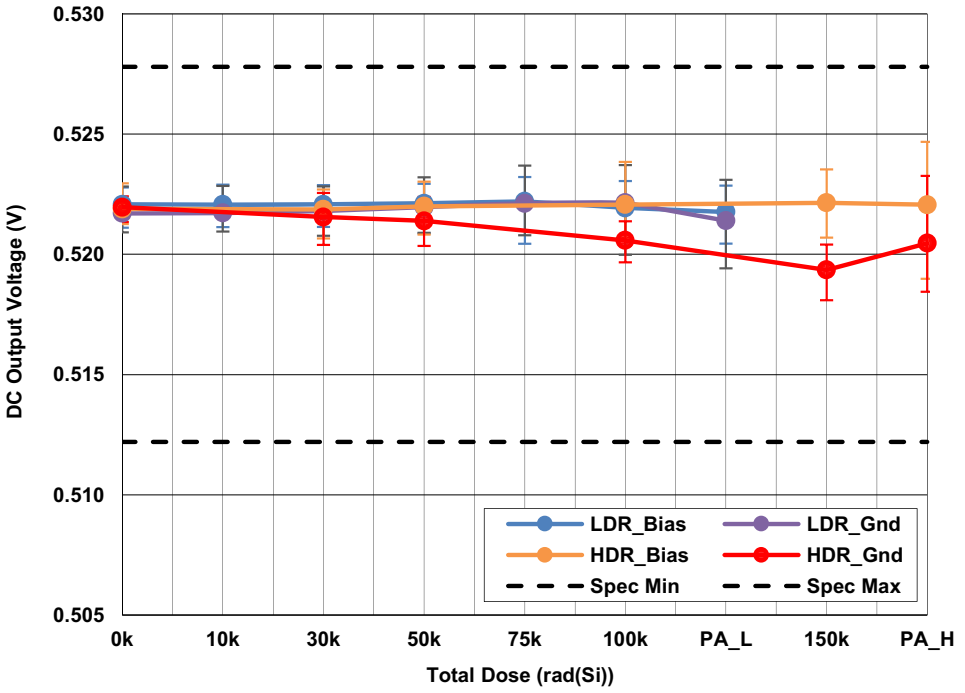


Figure 5. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 0.52V output, 3.6V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.512V minimum and 0.528V maximum.

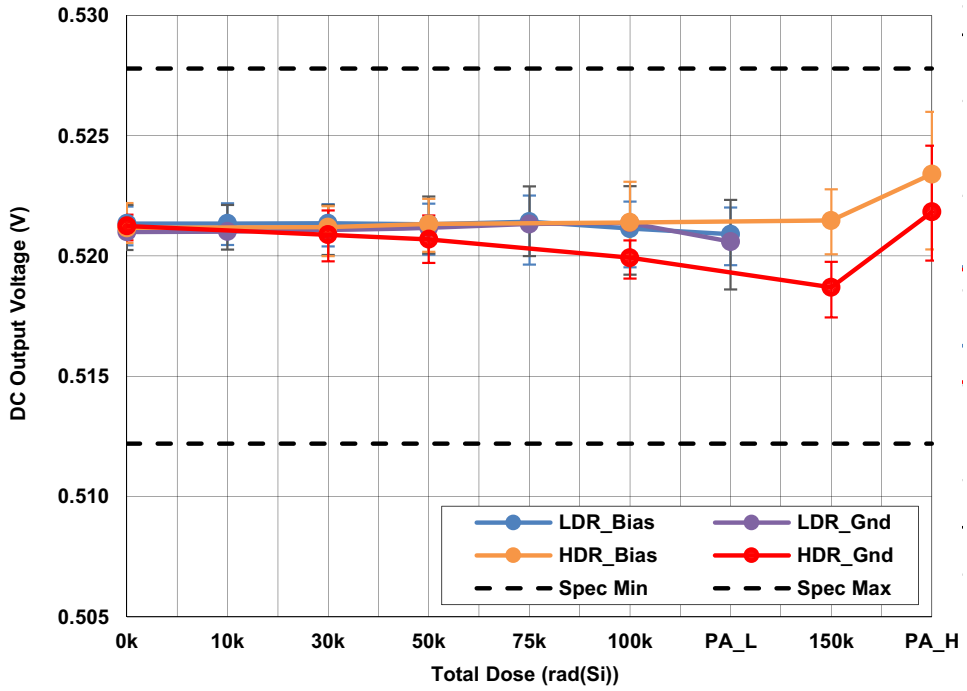


Figure 6. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 0.52V output, 3.6V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.512V minimum and 0.528V maximum.

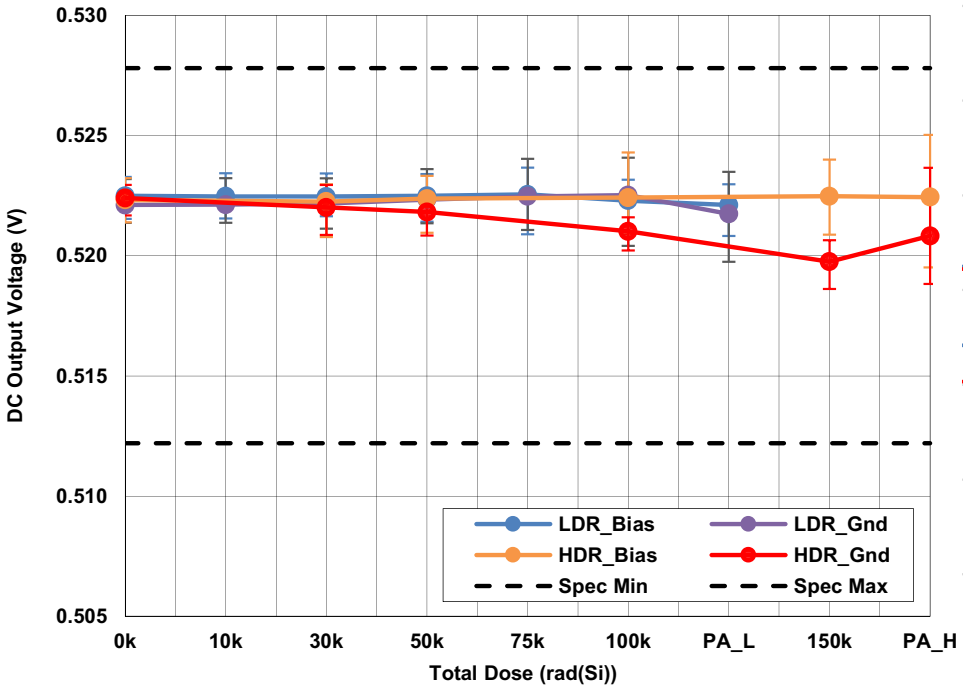


Figure 7. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 0.52V output, 5.5V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 0.512V minimum and 0.528V maximum.

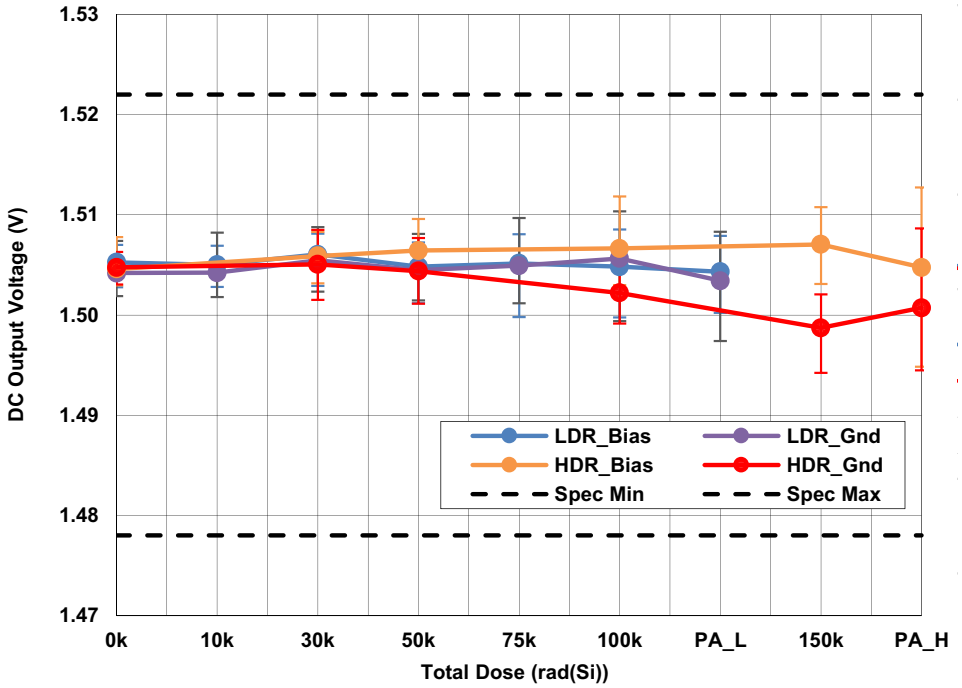


Figure 8. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.5V output, 2.2V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.478V minimum and 1.522V maximum.

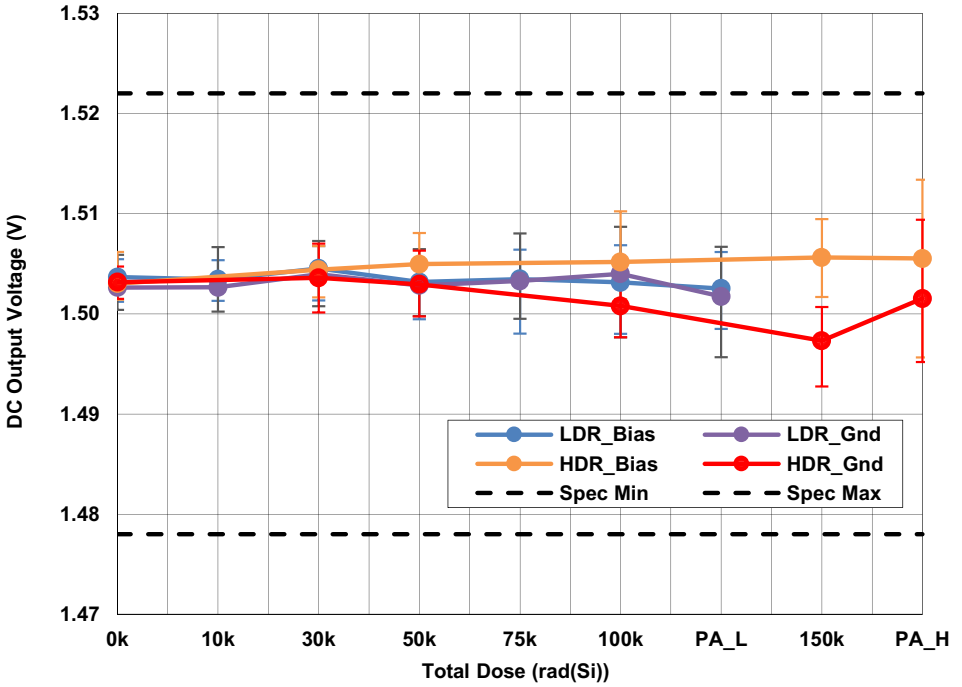


Figure 9. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.5V output, 2.2V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.478V minimum and 1.522V maximum.

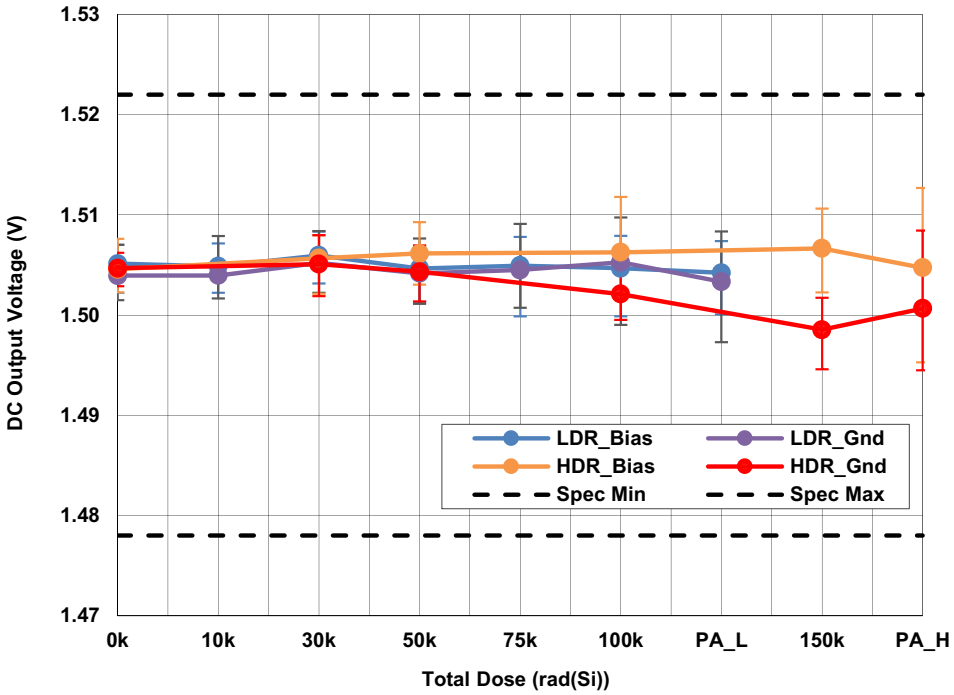


Figure 10. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.5V output, 3.6V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.478V minimum and 1.522V maximum.

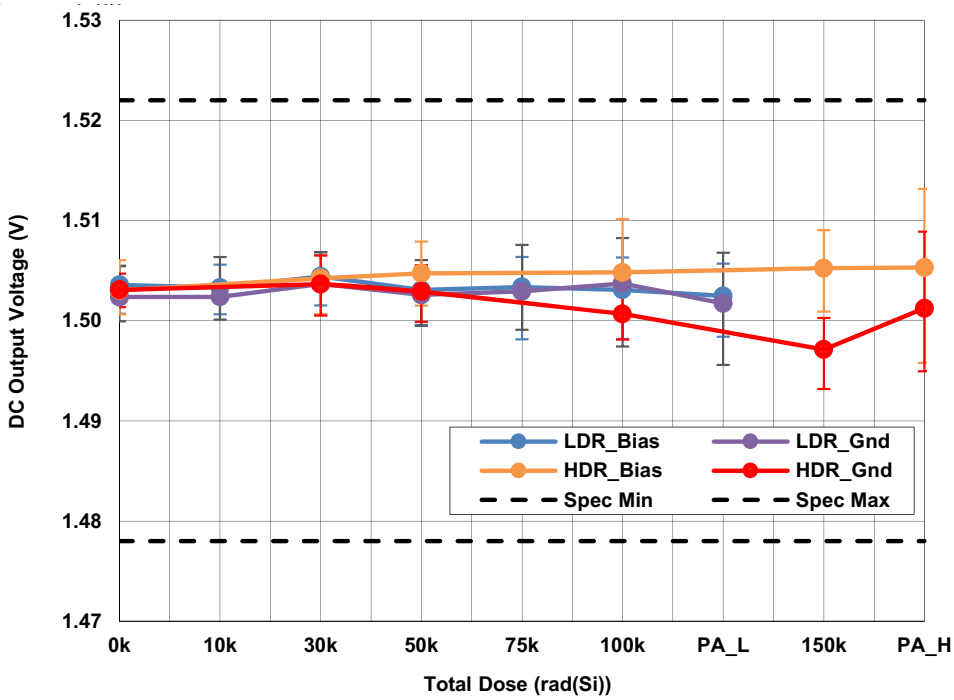


Figure 11. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.5V output, 3.6V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.478V minimum and 1.522V maximum.

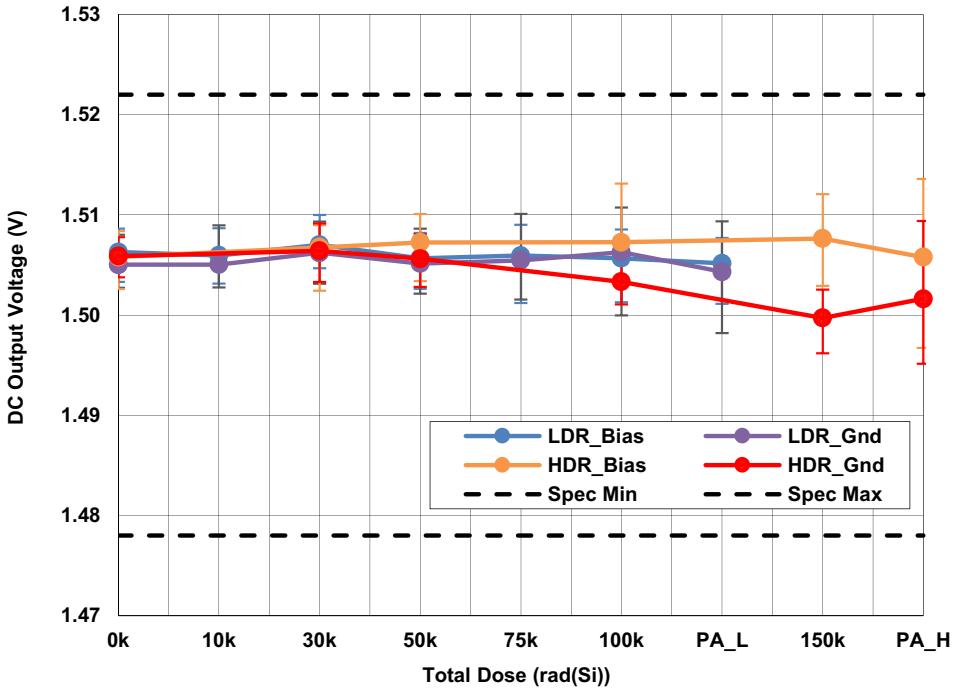


Figure 12. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.5V output, 5.5V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.478V minimum and 1.522V maximum.

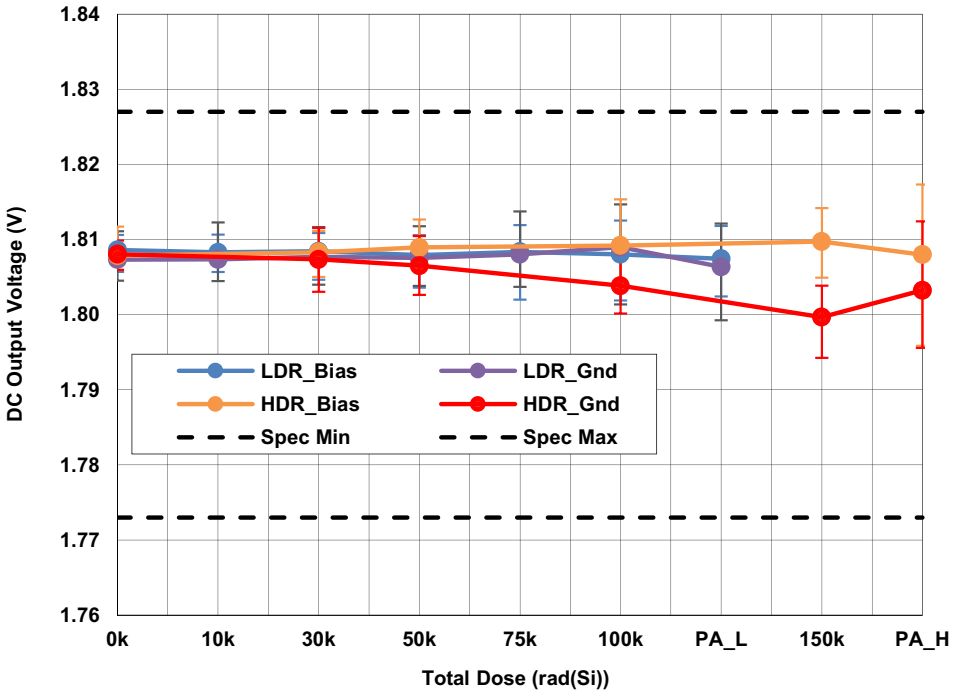


Figure 13. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.8V output, 2.2V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.773V minimum and 1.827V maximum.

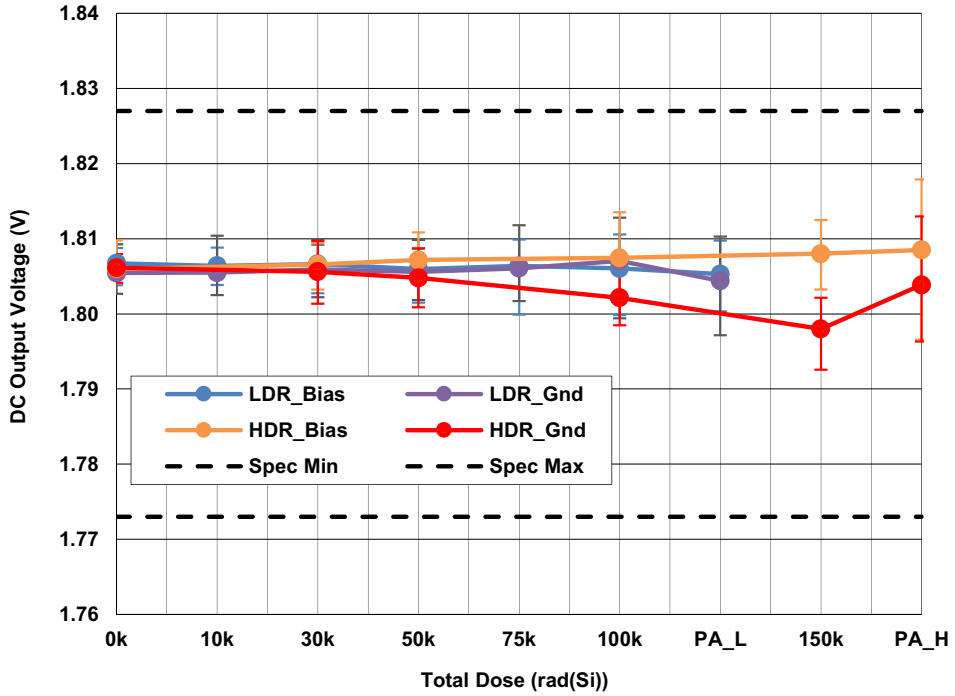


Figure 14. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.8V output, 2.2V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.773V minimum and 1.827V maximum.

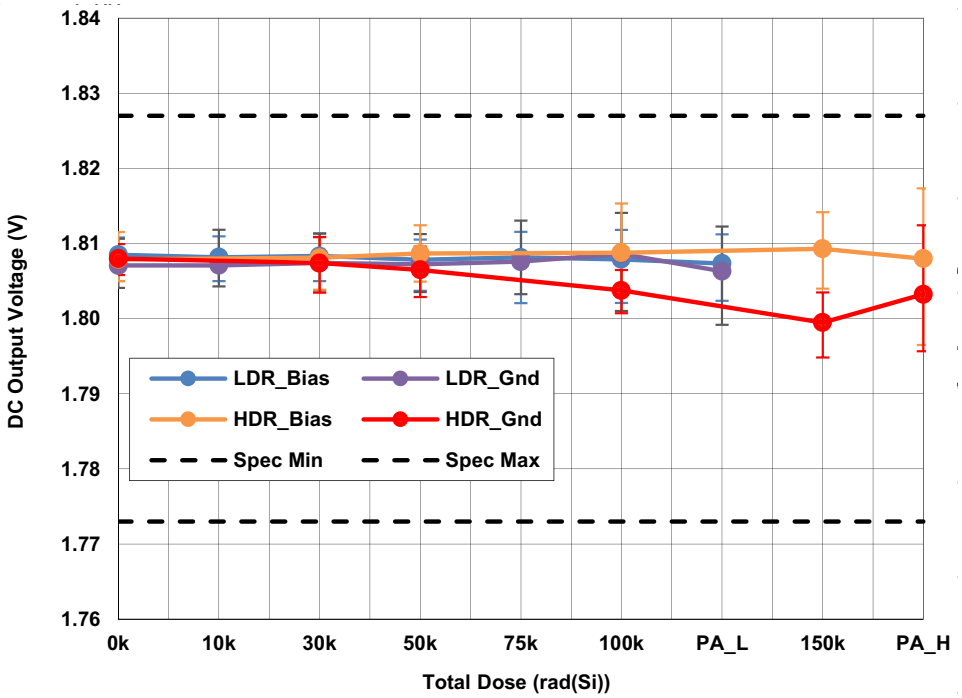


Figure 15. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.8V output, 3.6V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.773V minimum and 1.827V maximum.

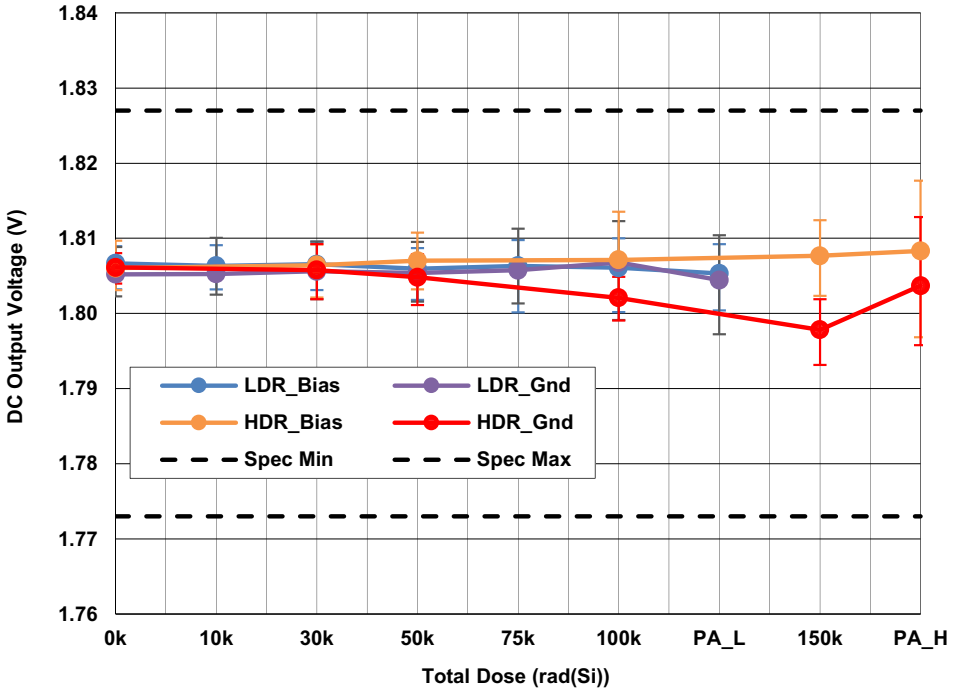


Figure 16. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.8V output, 3.6V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.773V minimum and 1.827V maximum.

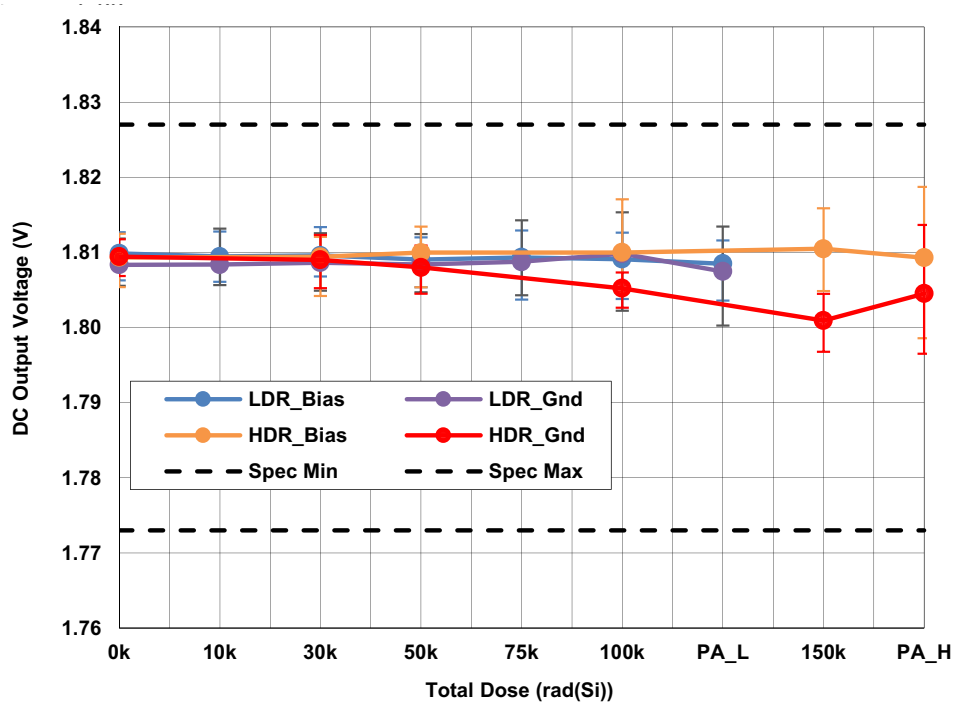


Figure 17. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 1.8V output, 5.5V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 1.773V minimum and 1.827V maximum.

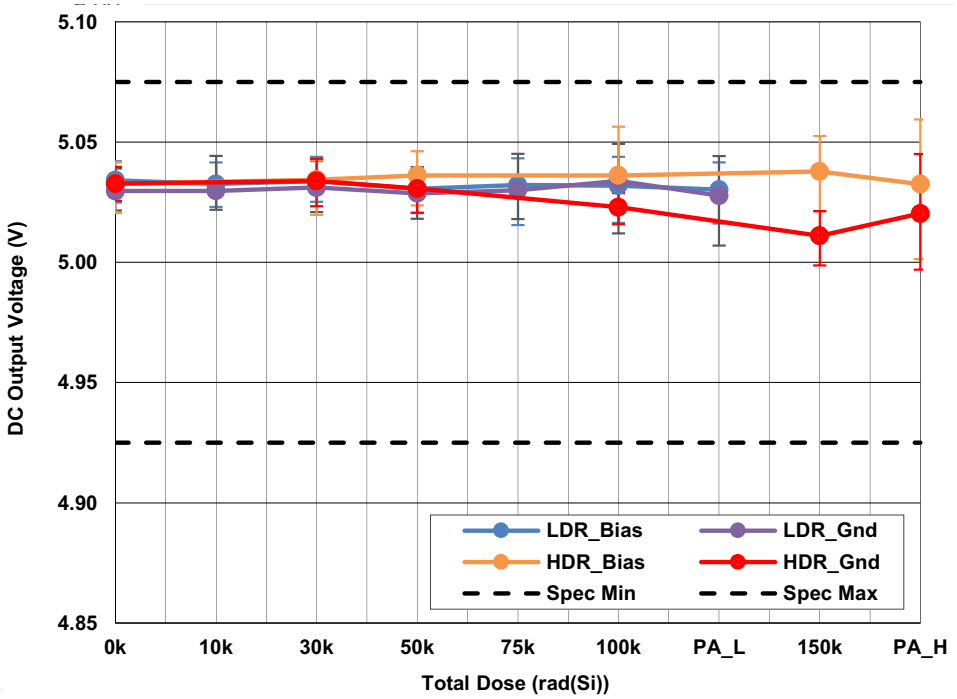


Figure 18. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 5.0V output, 5.4V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 4.925V minimum and 5.075V maximum.

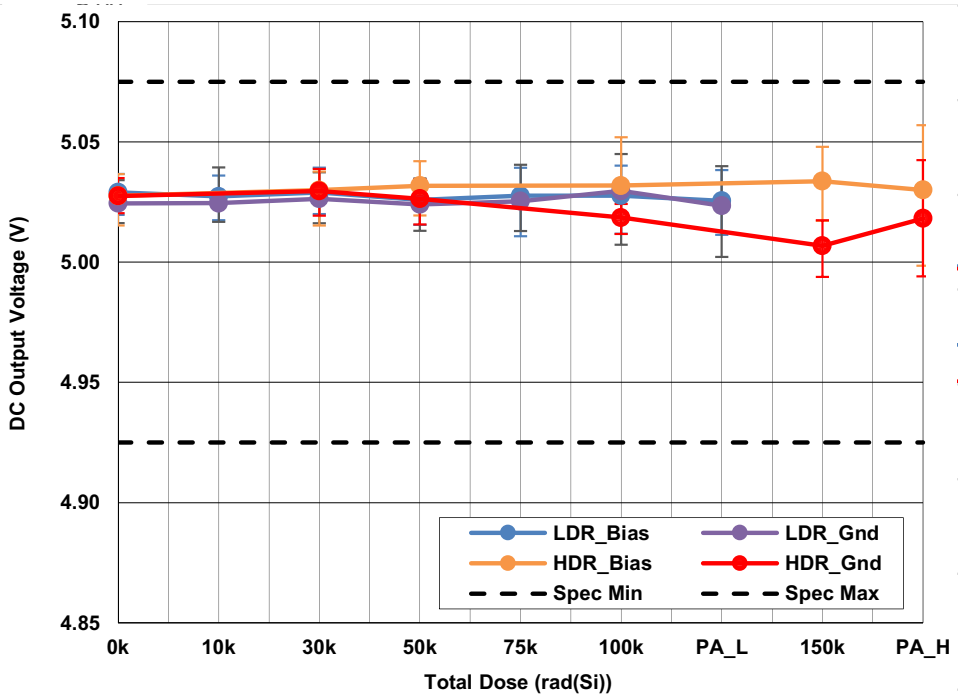


Figure 19. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 5.0V output, 5.4V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 4.925V minimum and 5.075V maximum.

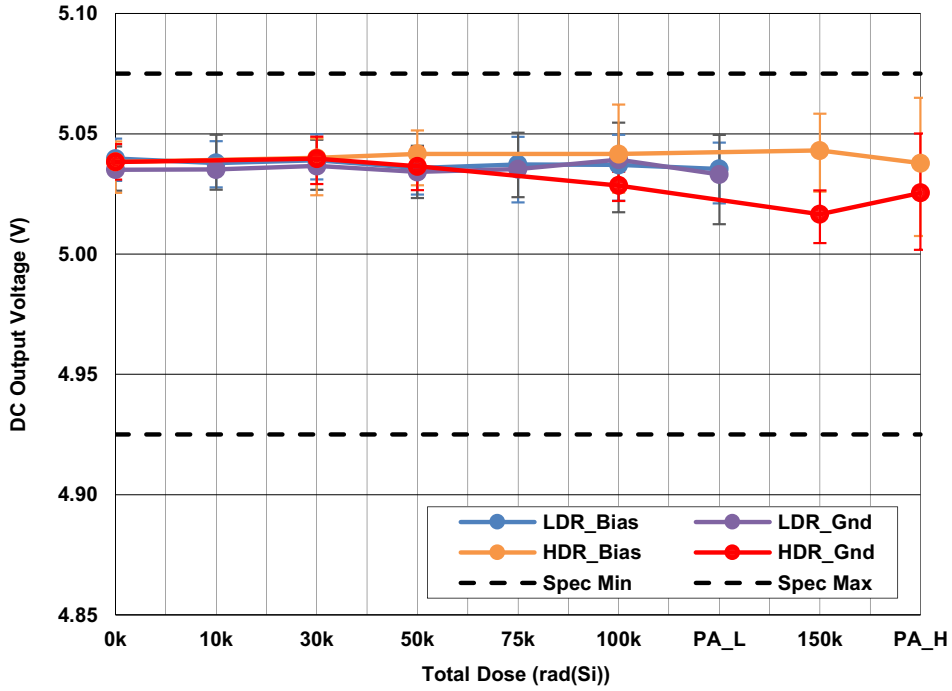


Figure 20. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 5.0V output, 6.0V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 4.925V minimum and 5.075V maximum.

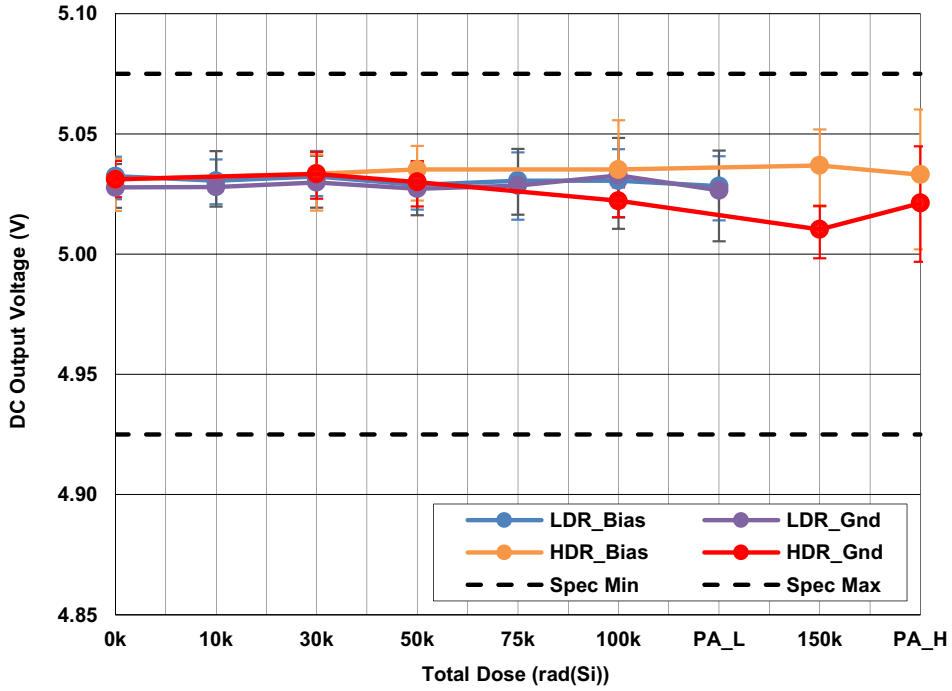


Figure 21. ISL75051ASEH DC output voltage accuracy (V_{OUT}), 5.0V output, 6.0V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 4.925V minimum and 5.075V maximum.

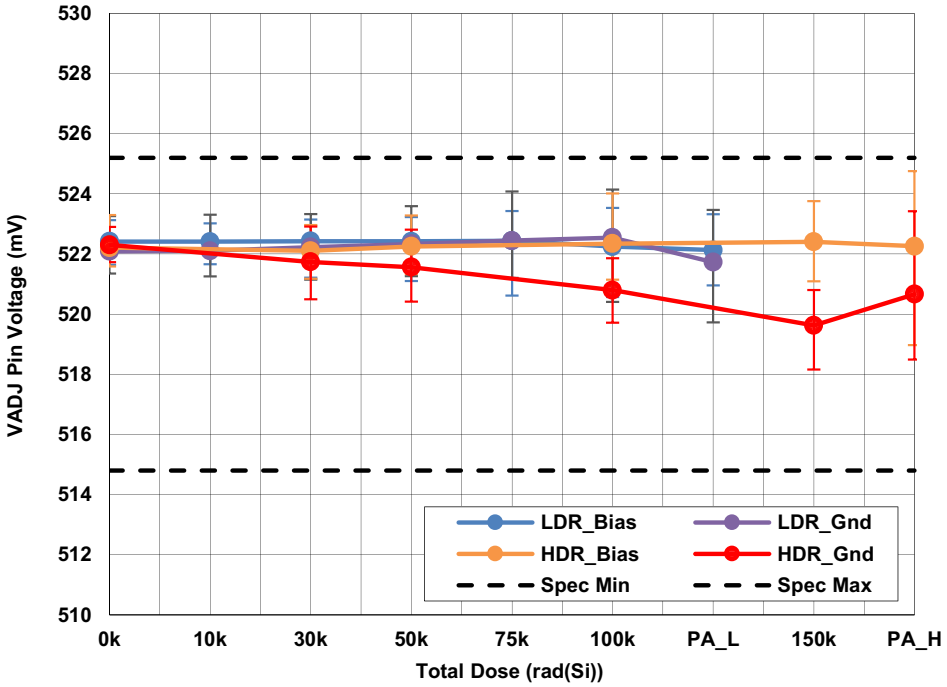


Figure 22. ISL75051ASEH feedback pin (VADJ), 1.5V output, 2.2V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 514.8mV minimum and 525.2mV maximum.

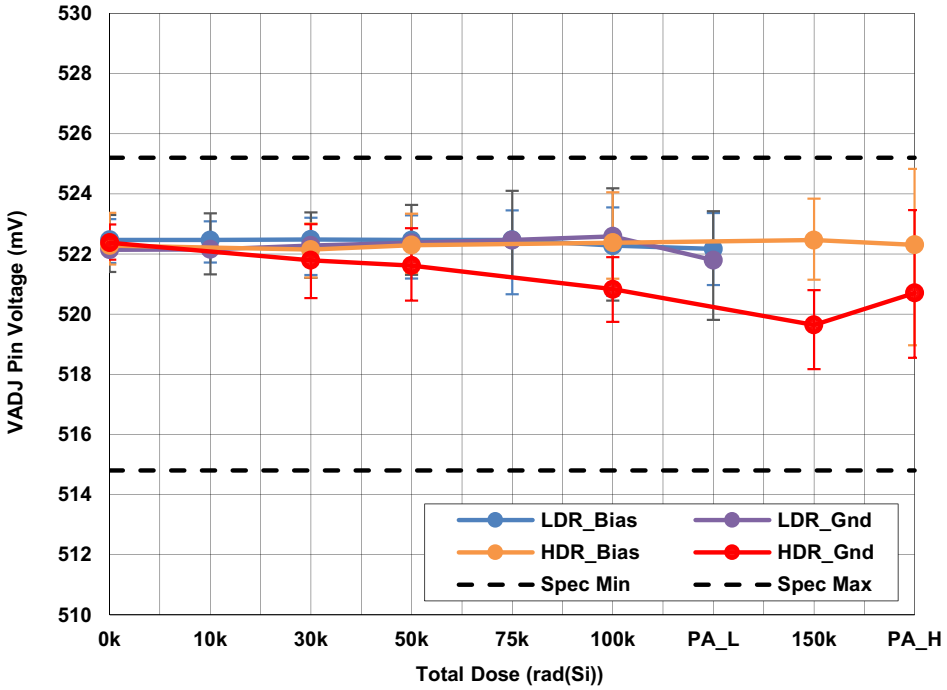


Figure 23. ISL75051ASEH feedback pin (VADJ), 1.5V output, 6.0V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are 514.8mV minimum and 525.2mV maximum.

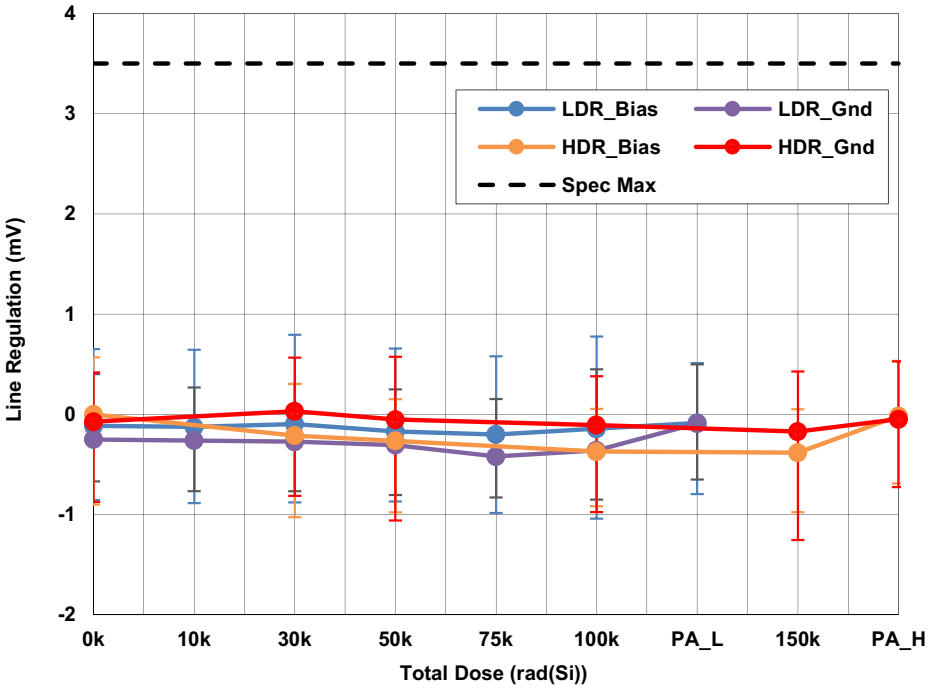


Figure 24. ISL75051ASEH DC input line regulation, 1.5V output, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 3.5mV maximum.

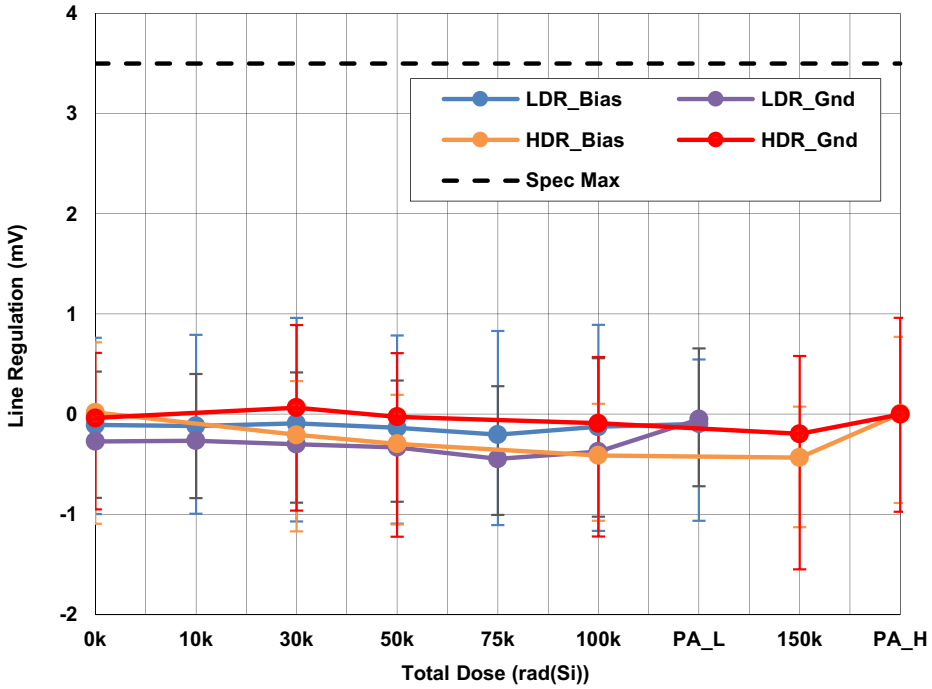


Figure 25. ISL75051ASEH DC input line regulation, 1.8V output, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 3.5mV maximum.

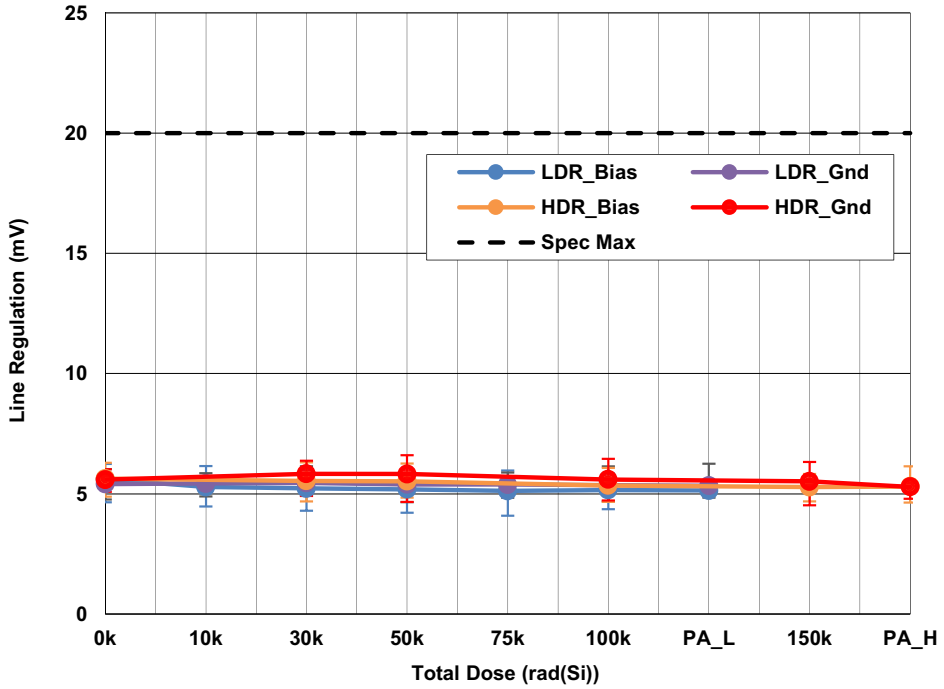


Figure 26. ISL75051ASEH DC input line regulation, 5.0V output, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 20mV maximum.

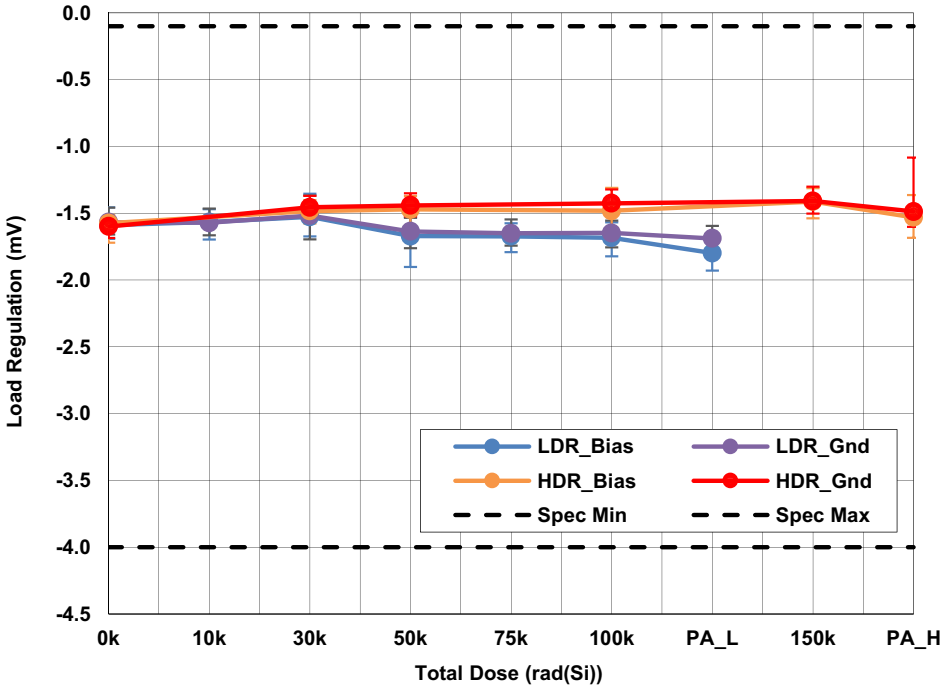


Figure 27. ISL75051ASEH DC output load regulation, 1.5V output, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are -4.00mV minimum and -0.10mV maximum.

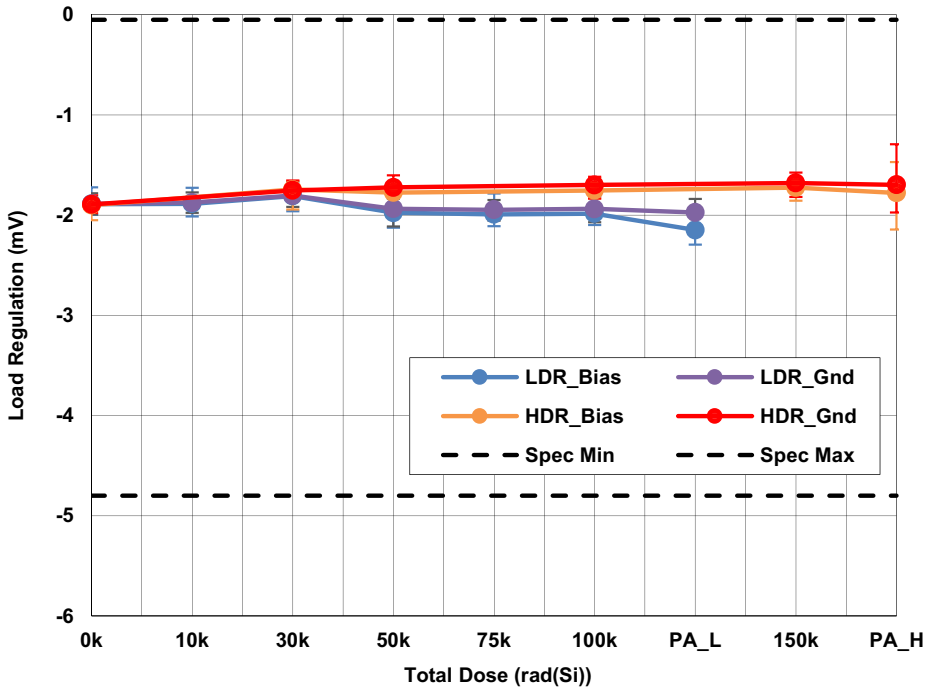


Figure 28. ISL75051ASEH DC output load regulation, 1.8V output, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are -4.80mV minimum and -0.05mV maximum.

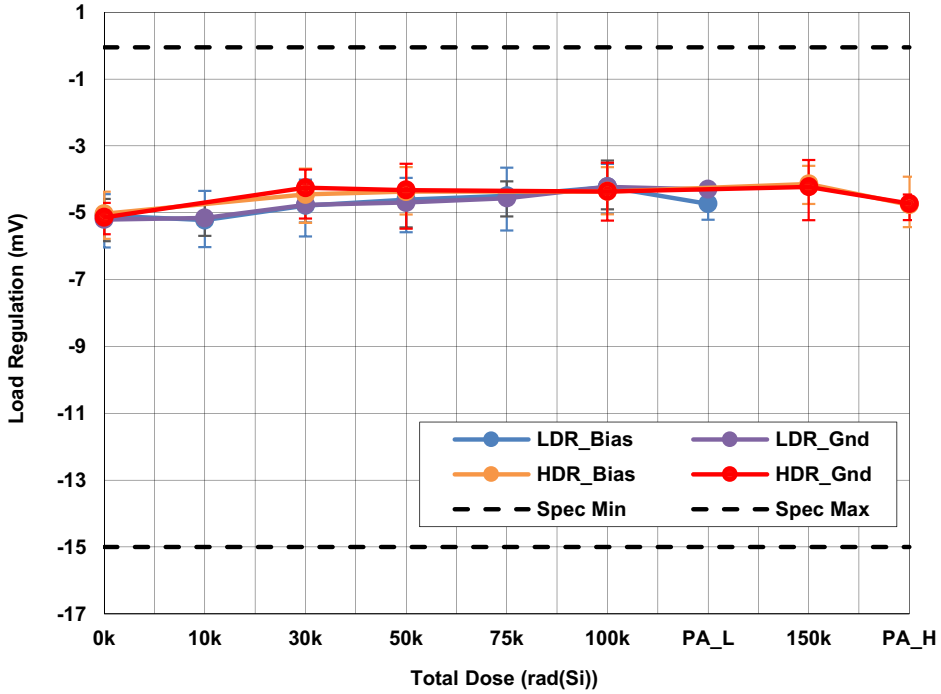


Figure 29. ISL75051ASEH DC output load regulation, 5.0V output, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limits are -15.0mV minimum and -0.05mV maximum.

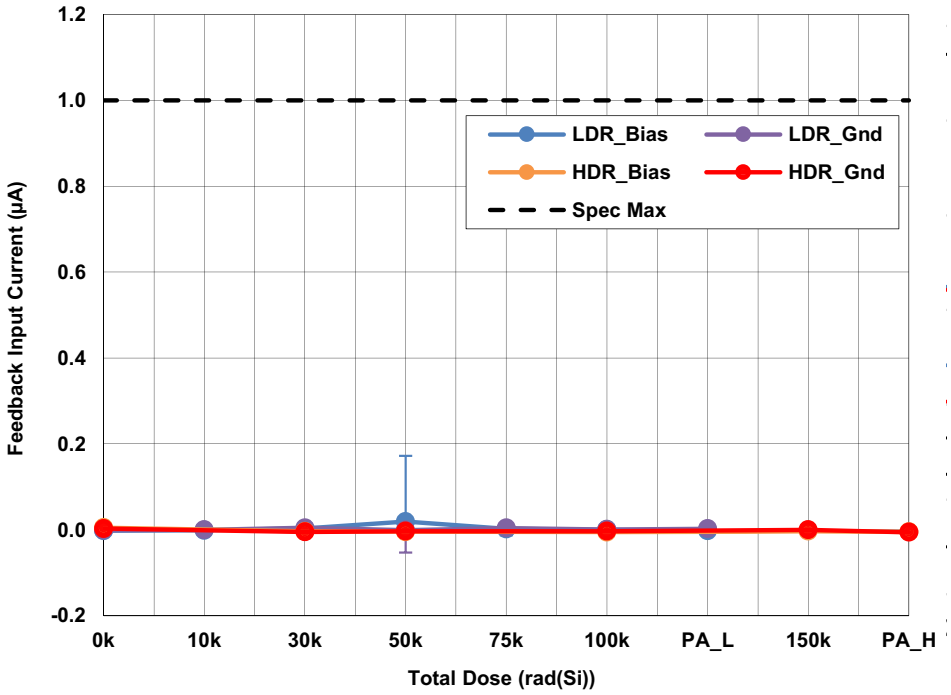


Figure 30. ISL75051ASEH feedback input current, V_{ADJ} = 0.5V, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 1µA maximum.

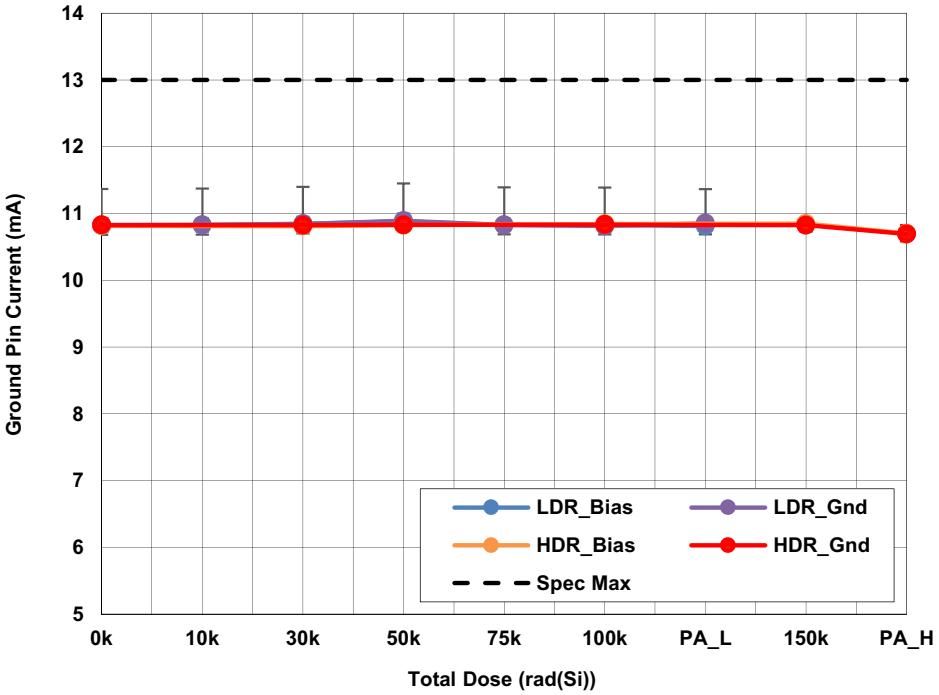


Figure 31. ISL75051ASEH ground pin current (I_Q), 1.5V output, 2.2V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 13mA maximum.

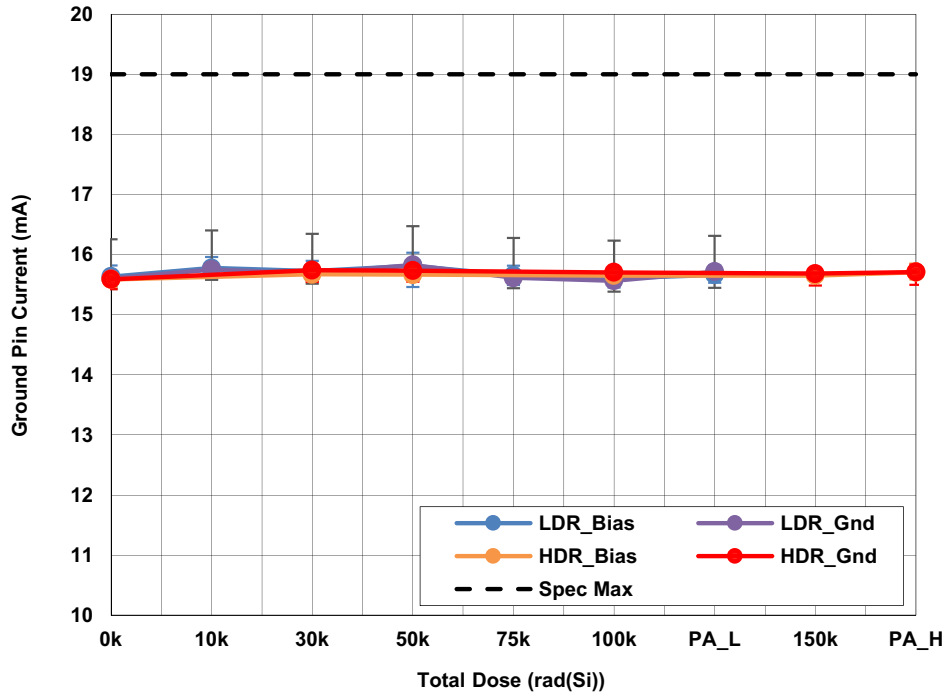


Figure 32. ISL75051ASEH ground pin current (I_Q), 5.0V output, 6.0V input, no load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 19mA maximum.

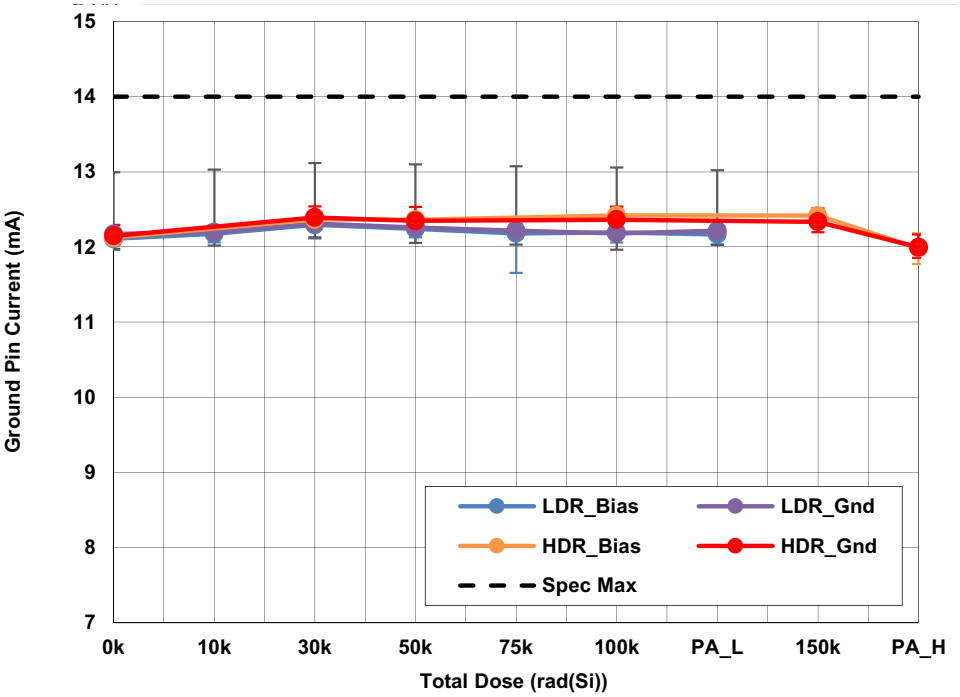


Figure 33. ISL75051ASEH ground pin current (I_Q), 1.5V output, 2.2V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 14mA maximum.

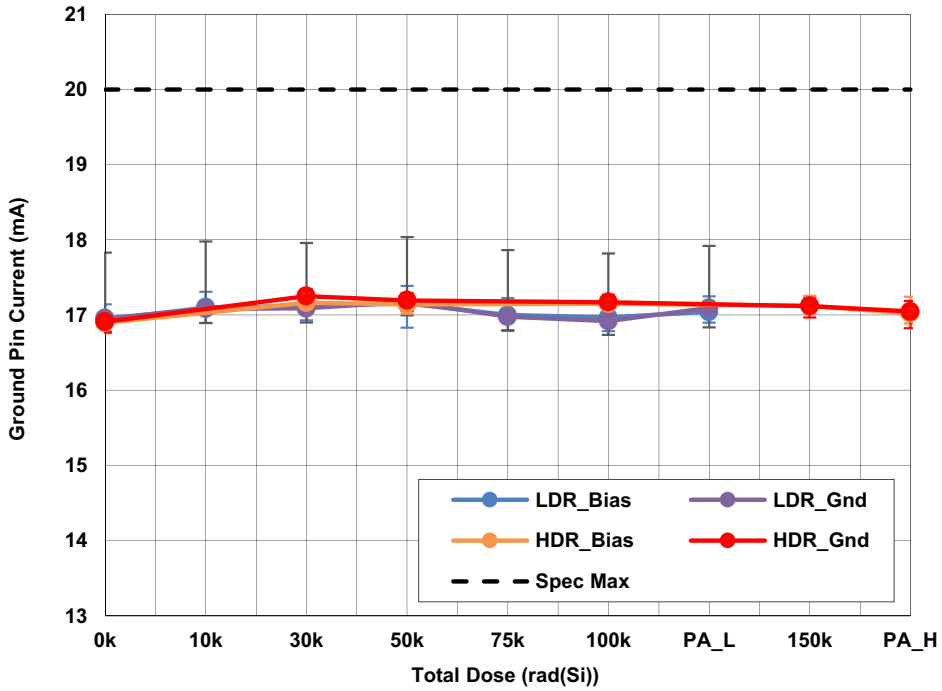


Figure 34. ISL75051ASEH ground pin current (I_Q), 5.0V output, 6.0V input, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 20mA maximum.

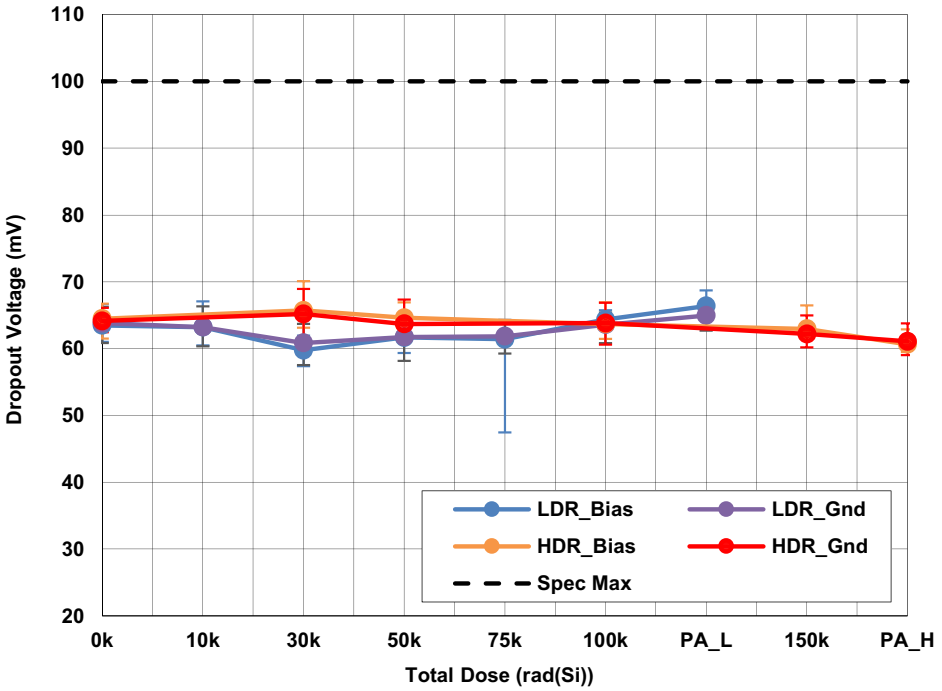


Figure 35. ISL75051ASEH dropout voltage (V_{DO}), 2.5V output, 1A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 100mV maximum.

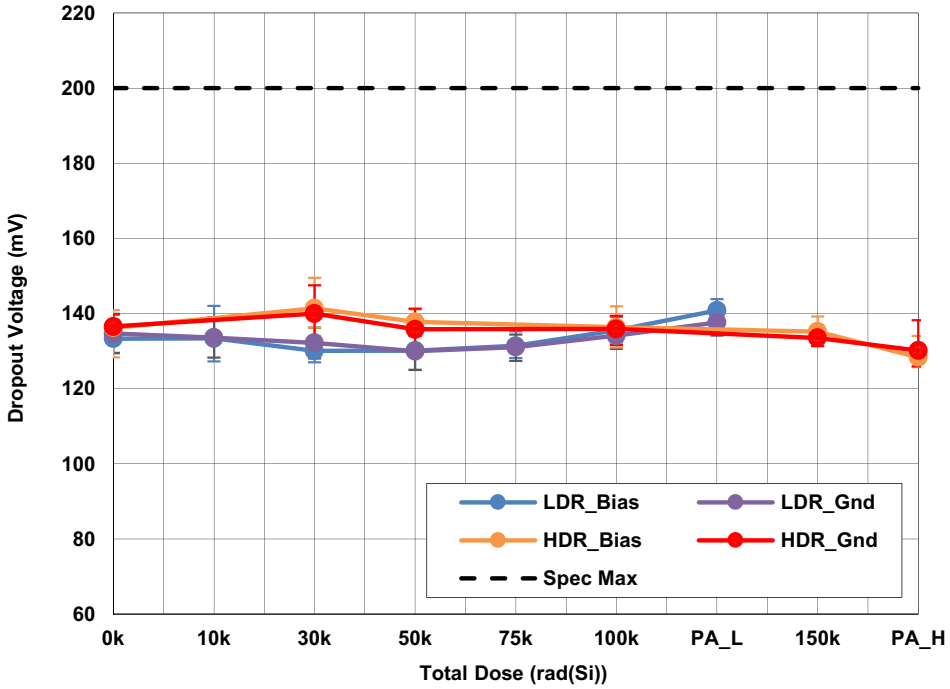


Figure 36. ISL75051ASEH dropout voltage (V_{DO}), 2.5V output, 2A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 200mV maximum.

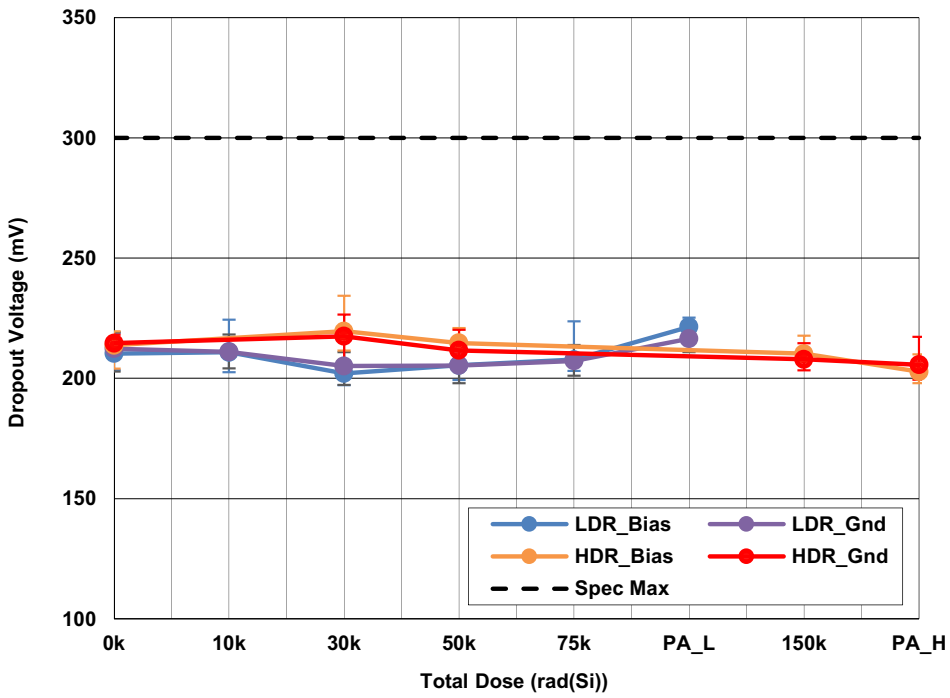


Figure 37. ISL75051ASEH dropout voltage (V_{DO}), 2.5V output, 3A load, as a function of total dose irradiation at LDR and at HDR for biased and grounded configurations and subsequent high temperature anneals. The error bars represent the minimum and maximum measured values. The post-irradiation SMD limit is 300mV maximum.

3. Discussion and Conclusion

We report the results of low and high dose rate total dose tests of the ISL75051ASEH low dropout regulator. Both irradiations were followed by a 168-hour anneal at 100°C under bias. All tested SMD parameters passed at all downpoints. No dose rate, bias, or anneal sensitivity was observed. "Attributes Data" on page 4 summarizes the attributes data for the test. "Key Parameter Listing" on page 5 summarizes selected key parameters for the part. Finally, "Key Parameter Variables Data" on page 6 provides plots of the total dose and anneal response for the selected parameters.

4. Revision History

Date	Rev.	Description
May 29, 2018	0.00	Initial release

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