ISL73040SEH

Total Dose Testing

TR061
Rev.0.00
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Introduction

This report documents the results of low dose rate total dose testing and subsequent high temperature biased annealing of the ISL73040SEH GaN FET driver. The tests were conducted to provide an assessment of the total dose hardness of the part and to provide an estimate of bias or anneal sensitivity. Parts were irradiated under bias and with all pins grounded at low dose rate. The ISL73040SEH is rated at 75krad(Si) at 0.01rad(Si)/s and is acceptance tested on a wafer-by-wafer basis to its SMD limits.

Product Description

The ISL73040SEH is a low-side driver designed to drive enhancement mode Gallium Nitride (eGaN) power FET devices. The part operates over a supply voltage range from 4.5V to 13.2V and offers both inverting (INB) and non-inverting (IN) inputs to satisfy requirements for inverting and non-inverting gate drive with a single device. The ISL73040SEH supplies 4.5V gate drive voltage (V_{DRV}) that is generated using an internal regulator, which prevents the driven device's gate voltage exceeding its maximum gate-source rating. The gate drive voltage also features Undervoltage Lockout (UVLO) protection that ignores the inputs (IN/INB) and keeps OUTL turned on to ensure the GaN FET is in an OFF state whenever V_{DRV} is below the UVLO threshold. The inputs of the ISL73040SEH can withstand voltages up to 14.7V. The split outputs of the ISL73040SEH offer the flexibility to adjust the turn-on and turn-off speed independently by adding impedance in the turn-on and turn-off paths.

The ISL73040SEH operates across the -55°C to +125°C temperature range and is offered in an 8 Ld hermetically sealed ceramic Surface Mount Device (SMD) package or in die form. The part is implemented in the Renesas P6 power management and mixed signal process, a junction-isolated 5V BiCMOS flow with added high voltage DMOS devices. The fabrication process is QML certified and is in volume commercial production.

Related Literature

- MIL-STD-883 Test Method 1019.
- For a full list of related documents, visit our website
  - ISL73040SEH product page

1. Test Description

1.1 Irradiation Facilities

Low dose rate testing was performed at 0.01rad(Si)/s using the Renesas Palm Bay Hopewell Designs N40 panoramic gamma ray irradiator. Biased irradiation and annealing were performed on all samples following irradiation, using the "Appendix" on page 15 bias configuration at +100ºC for 168 hours in a small temperature chamber.

1.2 Test Fixturing

The Appendix shows the configuration used for biased irradiation.

1.3 Characterization Equipment and Procedures

All electrical testing was performed at room temperature outside the irradiator, using production Automated Test Equipment (ATE) with datalogging to SMD 5962-17233 limits at each downpoint.

1.4 Experimental Matrix

Irradiation was performed in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 12 samples irradiated at low dose rate under bias, and 12 samples irradiated at low dose rate with all pins grounded. Three control units were used.

The ISL73040SEH samples were drawn from wafer lot 5VAFB. All samples were packaged in the hermetic 6mm x 6mm 8 Ld surface mount package (package code J8.A). Samples were processed through the standard burn-in cycle before irradiation.

1.5 Downpoints

Downpoints for the tests were 0, 10, 30, 50, and 75krad(Si). All irradiations were followed by a 168-hour high temperature biased anneal at +100ºC.

2. Test Results

2.1 Attributes Data

Table 1. ISL73040SEH Total Dose Test Attributes Data

Part	Dose Rate (rad(Si)/s)	Bias	Sample Size	Downpoint	Pass (Note 1)	Fail
ISL73040SEH	0.01	"Appendix" on page 15	12	Pre-irradiation	12	0
				10krad(Si)	12	0
				30krad(Si)	12	0
				50krad(Si)	12	0
				75krad(Si)	12	0
				Anneal	12	0
ISL73040SEH	0.01	Grounded	12	Pre-irradiation	12	
				10krad(Si)	12	0
				30krad(Si)	12	0
				50krad(Si)	12	0
				75krad(Si)	12	0
				Anneal	12	0

Note:
1. 'Pass' indicates a sample that passes all pre- and post-irradiation SMD limits.

2.2 Critical Parameter Listing

Table 2 lists 17 critical parameters that are considered indicative of part performance. These parameters are discussed in detail below, including the SMD parameter names for clarity, and are plotted in Figures 1 through 17. All parametric limits are in accordance with the ISL73040SEH SMD pre- and post-irradiation limits, which are identical.

Table 2. Critical Parameters

Figure	Parameter	Limit Low	Limit High	Units	Notes
1	Quiescent Power Supply Current	-	2.5	mA	4.5V supply
		-	2.5	mA	13.2V supply
2	Operating Supply Current	-	13.0	mA	4.5V supply, 500kHz
		-	15.0	mA	13.2V supply, 500kHz
3	Output Voltage	4.29	-	V	4.5V supply
		4.34	4.71	V	13.2V supply
4	Input HIGH Level Threshold	-	2.0	V	4.5V supply
		-	2.0	V	13.2V supply
5	Input LOW Level Threshold	1.0	-	V	4.5V supply
		1.0	-	V	13.2V supply
6	Input B HIGH Level Threshold	-	2.0	V	4.5V supply
		-	2.0	V	13.2V supply
7	Input B LOW Level Threshold	1.0	-	V	4.5V supply
		1.0	-	V	13.2V supply

Table 2. Critical Parameters (Continued)

Figure	Parameter	Limit Low	Limit High	Units	Notes
8	Output Rise Time	21	90	ns	C_L = 10,000pF
9	Output Fall Time	16	50	ns	C_L = 10,000pF
10	Input to Output Turn-On Propagation Delay	15	65	ns	C_L = 1,000pF
11	Input to Output Turn-Off Propagation Delay	15	65	ns	C_L = 1,000pF
12	Input B to Output Turn-On Propagation Delay	15	65	ns	C_L = 1,000pF
13	Input B to Output Turn-Off Propagation Delay	15	65	ns	C_L = 1,000pF
14	Input to Output Propagation Delay Match	-8	8	ns	
15	Input B to Output Propagation Delay Match	-8	8	ns	
16	Driver Output Resistance	-	3.2	Ω	IOUTH = 45mA
17	Driver Output Resistance	-	1.0	Ω	OUTH = V_{DRV}, IOUTL = -45mA
		-	3.0	Ω	OUTH = OUTL, IOUTL = -45mA

Figure 1 on page 5 plots the quiescent power supply current (I_{DDQ}) for the 4.5V supply and 13.2V supply cases.

Figure 2 on page 5 plots the operating power supply current (I_{DDO}) for the 4.5V supply and 13.2V supply cases.

Figure 3 on page 6 plots the output voltage (V_{DRV}) for the 4.5V supply and 13.2V supply cases.

Figure 4 on page 6 and Figure 5 on page 7 plot the input HIGH and LOW (V_{IH} and V_{IL}) logic threshold voltages for the 4.5V supply and 13.2V supply cases.

Figure 6 on page 7 and Figure 7 on page 8 plot the input B HIGH and LOW (V_{IH} and V_{IL}) logic threshold voltages for the 4.5V supply and 13.2V supply cases.

Figure 8 on page 8 and Figure 9 on page 9 plot the 10% to 90% output rise and fall times (t_{RISE} and t_{FALL}) with a 10nF load capacitance.

Figure 10 on page 9 and Figure 11 on page 10 plot the input to output turn-on and turn-off propagation delays (t_{DON} and t_{DOFF}).

Figure 12 on page 10 and Figure 13 on page 11 plot the input B to output turn-on and turn-off propagation delays (t_{DON} and t_{DOFF}).

Figure 14 on page 11 plots the input to output turn-on and turn-off propagation delay match (t_{DM}).

Figure 15 on page 12 plots the input B to output turn-on and turn-off propagation delay match (t_{DM}).

Figure 16 on page 12 plots the driver output resistance (r_{ONP}) with the HIGH output current at 45mA.

Figure 17 on page 13 plots the driver output resistance (r_{ONN}) with the HIGH output at V_{DRV} and the HIGH output at the LOW output cases, both with the LOW output current at -45mA.

2.3 Critical Parameter Variables Data

The plots in Figures 1 through 17 show the TID response of the critical parameters outlined in "Critical Parameter Listing" on page 3. The figures plot the average only because the data was tightly grouped.

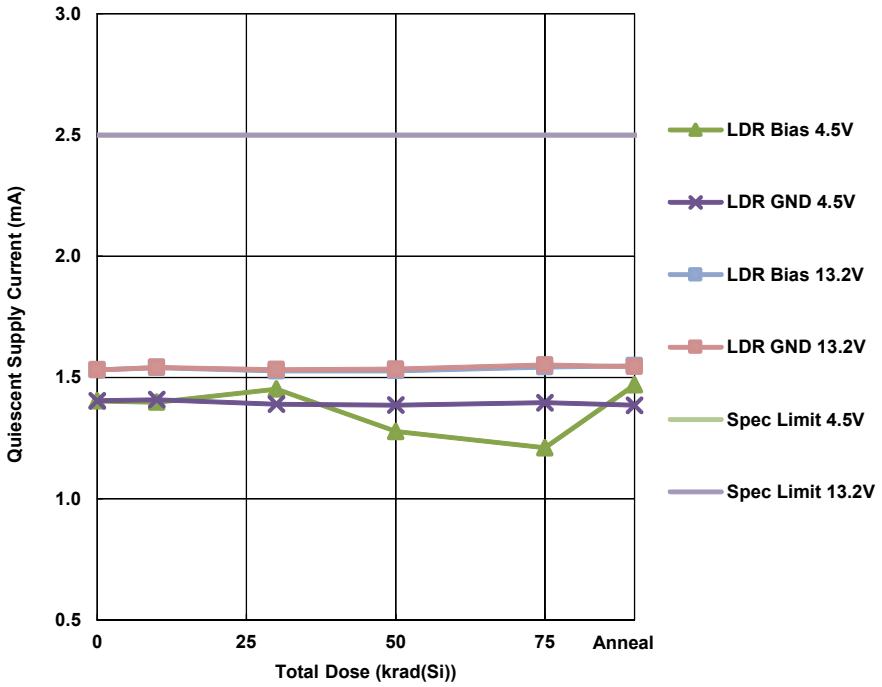

Figure 1. ISL73040SEH quiescent power supply current (I_{DDQ}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per "Appendix" on page 15) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limit is 2.5mA maximum (4.5V supply and 13.2V supply).

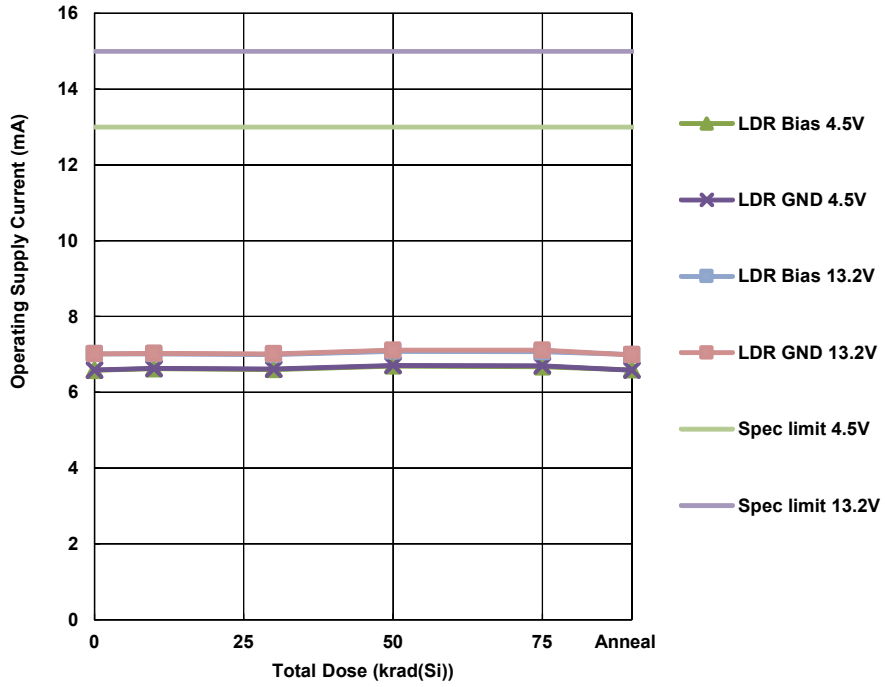

Figure 2. ISL73040SEH operating (500kHz) power supply current (I_{DDO}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 13mA maximum (4.5V supply) and 15mA maximum (13.2V supply).

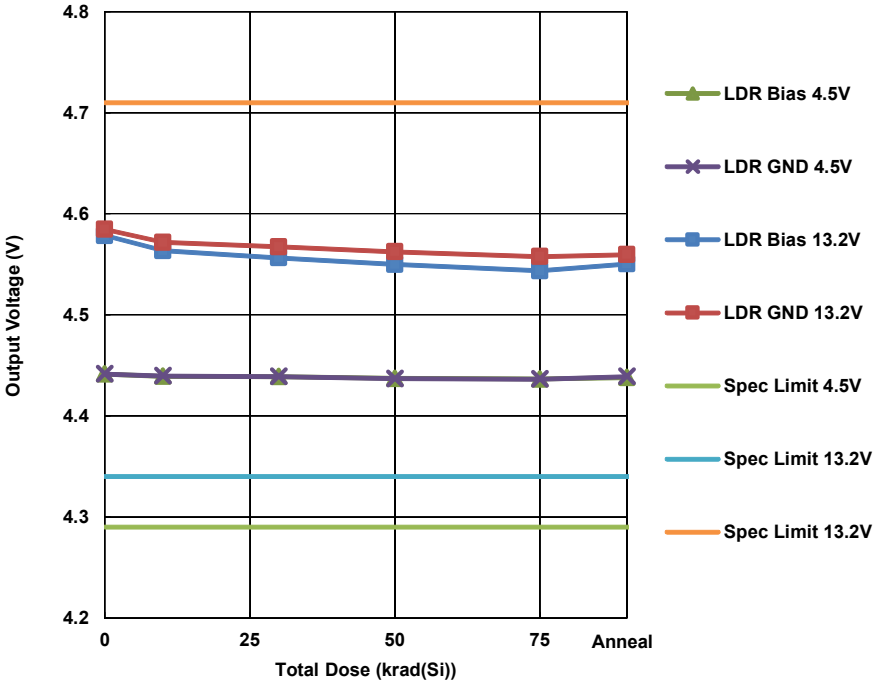

Figure 3. ISL73040SEH output voltage (V_{DRV}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 4.29V minimum (4.5V supply) and 4.34V to 4.71V (13.2V supply).

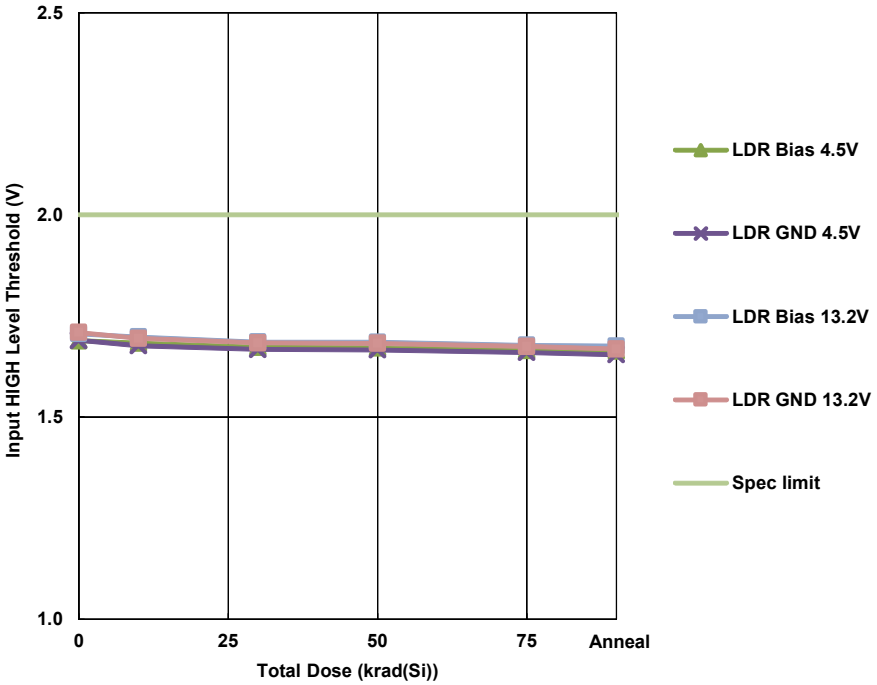

Figure 4. ISL73040SEH input HIGH level threshold (V_{IH}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limit is 2.0V maximum (4.5V supply and 13.2V supply).

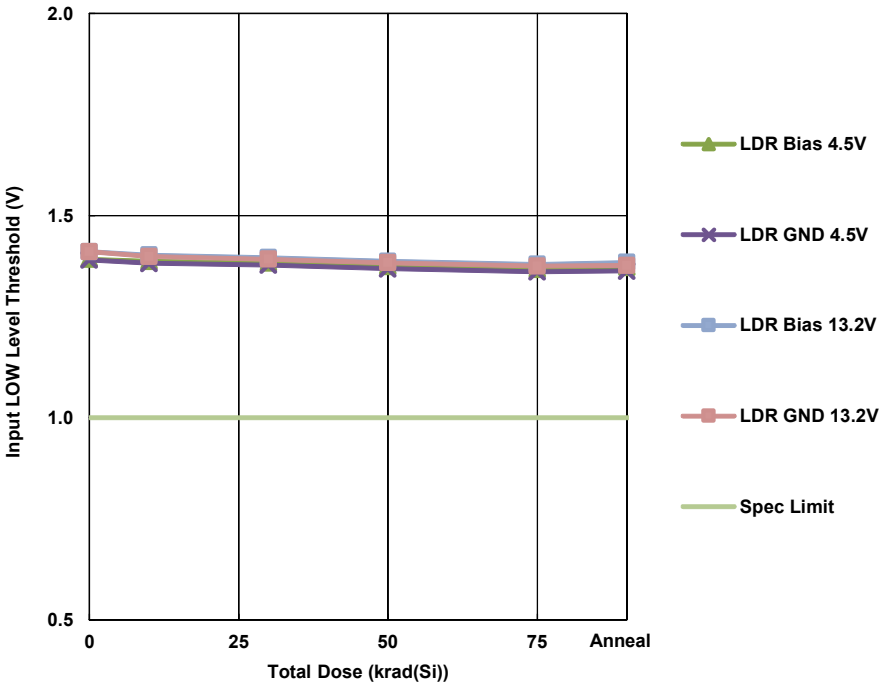

Figure 5. ISL73040SEH input LOW level threshold (V_{IL}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 1.0V minimum (4.5V supply and 13.2V supply).

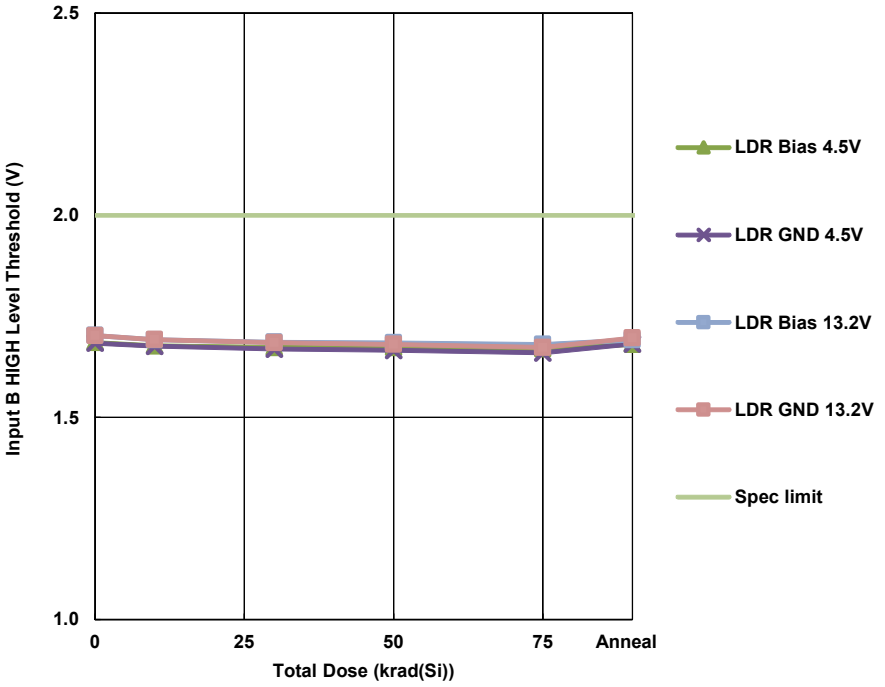

Figure 6. ISL73040SEH input B HIGH level threshold (V_{IH}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limit is 2.0V maximum (4.5V supply and 13.2V supply).

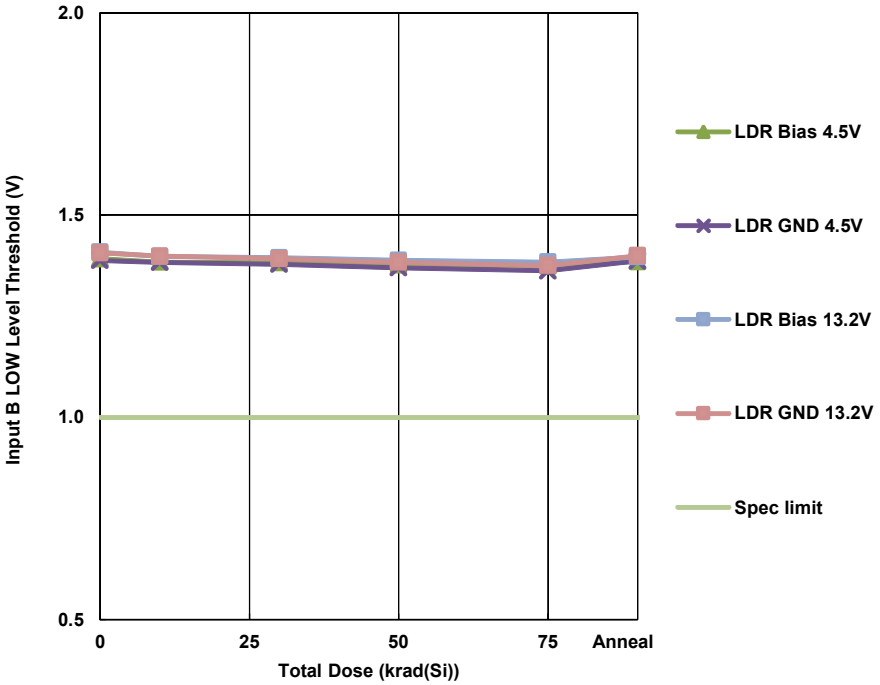

Figure 7. ISL73040SEH input B LOW level threshold (V_{IL}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limit is 1.0V minimum (4.5V supply and 13.2V supply).

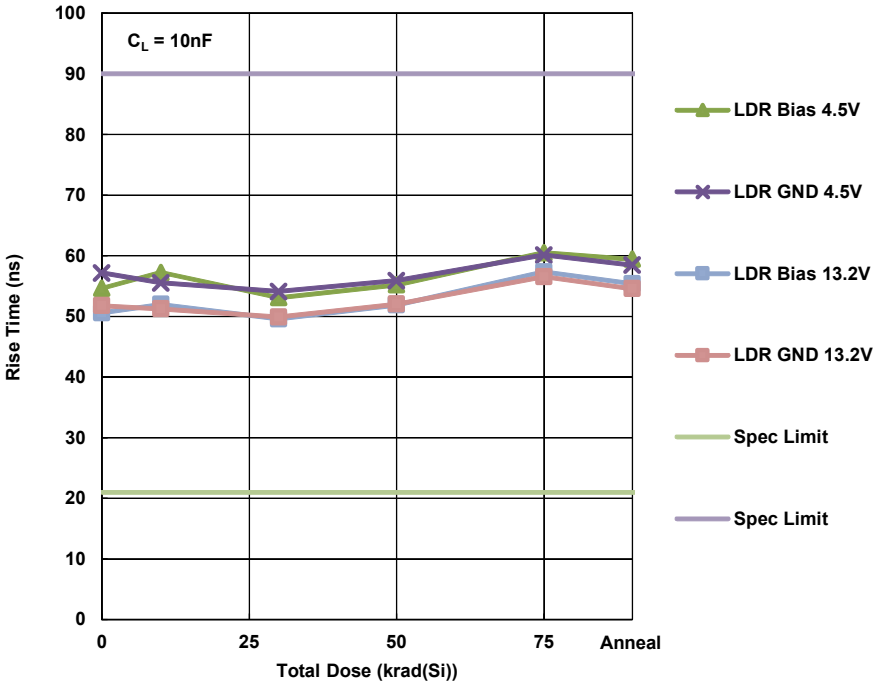

Figure 8. ISL73040SEH rise time (t_{RISE}) as a function of total dose irradiation, 10nF load capacitance, for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 21ns to 90ns.

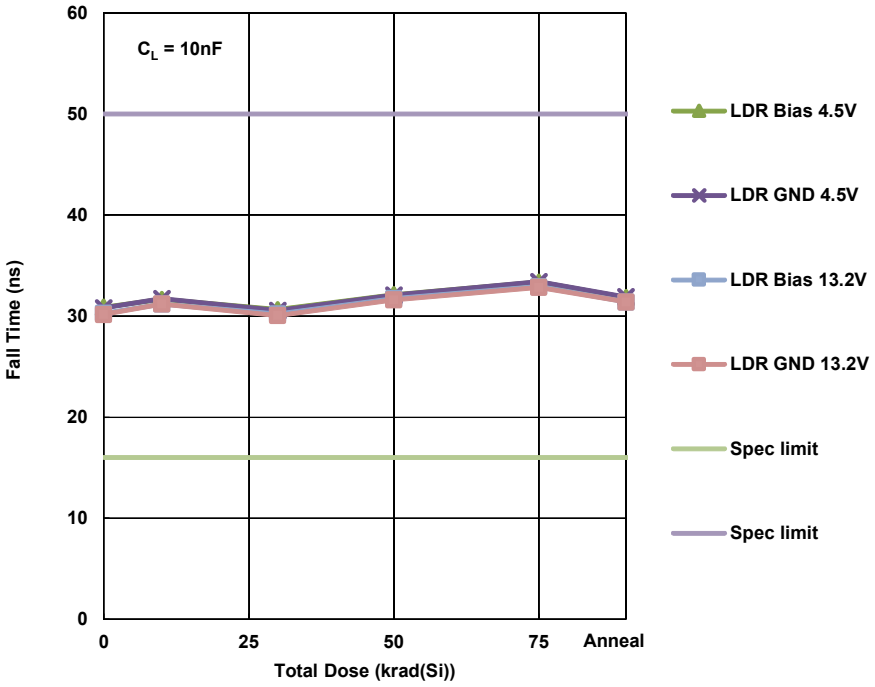

Figure 9. ISL73040SEH fall time (t_{FALL}) as a function of total dose irradiation, 10nF load capacitance, for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 16ns to 50ns.

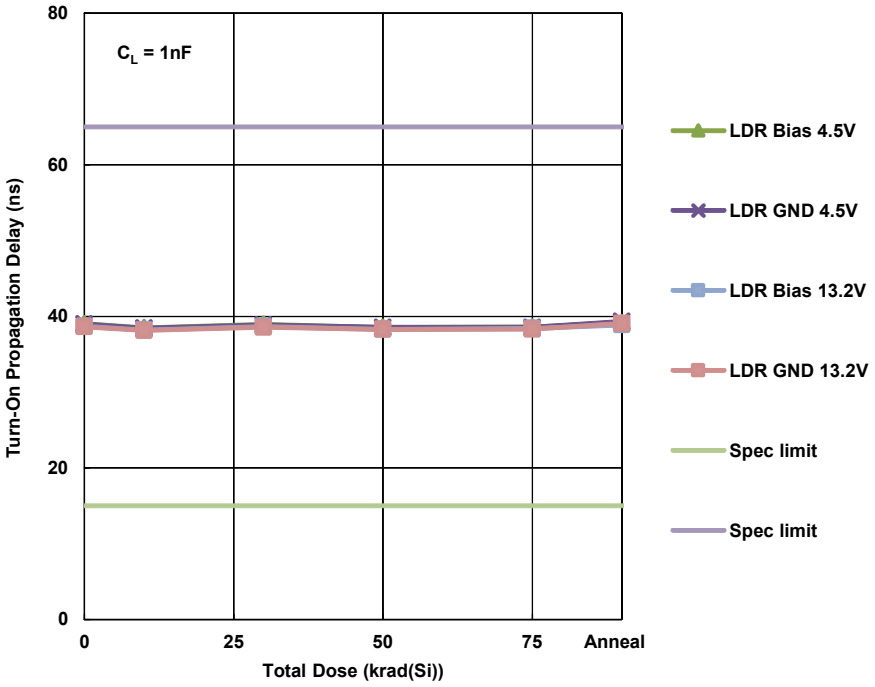

Figure 10. ISL73040SEH input to output turn-on propagation delay (t_{DON}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 15ns to 65ns.

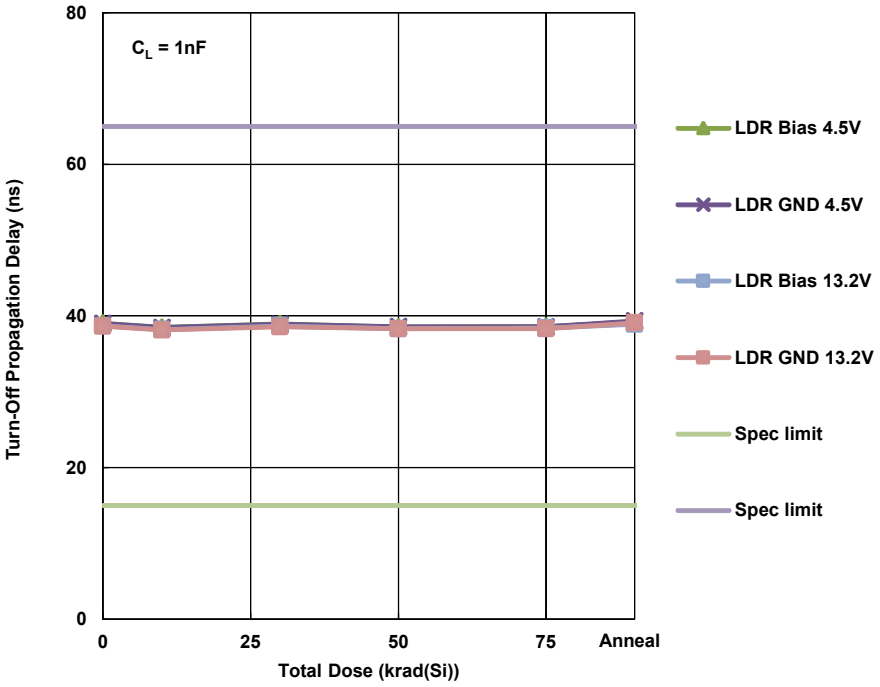

Figure 11. ISL73040SEH input to output turn-off propagation delay (t_{DOFF}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 15ns to 65ns.

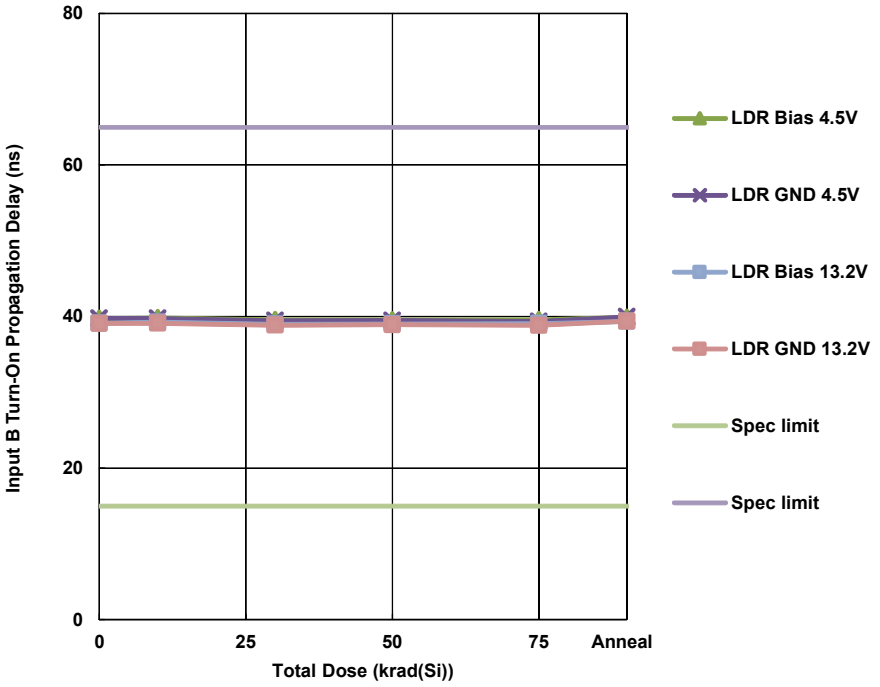

Figure 12. ISL73040SEH input B to output turn-on propagation delay (t_{DON}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 15ns to 65ns.

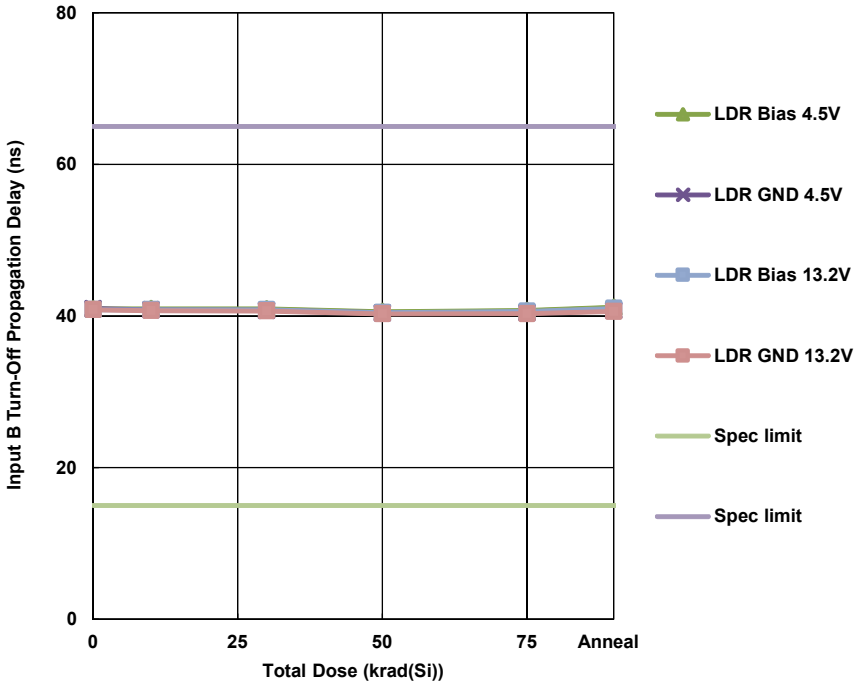

Figure 13. ISL73040SEH input B to output turn-off propagation delay (t_{DOFF}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 15ns to 65ns.

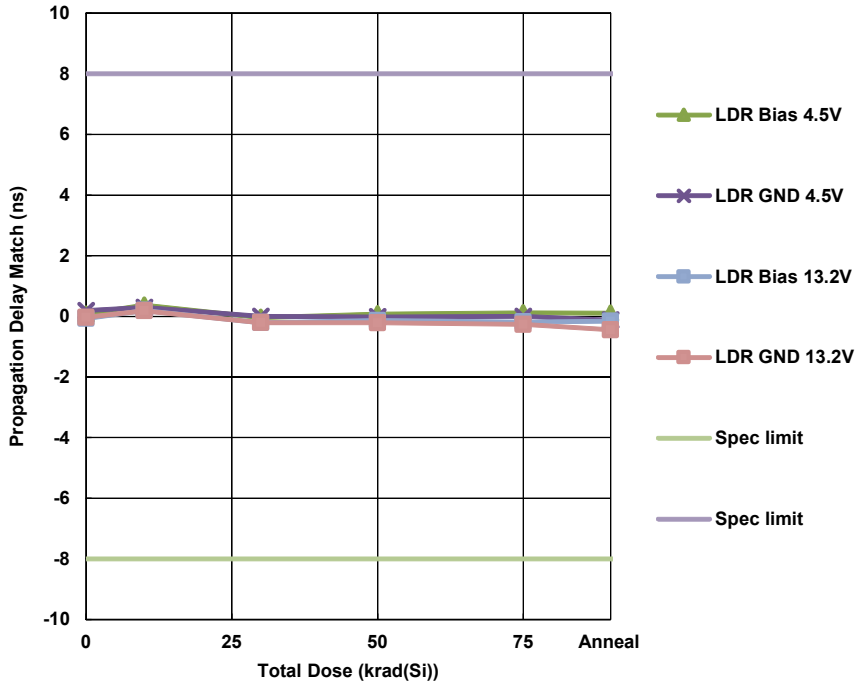

Figure 14. ISL73040SEH input to output propagation delay match (t_{DM}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are -8ns to 8ns.

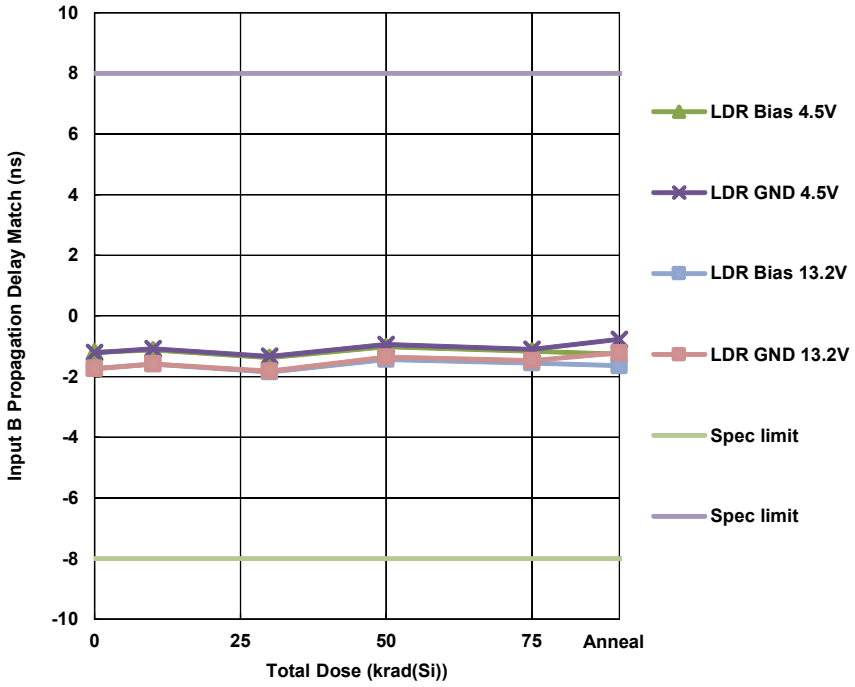

Figure 15. ISL73040SEH input B to output propagation delay match (t_{DM}), 4.5V and 13.2V supply, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are -8ns to 8ns.

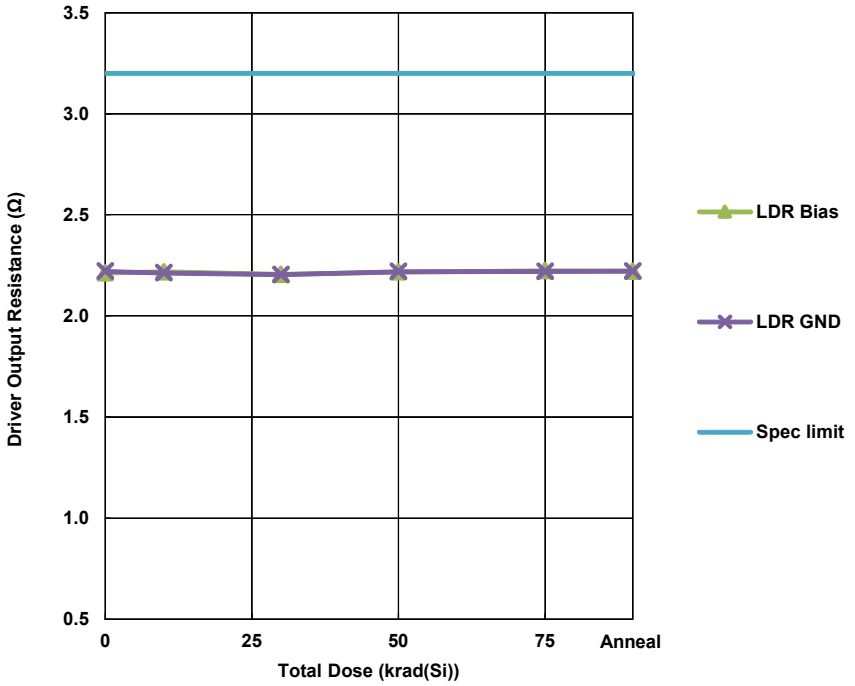

Figure 16. ISL73040SEH driver output resistance (r_{ONP}), output HIGH current 45mA, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limit is 3.2Ω maximum.

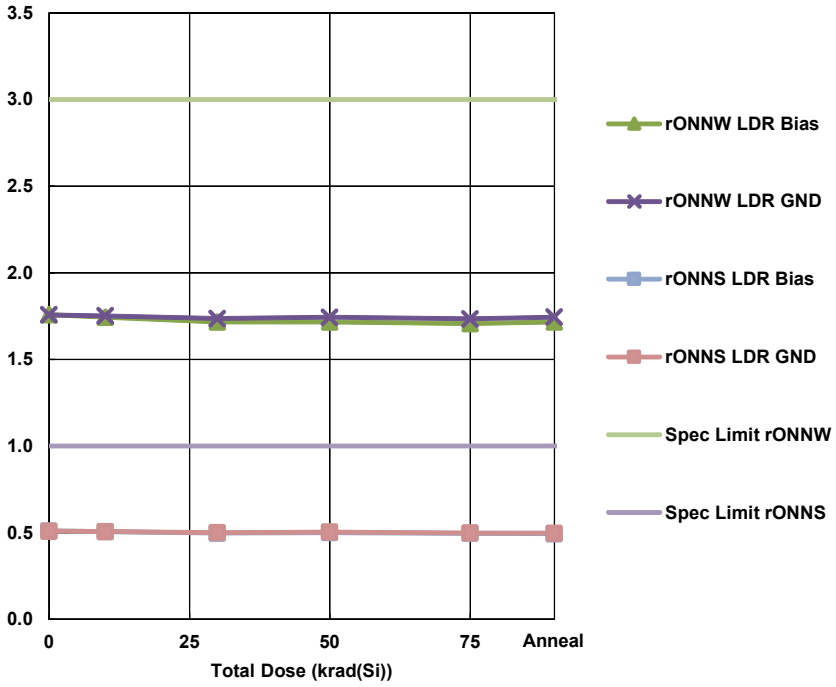

Figure 17. ISL73040SEH driver output resistance (r_{ONN}), output LOW current -45mA, HIGH output at V_{DRV} and at OUTL cases, as a function of total dose irradiation for the biased (per Appendix) and unbiased (all pins grounded) cases, plotting the average. The dose rate was 0.01rad(Si)/s. The irradiations were followed by a +100°C 168-hour biased anneal. The sample size of all cells was 12. The SMD limits are 1.0Ω maximum (OUTH = V_{DRV}) and 3.0Ω (OUTH = OUTL).

3. Discussion and Conclusion

The results of a low dose rate biased and grounded total dose test of the ISL73040SEH radiation tolerant low side GaN FET driver were reported. All irradiations were followed by a 168-hour anneal at +100ºC under bias. “Attributes Data” on page 3 summarizes the attributes data for the test. “Critical Parameter Listing” on page 3 summarizes the 17 critical parameters for the part. Finally, “Critical Parameter Variables Data” on page 4 provides plots of the total dose and anneal response for these critical parameters.

All parameters remained well within the SMD limits at all downpoints and showed no differences between biased and unbiased irradiation. This leads to the conclusion that the part is not bias sensitive.

4. Appendix

The ISL73040SEH uses the ISL70040SEH irradiation and anneal bias configuration, see Figure 18.

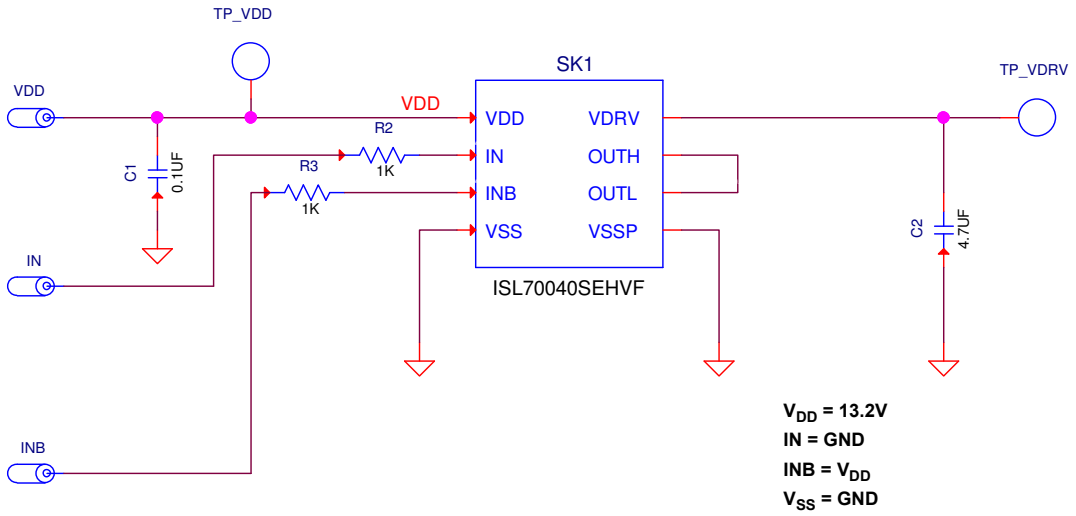

Figure 18. ISL73040SEH Irradiation and Anneal Bias Configuration

5. Revision History

Rev.	Date	Description
0.00	Jan 15, 2018	Initial release

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