ISL71830SEH

Total Dose Testing

TR020
Rev 0.00
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Introduction

This report summarizes the results of a total dose test of the ISL71830SEH 16-channel low voltage analog multiplexer. The test was conducted in order to determine the sensitivity of the part to the total dose environment. Irradiation under bias and with all pins grounded and subsequent high temperature anneals are complete.

Reference Documents

- MIL-STD-883 test method 1019
- ISL71830SEH datasheet.
- DLA Land and Maritime Standard Microcircuit Drawing (SMD) 5962-15247

Part Description

The ISL71830SEH is a radiation tolerant 16-channel analog multiplexer that is fabricated using Intersil's proprietary P6SOI (Silicon on Insulator) process technology to provide excellent latch-up performance. The part operates over a single supply range from 3.3V to 5V and has four digital address inputs plus an enable pin that can be driven with adjustable logic thresholds to select one of 16 available channels. Inactive channels are isolated from the active channel by a high impedance, which inhibits any interaction between them.

The ISL71830SEH's low switch ON-resistance allows improved signal integrity and reduced power losses. The ISL71830SEH is also designed for cold sparing making it compatible with redundancy techniques in high reliability applications. The part is designed to provide a high impedance to the analog source in a powered OFF condition, making it easy to add additional backup devices without incurring extra power dissipation. The ISL71830SEH also has analog overvoltage protection on the switch inputs that disables the switch during an overvoltage event to protect upstream and downstream devices. All inputs are Electrostatic Discharge (ESD) protected to 5kV Human Body Model (HBM).

The ISL71830SEH is available in a 28 Ld Ceramic Dual Flatpack (CDFP) and operates over the extended temperature range of -55°C to +125°C. The ISL71831SEH is a 32-channel version of the ISL71830SEH and is available in a 48 Ld Ceramic Quad Flatpack (CQFP); please refer to the ISL71831SEH datasheet for further information.

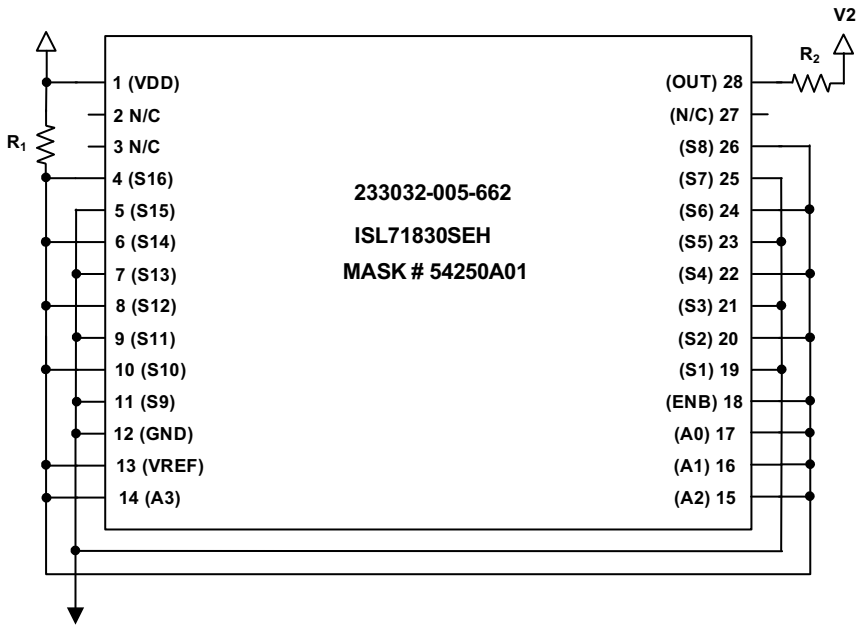
Test Description

Irradiation Facilities

Irradiation was performed using a Hopewell Designs N40 panoramic low dose rate ^{60}Co irradiator located in the Palm Bay, Florida Intersil facility. The irradiations were performed at 8.554mrad(Si)/s to 9.322mrad(Si)/s in accordance with MIL-STD-883 Test Method 1019. A PbAl box was used to shield the test board and devices under test against low energy secondary gamma radiation. The high temperature anneal was performed under bias at +100°C for 168 hours.

Test Fixturing

Figure 1 on page 2 shows the configuration and power supply sequencing used for biased irradiation.



1. V1 = +5.5V, ±0.1V
2. V2 = +2.75V, ±0.1V
3. R_1 and R_2 = 1Ω, ±5%, ¼ Watt (Per socket)
4. Socket is 28 pin flatpack (Sensata 628-0282315
5. Power-on sequence is V1 followed by V2
6. Power-off sequence is V2 then V1

FIGURE 1. IRRADIATION BIAS CONFIGURATION AND POWER SUPPLY SEQUENCING FOR THE ISL71830SEH

Characterization Equipment and Procedures

All electrical testing was performed outside the irradiator using production Automated Test Equipment (ATE) with data logging of all parameters at each downpoint. All downpoint electrical testing was performed at room temperature.

Experimental Matrix

Testing proceeded in accordance with the guidelines of MIL-STD-883 Test Method 1019. The experimental matrix consisted of 16 samples irradiated at low dose rate with all pins grounded and 16 samples irradiated at low dose rate under bias (four control units were used).

Samples of the ISL71830SEH were drawn from development lot J69526 and were packaged in the production hermetic 28-pin ceramic flatpack package outline K28.A. The samples were processed through the standard burn in cycle and were screened to the SMD 5962-15247 limits at room, low and high temperature before irradiation.

Downpoints

Downpoints were zero, 10krad(Si), 30krad(Si), 50krad(Si) and 75krad(Si). All samples were subjected to a high temperature biased anneal for 168 hours at +100°C following irradiation

Results

Attributes Data

Total dose testing of the ISL71830SEH is complete and showed no reject devices after irradiation up to 75krad(Si) or after the post-75krad(Si) irradiation anneal. Table 1 summarizes the results.

TABLE 1. ISL71830SEH TOTAL DOSE TEST ATTRIBUTES DATA

DOSE RATE	BIAS	SAMPLE SIZE	DOWNPOINT	BIN 1 (Note 1)	REJECTS
8.554mrad(Si)/s to 9.322mrad(Si)/s	Figure 1	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal, 168 hours at +100°C (Note 2)	16	0
8.554mrad(Si)/s to 9.322mrad(Si)/s	Grounded	16	Pre-irradiation	16	
			10krad(Si)	16	0
			30krad(Si)	16	0
			50krad(Si)	16	0
			75krad(Si)	16	0
			Anneal, 168 hours at +100°C (Note 2)	16	0

NOTES:

1. Bin 1 indicates a device that passes all pre-irradiation specification limits.
2. The 168 hours anneal was performed at +100°C using the bias configuration shown in Figure 1.

Variables Data

The plots in Figures 2 through 22 show data at all downpoints. The plots show the average of key parameters as a function of total dose for each of the two irradiation conditions. Many of the plots show the total dose response of the average of parameters, such as ON-resistance and the various leakage parameters for each of the 16 channels in order to facilitate the interpretation of the results as well as managing the length of this report. All samples showed excellent stability over irradiation. See the "Conclusion" on page 15 for further discussion.

Variables Data Plots

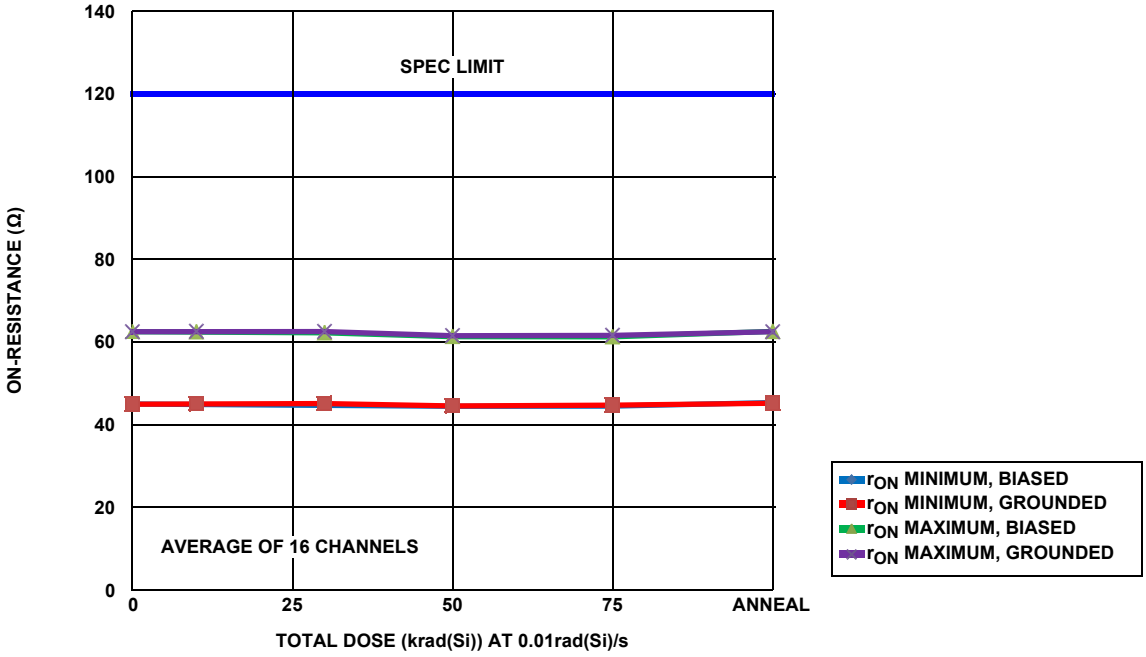


FIGURE 2. ISL71830SEH minimum and maximum switch ON-resistance, average of 16 channels, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 120Ω maximum.

Variables Data Plots (Continued)

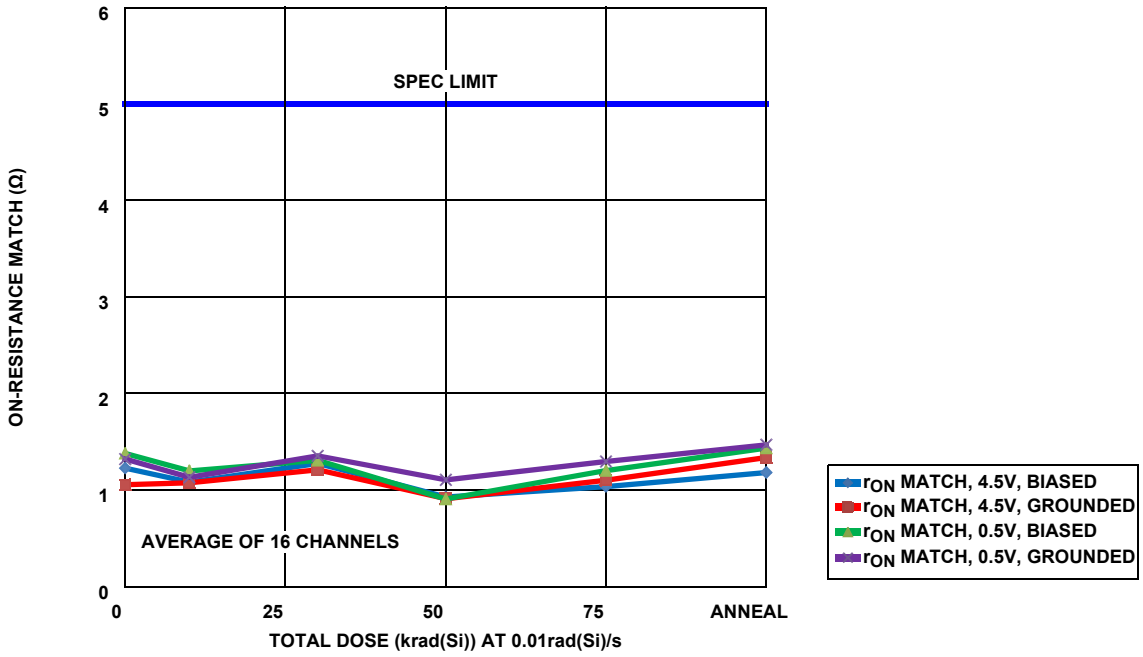


FIGURE 3. ISL71830SEH switch ON-resistance match, average of 16 channels, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 5Ω maximum.

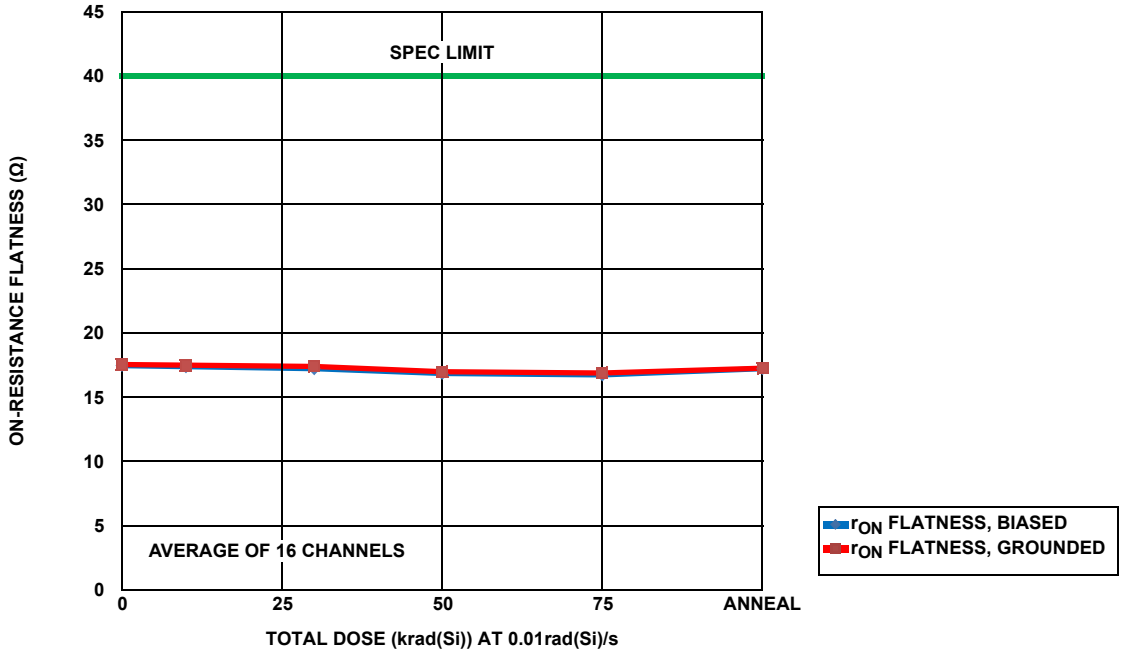


FIGURE 4. ISL71830SEH ON-resistance flatness, average of 16 channels, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 40Ω maximum.

Variables Data Plots (Continued)

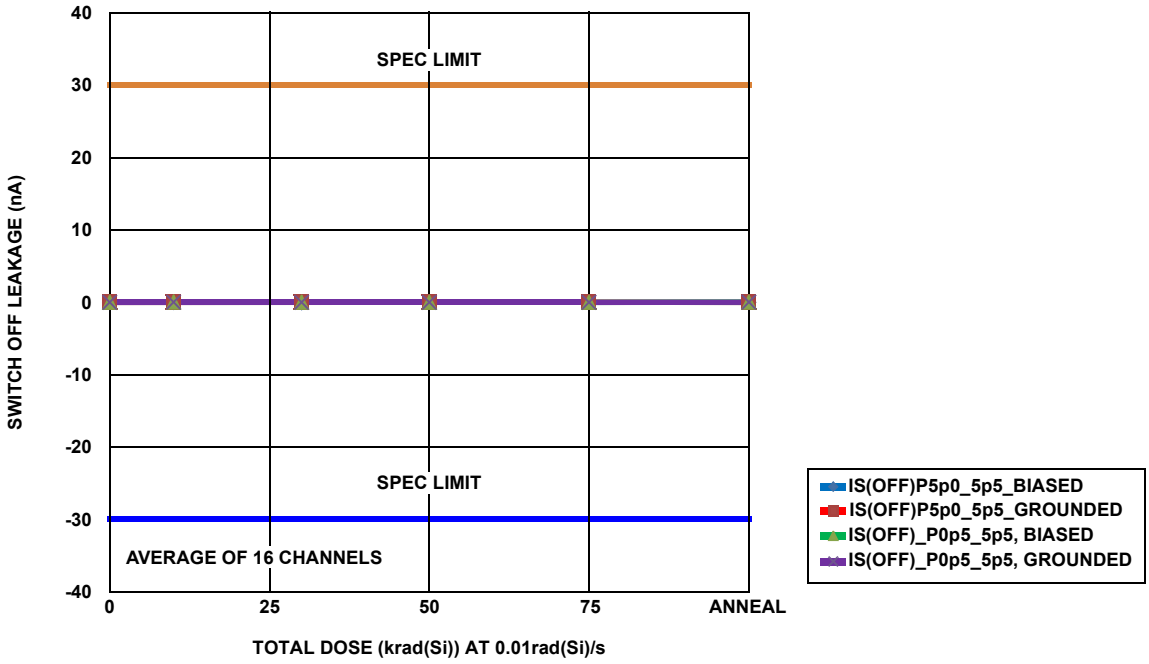


FIGURE 5. ISL71830SEH switch input OFF leakage, average of all 16 channels, 5.5V supply, input voltage to selected switch 5V or 0.5V, output and all unselected inputs at 0.5V, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -30µA to 30µA.

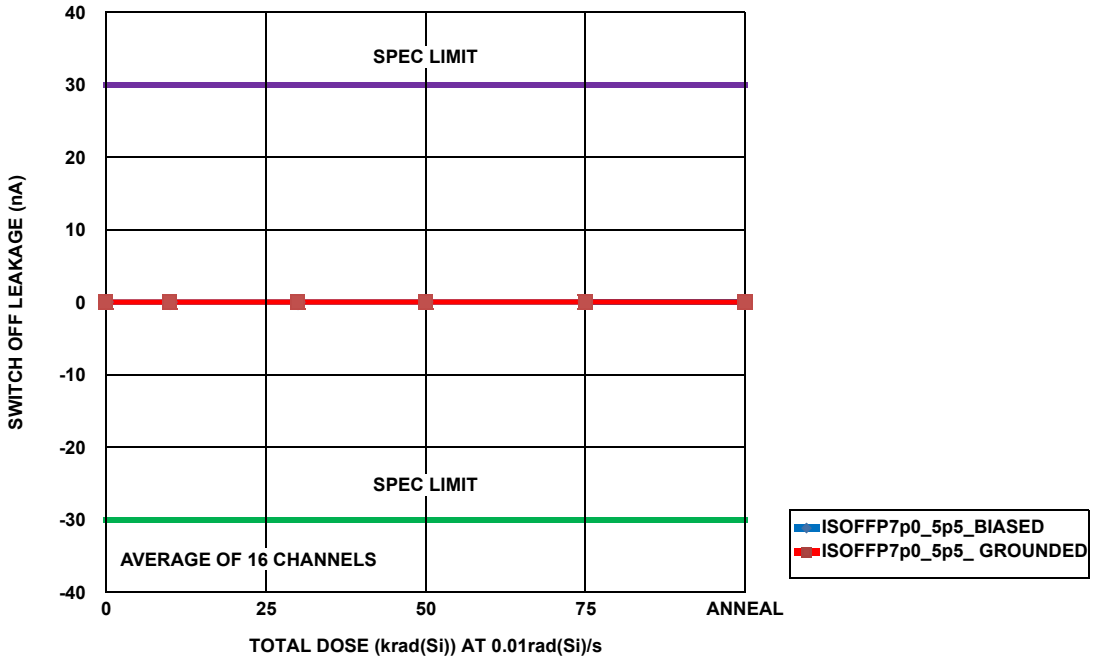


FIGURE 6. ISL71830SEH switch input overvoltage OFF leakage, average of all 16 channels, 5.5V supply, input voltage to selected switch 7V, output and all unselected inputs at 0.0V as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -30µA to 30µA.

Variables Data Plots (Continued)

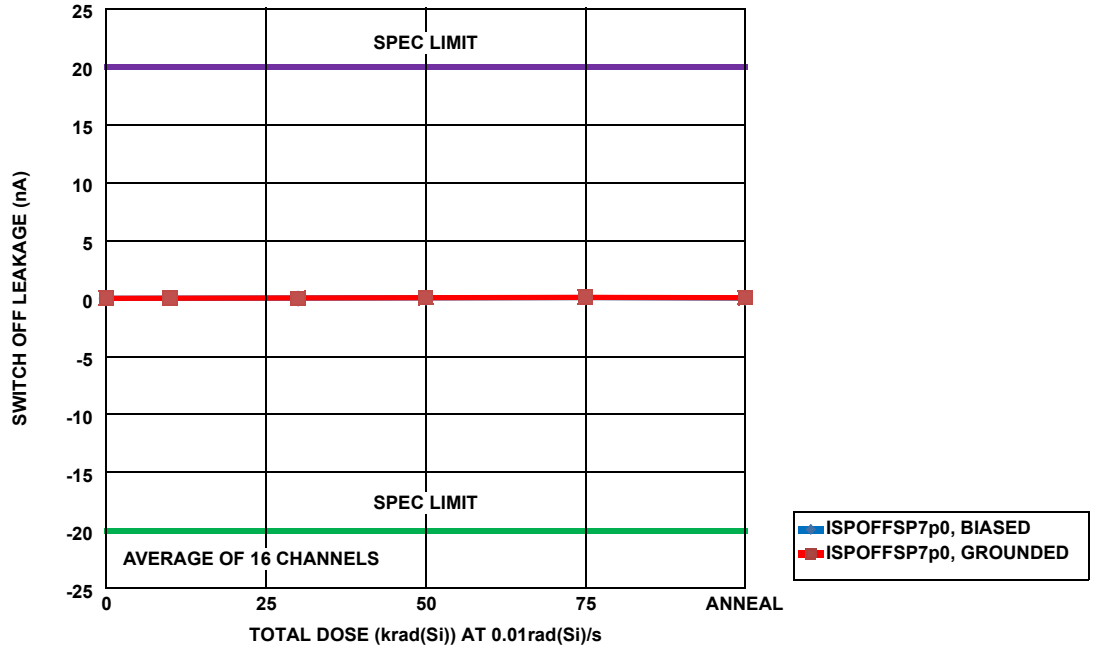


FIGURE 7. ISL71830SEH 'supplies off' switch OFF leakage into the input of an unselected channel, average of all 16 channels, supplies, address pins, enable pin and unselected inputs grounded, input voltage to selected switch 7V as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -20µA to 20µA.

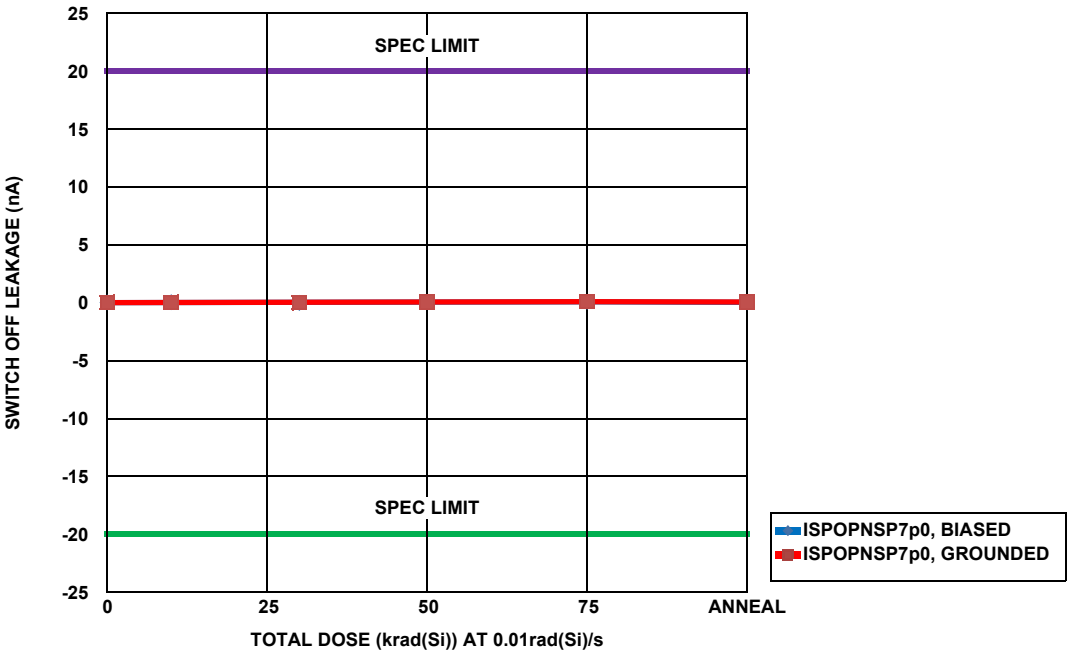


FIGURE 8. ISL71830SEH 'supplies open' switch OFF leakage into the input of an unselected channel, supplies, address pins, enable pin and unselected inputs grounded, input voltage to selected switch 7V and average of all 16 channels, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -20µA to 20µA.

Variables Data Plots (Continued)

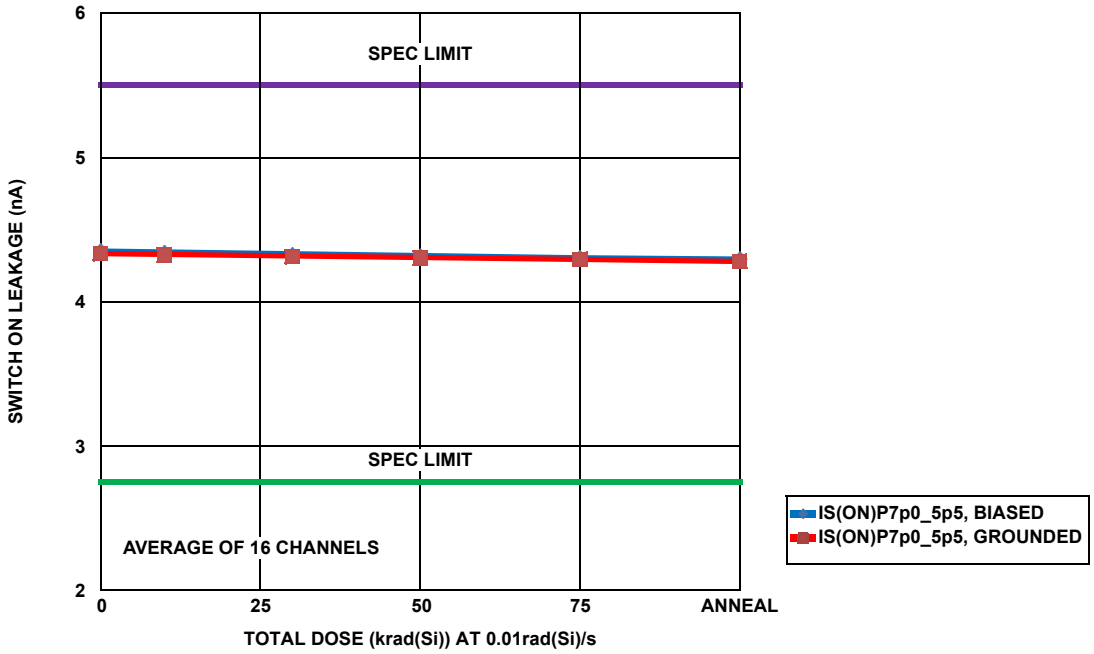


FIGURE 9. ISL71830SEH 'overvoltage' switch ON leakage into a selected channel, average of all 16 channels, 5.5V supply, input voltage to selected switch 7V, output open and unselected inputs at 0.0V, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 2.75µA to 5.5µA.

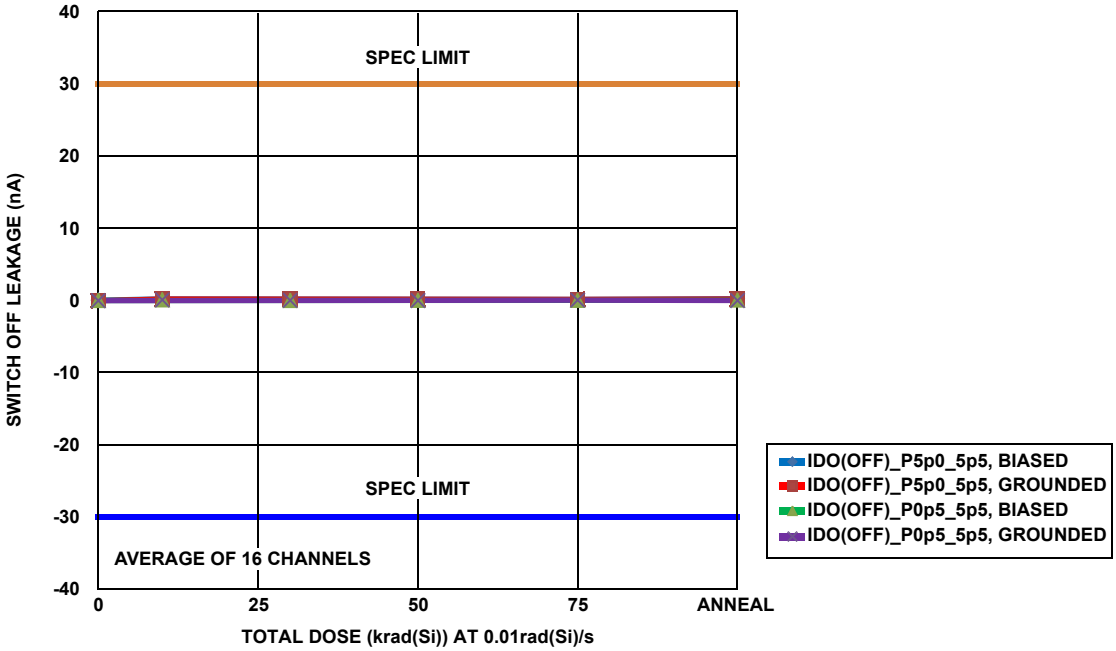


FIGURE 10. ISL71830SEH switch OFF leakage into the multiplexer output, 5.5V supply, input voltage 0.5V or 5V and output voltage 5V or 0.5V as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -30µA to 30µA.

Variables Data Plots (Continued)

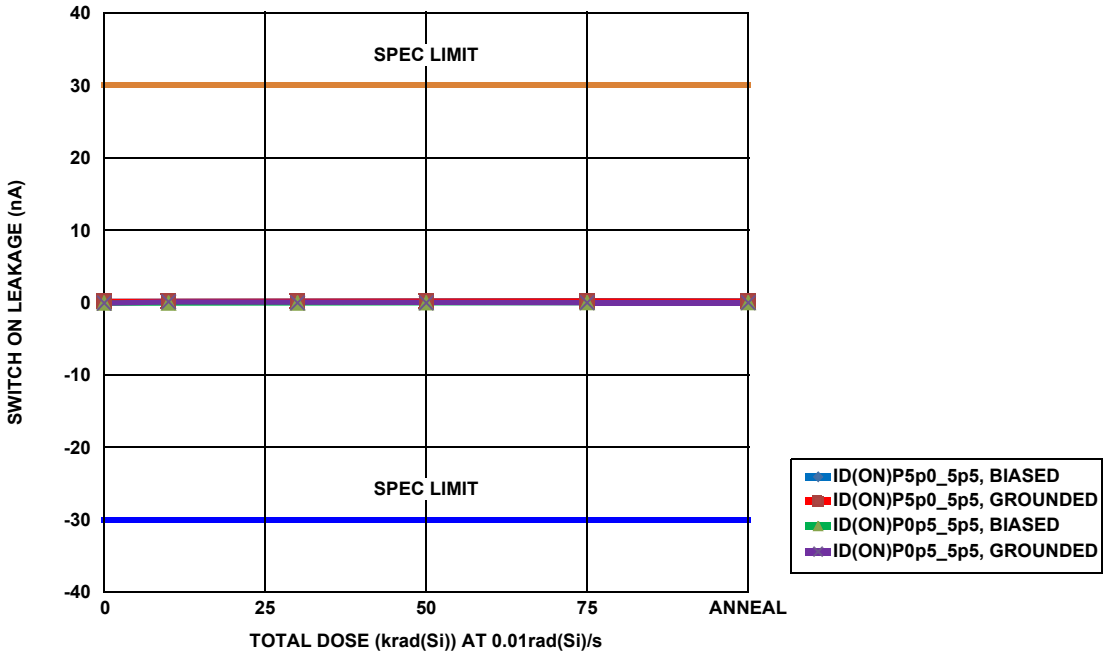


FIGURE 11. ISL71830SEH switch ON leakage into the input and output for a selected switch, average of all 16 channels, 5.5V supply, selected input and output at 0.5V or 5V and unselected inputs at 5V or 0.5V, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is -30µA to 30µA.

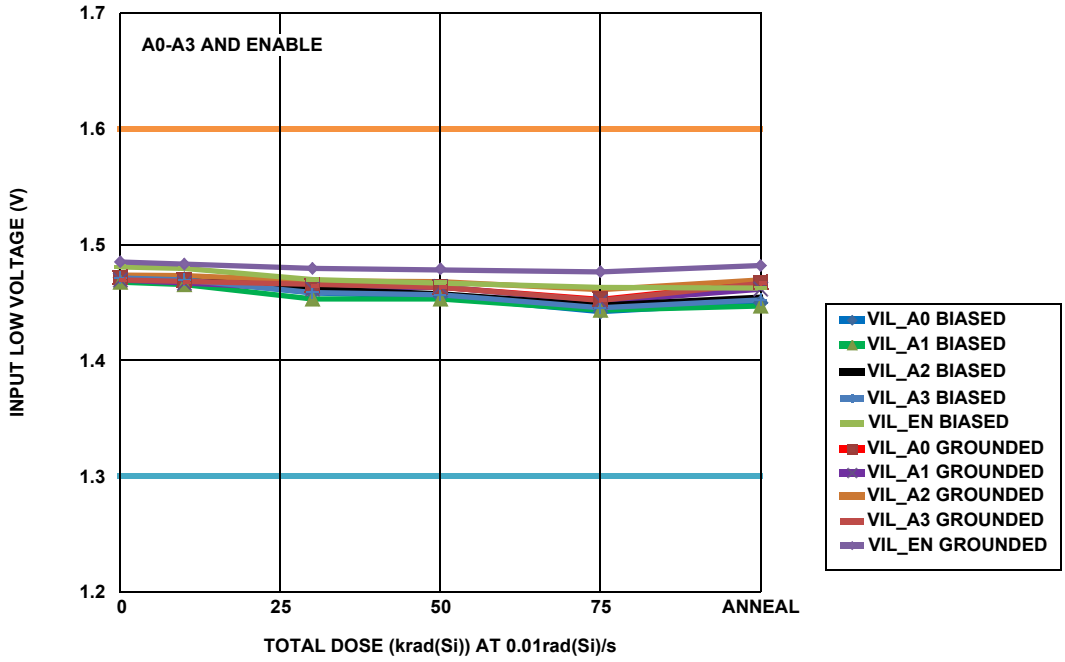


FIGURE 12. ISL71830SEH input LOW voltage, address pins A0 through A3 and Enable pin as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 1.3V to 1.6V.

Variables Data Plots (Continued)

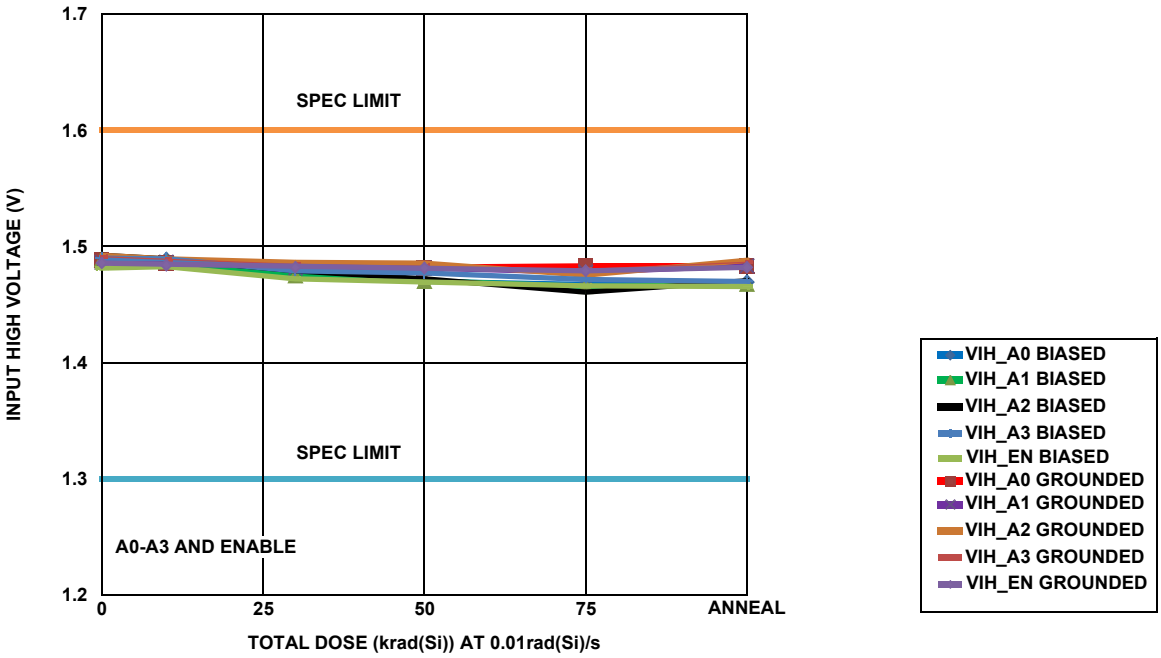


FIGURE 13. ISL71830SEH input HIGH voltage, address pins A0 through A3 and Enable pin, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 1.3V to 1.6V.

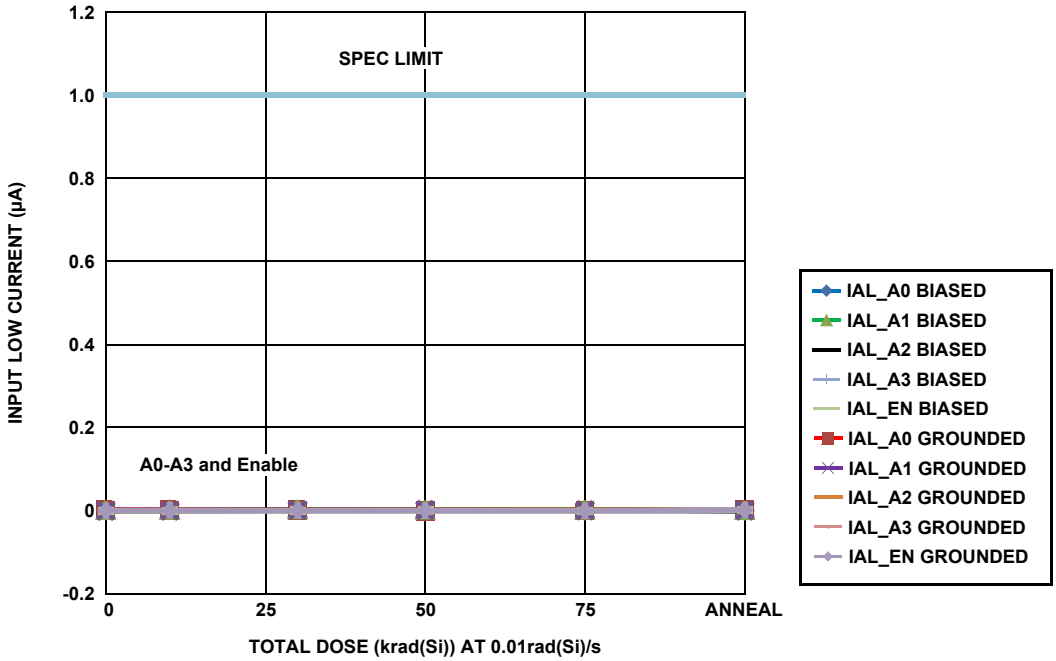


FIGURE 14. ISL71830SEH input LOW current, address pins A0 through A3 and Enable pin, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are -0.1µA to 0.1µA.

Variables Data Plots (Continued)

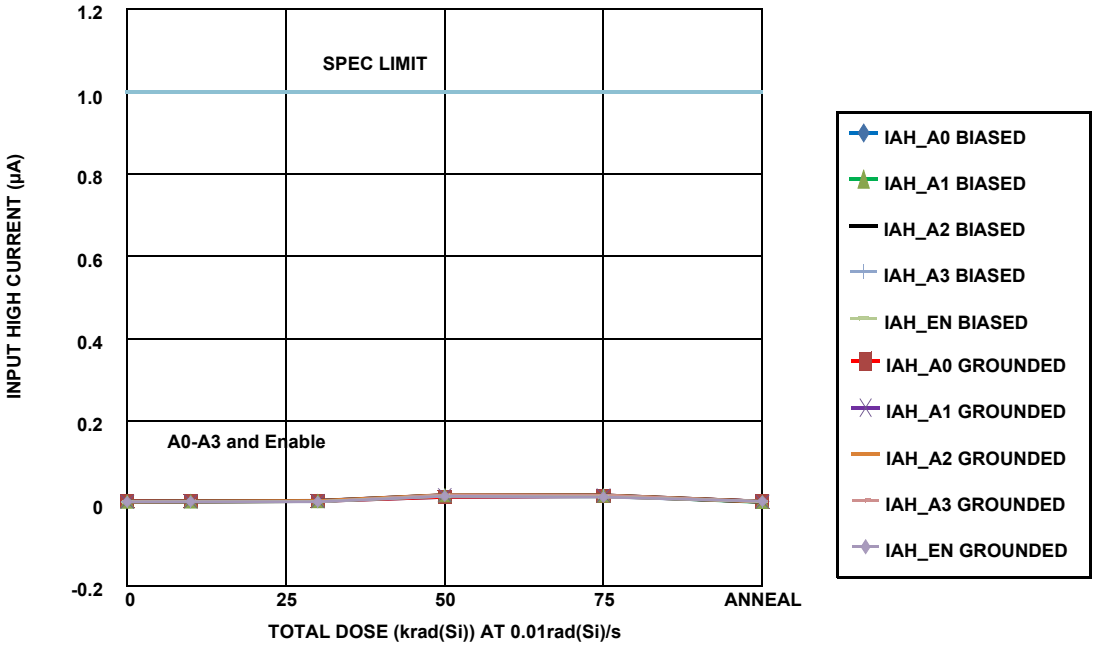


FIGURE 15. ISL71830SEH input HIGH current, address pins A0 through A3 and Enable pin, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are -0.1µA to 0.1µA.

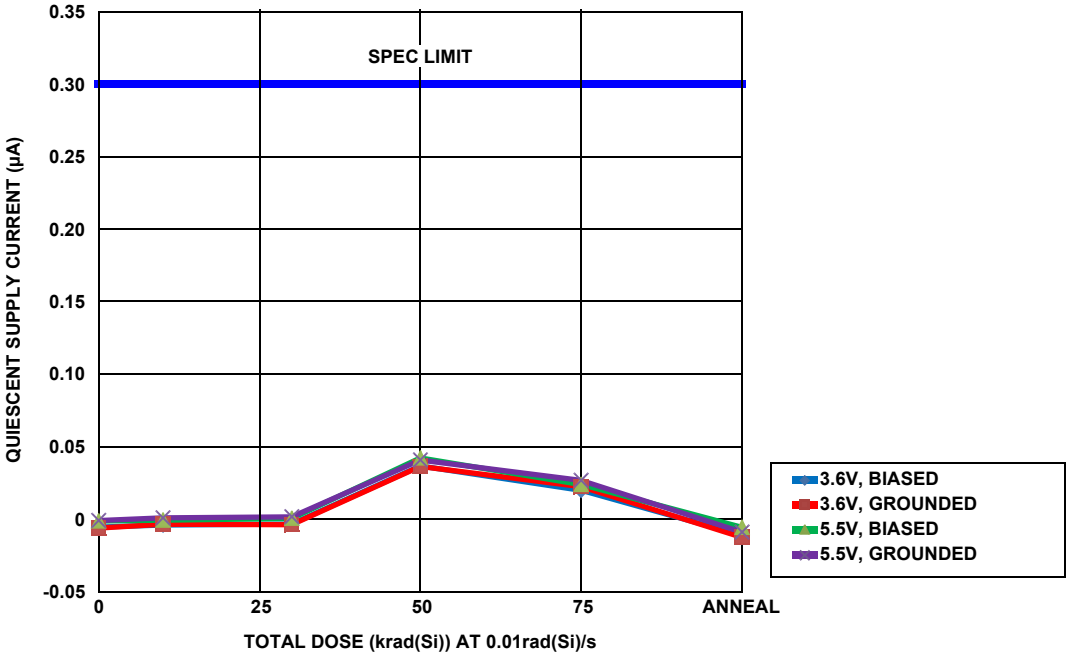


FIGURE 16. ISL71830SEH quiescent supply current, 3.6V and 5.5V supply and V_{REF} voltage, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 0.3µA maximum for both voltages.

Variables Data Plots (Continued)

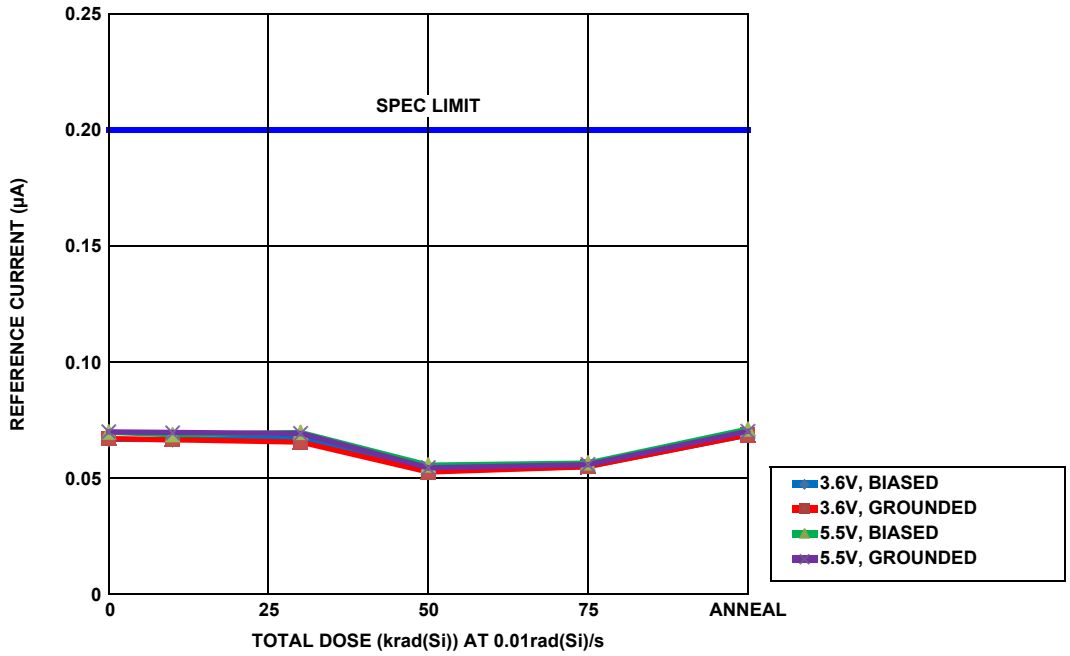


FIGURE 17. ISL71830SEH reference supply current, 3.6V and 5.5V supply and V_{REF} voltage as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limit is 0.2µA maximum for both voltages.

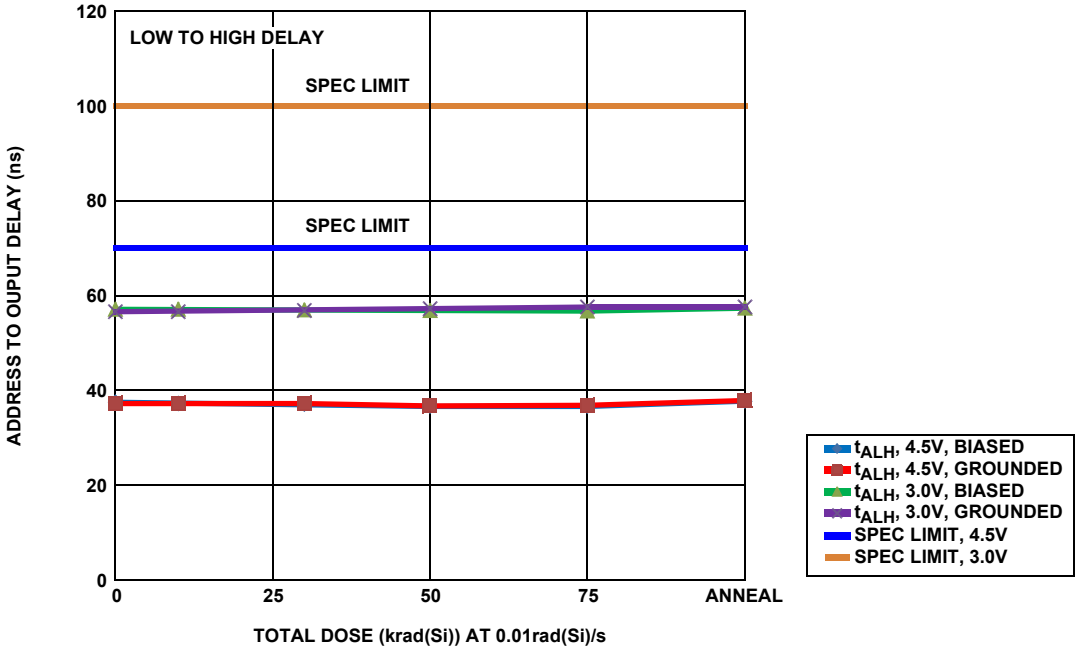


FIGURE 18. ISL71830SEH address input to multiplexer output delay, LOW to HIGH as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 70ns maximum (4.5V) and 100ns maximum (3.0V).

Variables Data Plots (Continued)

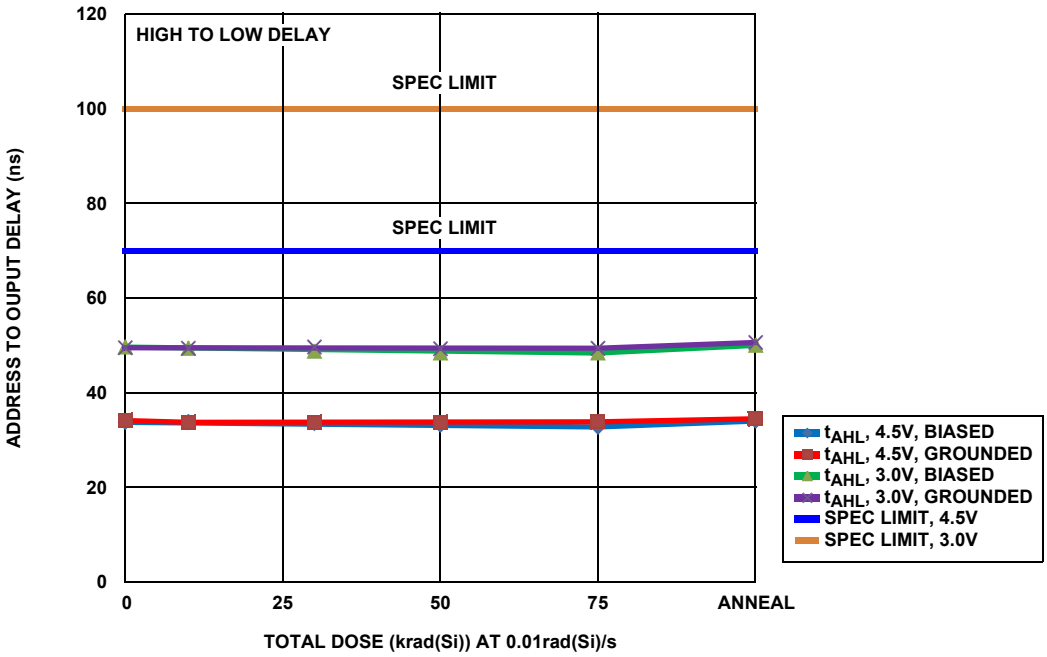


FIGURE 19. ISL71830SEH address input to multiplexer output delay, HIGH to LOW, as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 70ns maximum (4.5V) and 100ns maximum (3.0V).

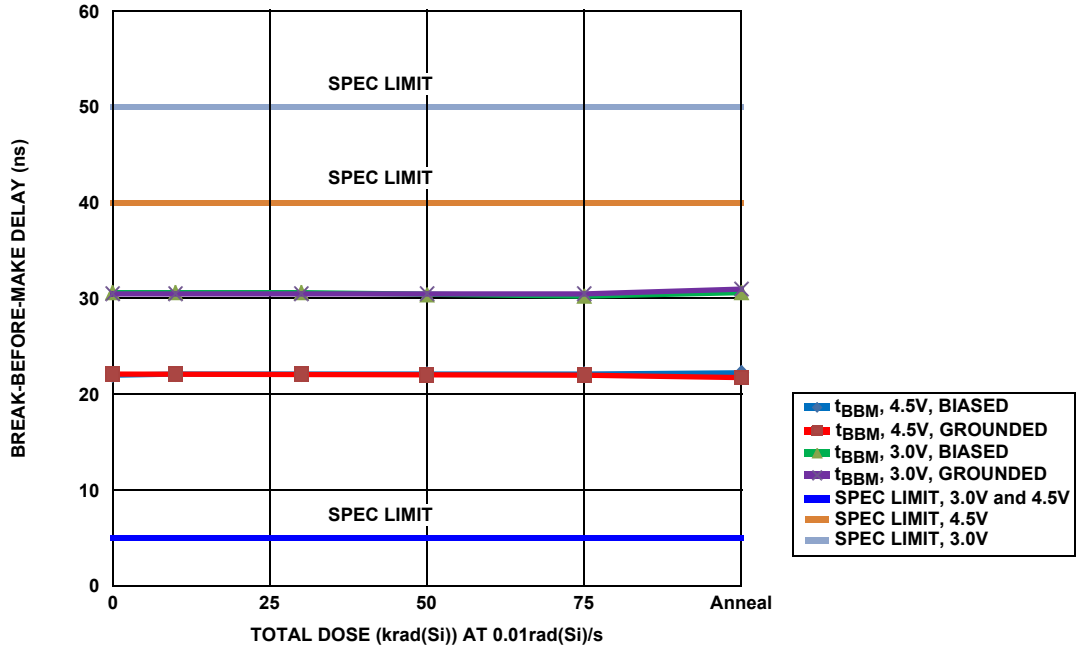


FIGURE 20. ISL71830SEH Break-Before-Make (BBM) delay as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 5ns minimum and 40ns maximum (4.5V) and 5ns minimum and 50.0ns maximum (3.0V).

Variables Data Plots (Continued)

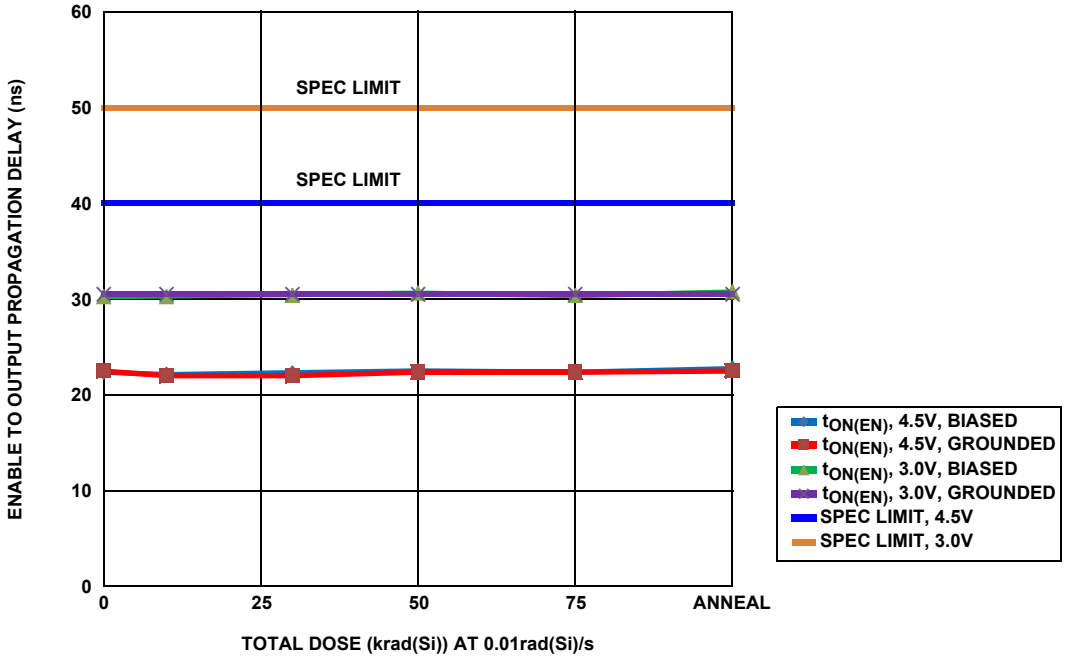


FIGURE 21. ISL71830SEH enable ON to multiplexer output propagation delay as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 40ns maximum (4.5V) and 50ns maximum (3.0V).

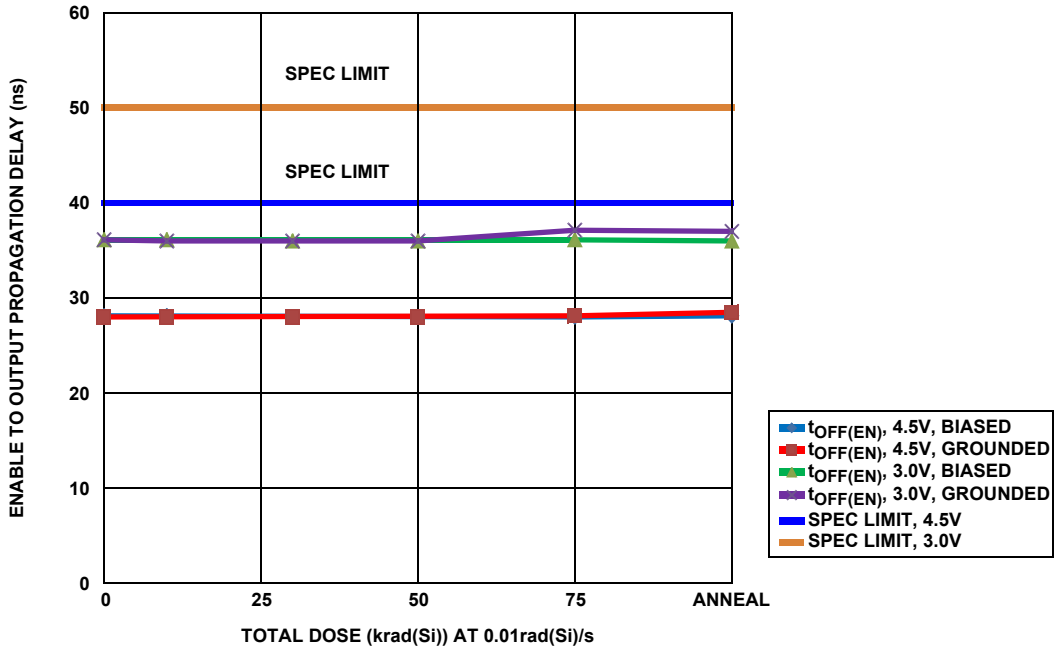


FIGURE 22. IISL71830SEH enable OFF to multiplexer output propagation delay as a function of low dose rate total dose irradiation for the unbiased (all pins grounded) and the biased (per Figure 1) cases. The dose rate was 8.554mrad(Si)/s to 9.322mrad(Si)/s. Sample size for each of the two cells was 16. The post-irradiation SMD limits are 40ns maximum (4.5V) and 50ns maximum (3.0V).

Conclusion

This document reports results of a low dose rate total dose test of the ISL71830SEH 16-channel analog multiplexer. Parts were tested at low dose rate underbiased and unbiased conditions as outlined in MIL-STD-883 Test Method 1019.7. The samples were also taken through a high temperature biased anneal at +100°C for 168 hours.

ATE characterization testing at downpoints showed no rejects to the SMD Group A limits after biased and grounded irradiation at low dose rate or after the high temperature anneal. Attributes data is presented in Table 1, while variables data for selected parameters is presented in Figure 2 through 22. All parameters showed excellent stability.

TABLE 2. REPORTED PARAMETER

FIGURE	PARAMETER	LIMIT LOW	LIMIT HIGH	UNIT	NOTES
2	Switch ON-resistance	-	120	Ω	
3	Switch ON-resistance match	-	5	Ω	
4	Switch ON-resistance flatness	-	40	Ω	
5	Switch input OFF leakage	-30	30	nA	
6	Switch input OFF leakage	-30	30	nA	Overvoltage
7	Switch input OFF leakage	-20	20	nA	Supplies grounded
8	Switch input OFF leakage	-20	20	nA	Supplies open
9	Switch input ON leakage	2.75	5.5	µA	
10	Switch output OFF leakage	-30	30	nA	
11	Switch output ON leakage	-30	30	nA	
12	Logic input LOW voltage	1.3	1.6	V	
13	Logic input HIGH voltage	1.3	1.6	V	
14	Logic input LOW current	-0.1	0.1	µA	
15	Logic input HIGH current	-0.1	0.1	µA	
16	Quiescent supply current	-	0.3	µA	
17	VREF supply current	-	0.2	µA	
18	Address input to output delay	-	70/100	ns	LOW to HIGH, 4.5V/3.0V
19	Address input to output delay	-	70/100	ns	HIGH to LOW, 4.5V/3.0V
20	Break before make delay	5	40/50	ns	4.5V/3.0V
21	Enable ON to output delay	-	40/50	ns	4.5V/3.0V
22	Enable OFF to output delay	-	40/50	ns	4.5V/3.0V

NOTE:

3. Limits are taken from Standard Microcircuit Drawing (SMD) 5962-15247.

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