Total dose testing of the IS-1825ASRH Dual Output PWM

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1. Introduction

This report documents the results of a low and high dose rate total dose test of the IS1825ASRH dual output pulse width modulator (PWM). The test was conducted in order to determine the sensitivity of the part to the total dose environment and to determine if dose rate and bias sensitivity exist. The radiation testing results for the IS-1825ASRH are considered to apply to the IS-1825BSRH, IS-1825BSEH, ISL71823ASRH, and ISL71823BSRH as well, as these parts differ only in their electrical testing, total dose lot acceptance testing, and output operation (1825 is dual alternating and 1823 is in-phase).

2. Reference Documents

MIL-STD-883G test method 1019.7
IS-1825ASRH data sheet
DLA Standard Microcircuit Drawing (SMD) 5962-02511

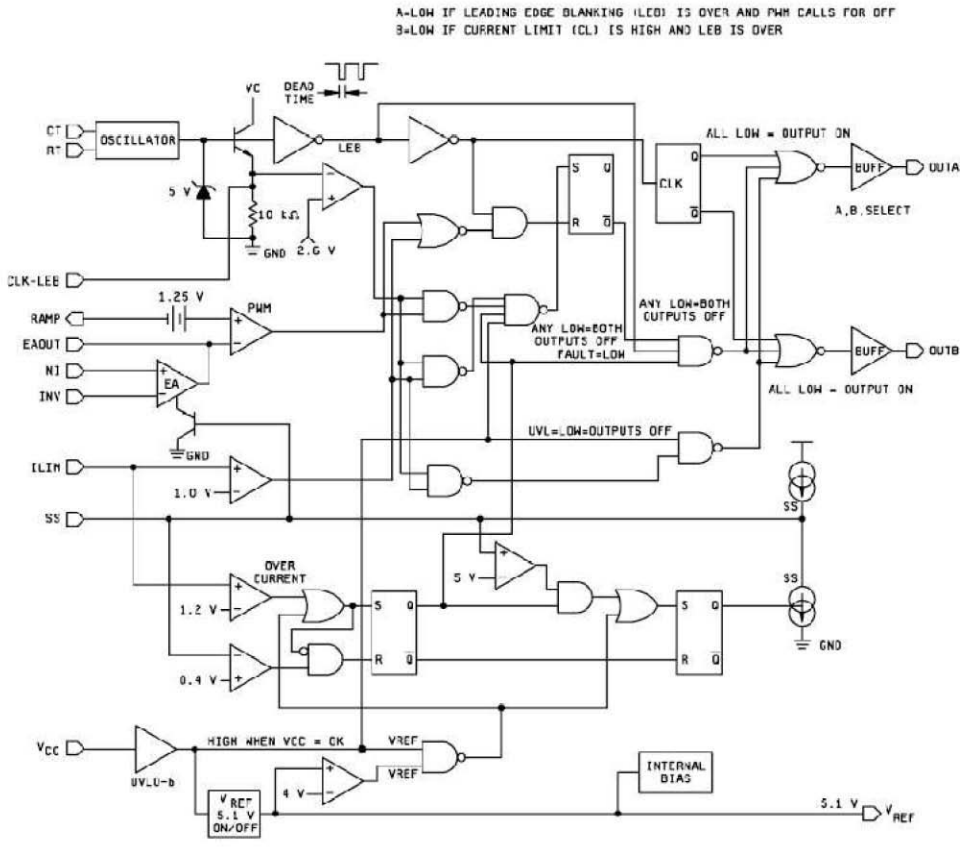
3: Part Description

The radiation hardened IS-1825ASRH pulse width modulator is designed to be used in high frequency switched-mode power supplies and can be used in either current-mode or voltage-mode. It is well suited for single-ended boost converter applications.

Device features include a precision voltage reference, low power start-up circuit, high frequency oscillator, wide-band error amplifier, and fast current-limit comparator. The use of proprietary process capabilities and unique design techniques results in fast propagation delay times and high output current over a wide range of output voltages. Constructed using the Intersil Rad Hard Silicon Gate (RSG) Dielectric Isolation BiCMOS process, the IS-1825ASRH has been specifically designed to provide highly reliable performance when exposed to harsh radiation environments.

The IS-1825ASRH is available in five versions that differ in their electrical testing, total dose lot acceptance testing, and output operation (1825 is dual alternating and 1823 is in-phase). The IS-1825BSEH is acceptance tested on a wafer by wafer basis to 300 krad(Si) at high dose rate (50 – 300 rad(Si)/s) and to 50 krad(Si) at low dose rate (0.01 rad(Si)/s). The IS-1825ASRH and IS-1825BSRH are acceptance tested on a wafer by wafer basis to 300 krad(Si) at high dose rate (50 – 300 rad(Si)/s) only. The ISL71823ASRH and IS71823BSRH are acceptance tested on a wafer by wafer basis to 300 krad(Si) at high dose rate (50 – 300 rad(Si)/s) only. -EH versions of the ISL71823ASRH and IS71823BSRH are not planned at this time.

Specifications for radiation hardened QML devices are controlled by the Defense Logistics Agency - Land & Maritime (DLA). Detailed electrical specifications for the IS-1825ASRH are contained in SMD 5962-02511. The document may be downloaded from the Intersil website at www.intersil.com/space or from the DLA site. The SMD numbers must be used when ordering.



NOTE: For device type 02 only, toggles Q and $\overline{Q}$ are always low.

Figure 1: IS-1825ASRH block diagram.

4: Test Description

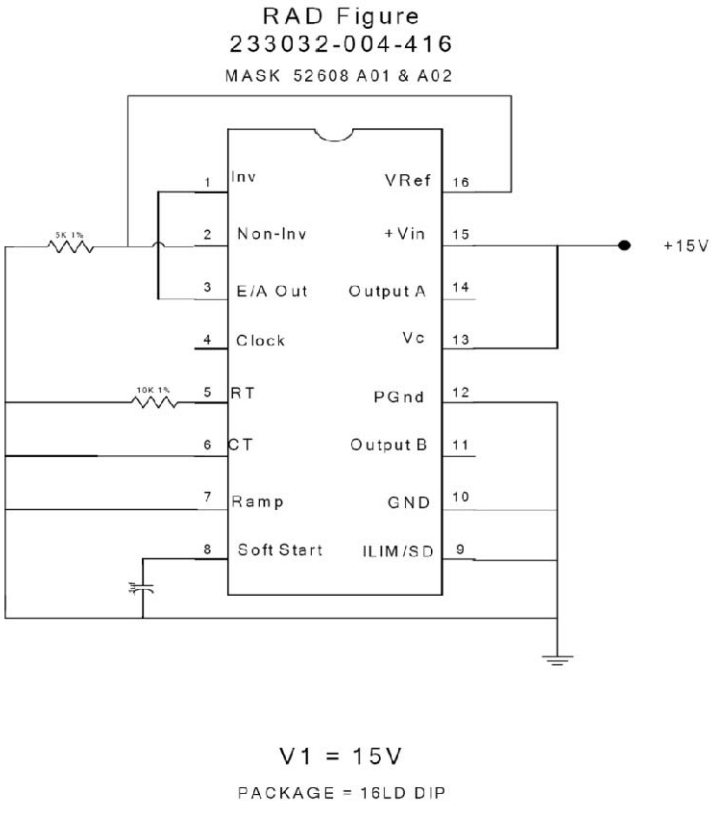
4.1 Irradiation Facilities

High dose rate testing was performed using a Gammacell 220^{60}Co irradiator located in the Palm Bay, Florida Intersil facility. Low dose rate testing was performed on a subcontract basis at White Sands Missile Range (WSMR) Survivability, Vulnerability and Assessment Directorate (SVAD), White Sands, NM, using a vault-type ^{60}Co irradiator. The high dose rate irradiations were done at 55rad(Si)/s and the low dose rate work was performed at 0.010rad(Si)/s, both per MIL-STD883 Method 1019.7. Dosimetry for the low dose rate test was performed using Far West Technology radiochromic dosimeters and readout equipment.

4.2 Test Fixturing

Fig. 2 shows the configuration used for biased irradiation at both high and low dose rate. This bias configuration differed in detail from the SMD 5962-02511 configuration in the method used for disabling the on-chip oscillator. This change was made due to concerns about disabling the oscillator through tying the RT terminal to 15V. As both configurations are static and are used to apply a DC electric field across MOOSFET device gate oxide, total dose tests for b both configurations are expected to correlate well.

Figure 2: Irradiation bias configuration for the IS-1825ASRH per Standard Microcircuit Drawing (SMD) 5962-02511.



4.3 Characterization equipment and procedures

All electrical testing was performed outside the irradiator using the production automated test equipment (ATE) with datalogging at each downpoint. Downpoint electrical testing was performed at room temperature. Performing low dose rate testing at a remote site introduces some challenges, and shipping was performed using g a foam container with a frozen Gelpack™ along with a strip chart temperature recorder in order to remain well within the temperature limits imposed by MIL-STD-883 Test Method 1019.7. Close coordination between the two organizations is required, and support by WSMR is gratefully acknowledged.

4.4 Experimental matrix

The experimental matrix consisted of five samples irradiated at high dose e rate with all pins grounded, five samples irradiated at high dose rate under bias, five samples irradiated at low dose rate with all pins grounded and five e samples irradiated at low dose rate under bias. One control unit was used.

Samples of the IS-1825ASRH die were drawn from production lot EOT2EA and were packaged in the standard hermetic 16-pin solder-sealed flatpack (CDFP4-F16) production package. Samples were processed through the standard burnin cycle before irradiation, as required by MILSTD-883, and were screened to the SMD 5962-02511 limits at room, low and high temperatures prior to the test.

4.5 Downpoints

Downpoints for the tests were 0, 10, 15, 20 and 25krad(Si) for the high dose rate test and 0, 10, 14, 20, 25, 35, 50, 75, 100, 125 and 150krad(Si) for the low dose rate test.

5: Results

5.1 Test results

Testing at both dose rates of the IS-1825ASRH is complete through all down points. In earlier work, the IS-1825ASRH was tested in 2003 using an early accelerated low dose test protocol, consisting of irradiation at 10rad(Si)/s at an ambient temperature of 100°C. This work was performed in collaboration with Harris Corporation using a modified Gammacell 220. The modifications included extra field flattener shields and a high temperature fixture and closed-loop control system. Using this approach, the IS-1825ASRH was tested to 25krad(Si). Samples showed significant parametric degradation.

The current test was undertaken to determine the response of current production parts to true low dose rate irradiation. A high dose rate test was run up to 25krad(Si) as a baseline. For the current test, the great majority of parameters were very stable over low and high dose rate irradiation. The median error amplifier input offset voltage showed a change of 4mV over the 150krad(Si) low dose rate exposure, while the input offset current median showed a 1µA shift. Both parameters were well within the applicable SMD limits, see Figs. 17 and 19. The PWM comparator ramp offset voltage was at the 0.81V limit after 150krad(Si), see Fig. 30. Note the 50krad(Si) median for this parameter was at the 1.5V ATE limit. This data point is considered of doubtful quality and is plotted for information only. Additionally the median current limit threshold and overcurrent threshold were near their respective 0.85V and 1.05V specifications after 150krad(Si) at low dose rate, see Figures 35 and 36.

The high dose rate irradiation to 25krad(Si) produced very little change in any of the monitored parameters.

The part is considered moderately low dose rate sensitive but remains within the SMD post-irradiation limits to a maximum of 100krad(Si) in this environment. We also observed some bias sensitivity in the low dose rate results, with biased irradiation clearly the worst-case condition.

5.2 Variables data

The plots in Figs. 3 through 51 show data at all downpoints. The plots show the median of key parameters as a function of total dose for each of the four irradiation conditions. We chose to plot the median for these parameters due to the relatively small sample sizes.

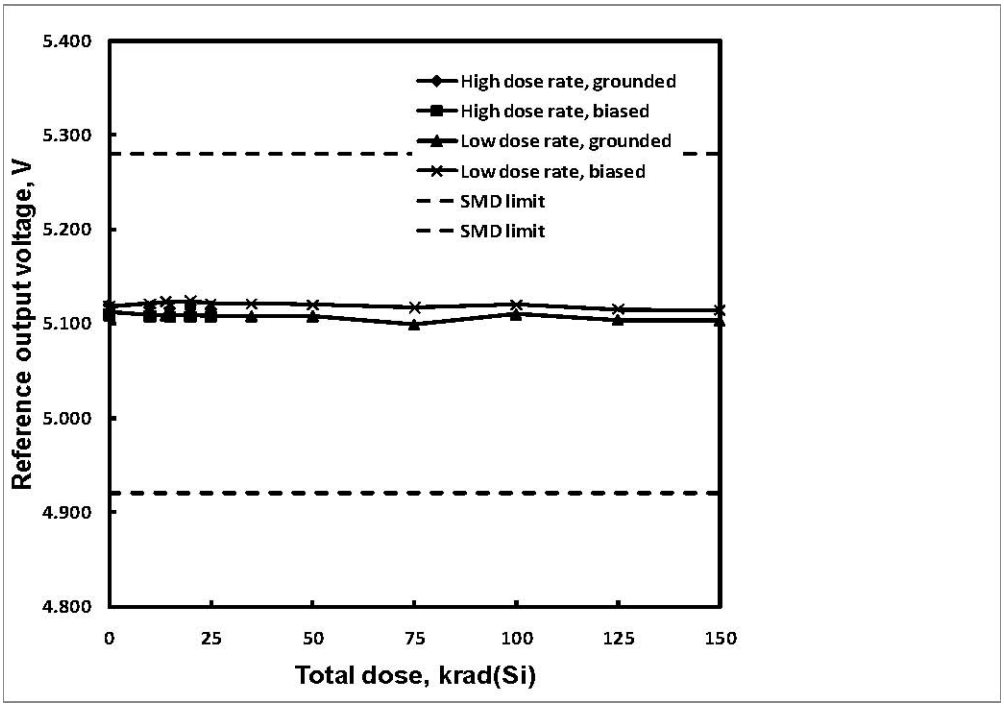


Fig. 3: IS-1825ASRH reference output voltage as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Fig. 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are 4.92V to 5.28V.

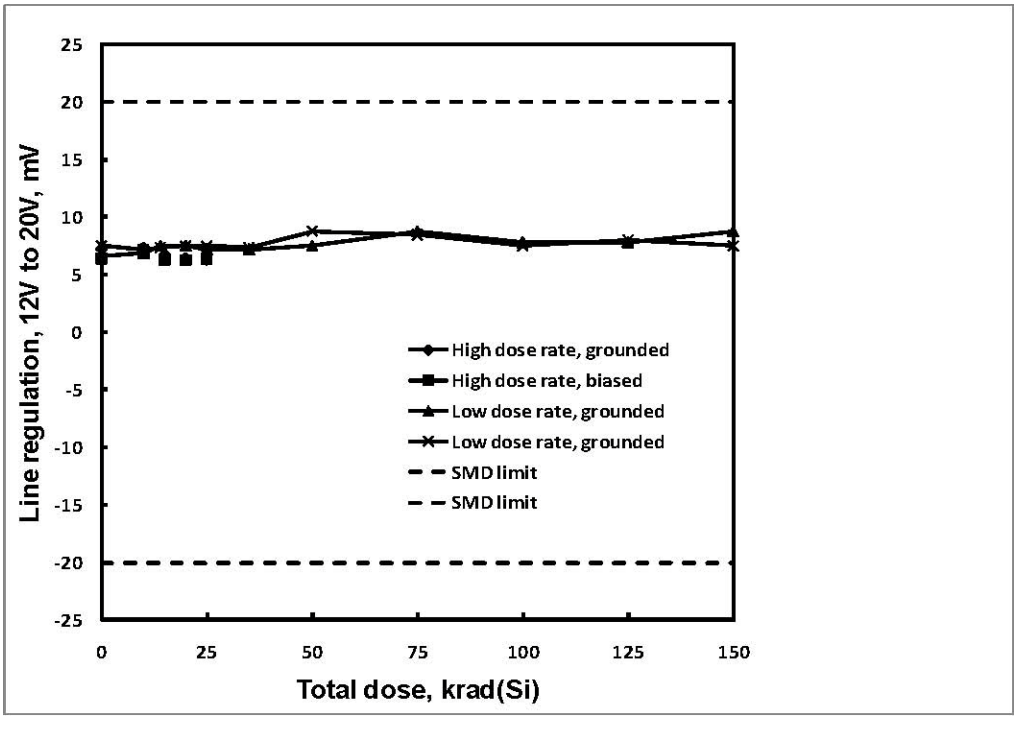


Fig. 4: IS-1825ASRH line regulation as a function of total dose irradiation at low and high dose rate for the unbiased (all pins grounded) and the biased (per Fig. 2) cases. The low dose rate was 0.01rad(Si)/s and the high dose rate 55rad(Si)/s. Sample size for each cell was 5. The post-irradiation SMD limits are -20mV to +20mV.

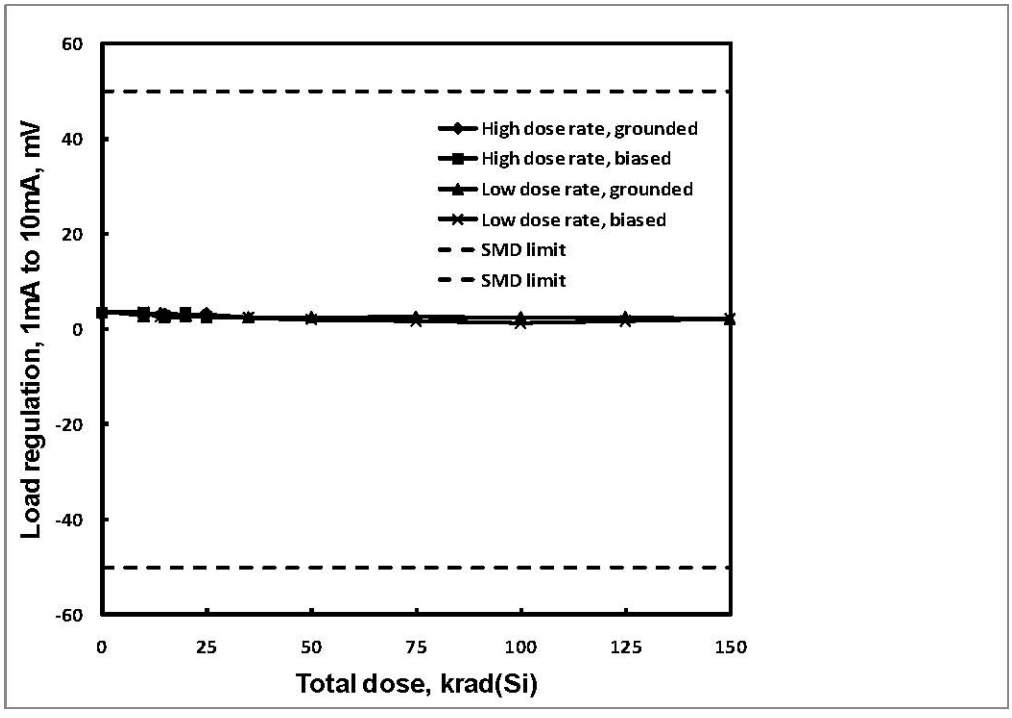


Fig. 5: IS-1825ASRH load regulation, 1mA to 10mA load step, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -50mV to +50mV.

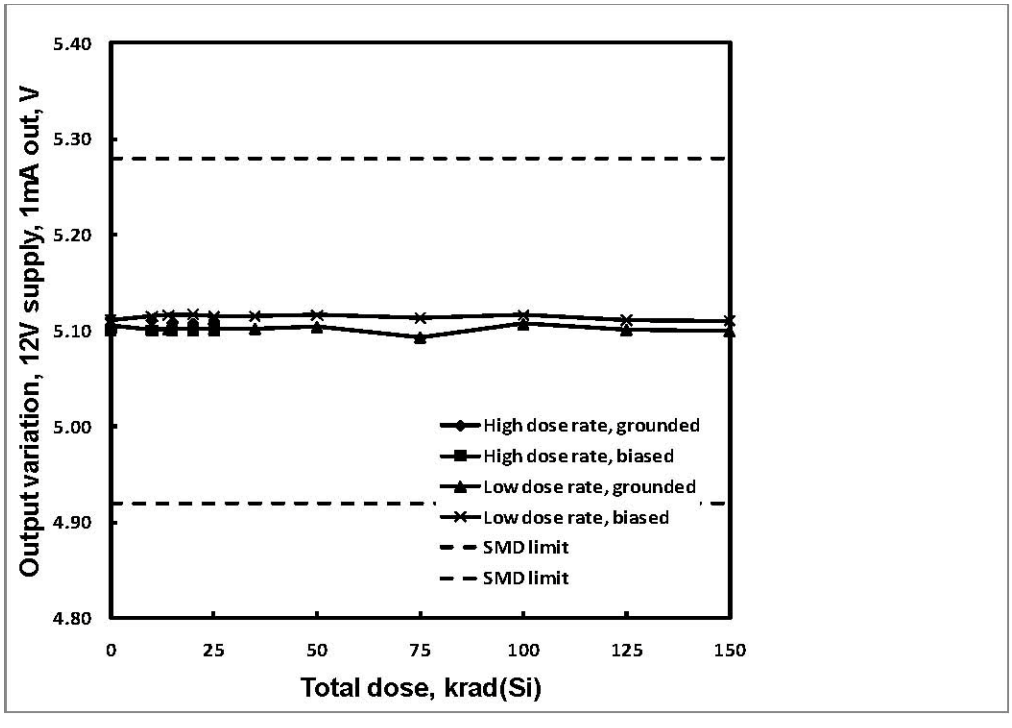


Fig. 6: IS-1825ASRH total reference voltage variation, 12V supply, 1mA output current, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 4.92V to 5.28V.

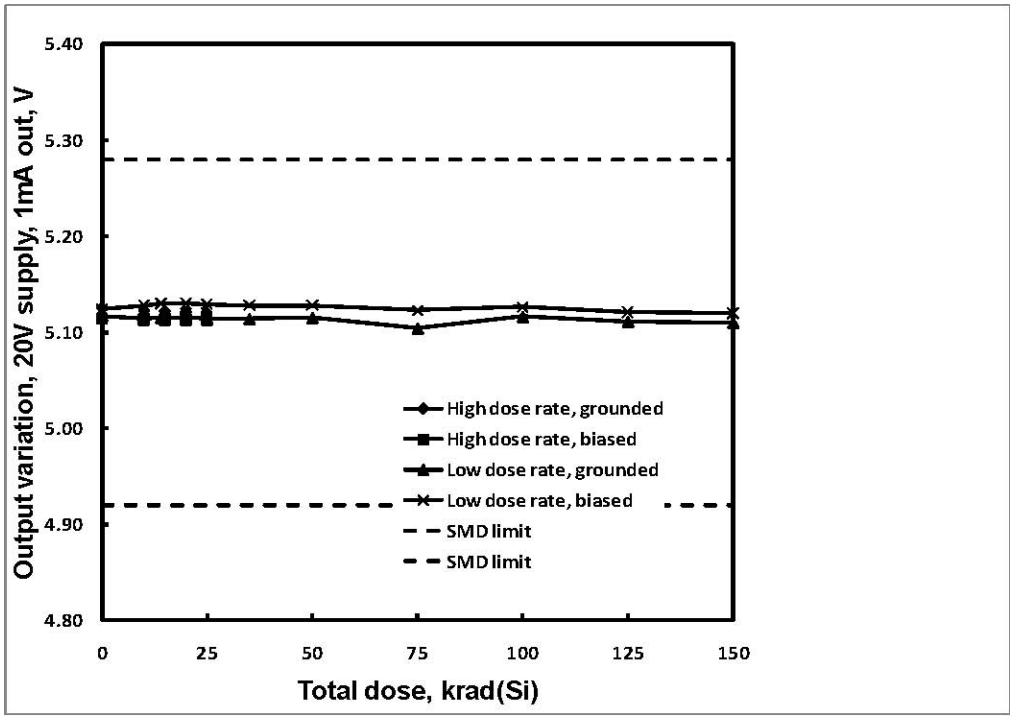


Fig. 7: IS-1825ASRH total reference voltage variation, 20V supply, 1mA output current, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 4.92V to 5.28V.

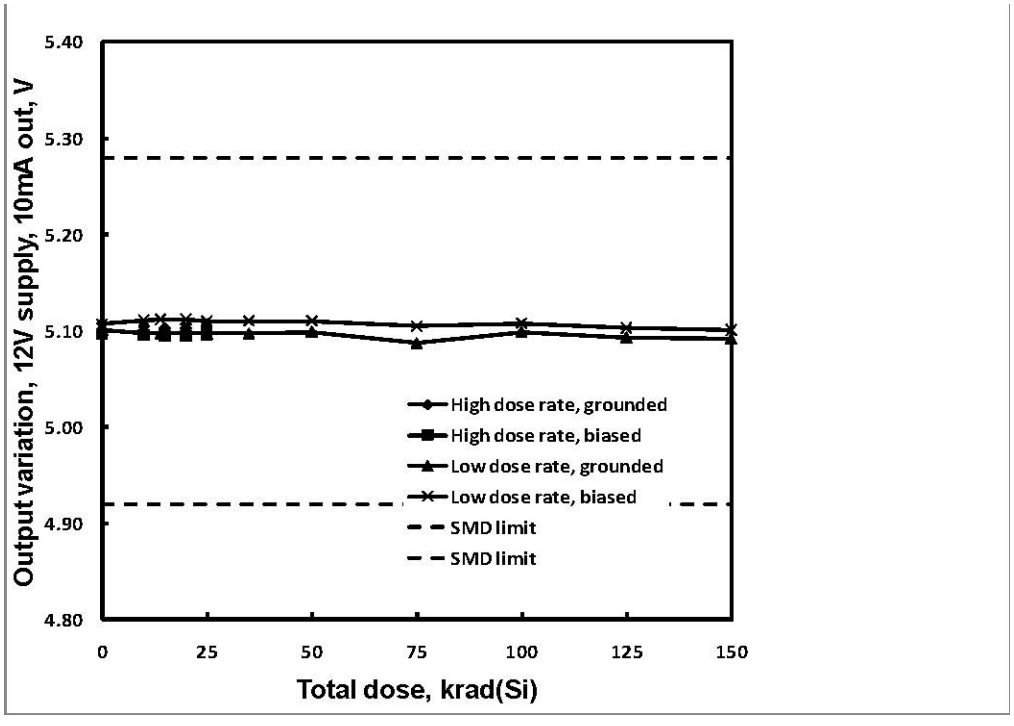


Fig. 8: IS-1825ASRH total reference voltage variation, 12V supply, 10mA output current, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 4.92V to 5.28V.

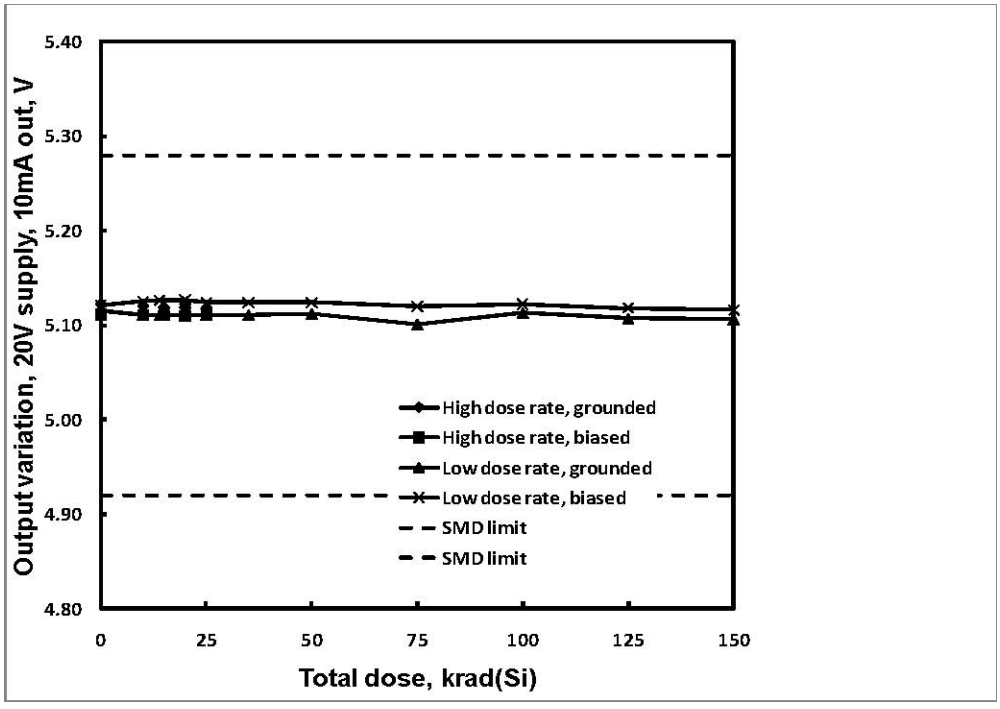


Fig. 9: IS-1825ASRH total reference voltage variation, 20V supply, 10mA output current, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 4.92V to 5.28V.

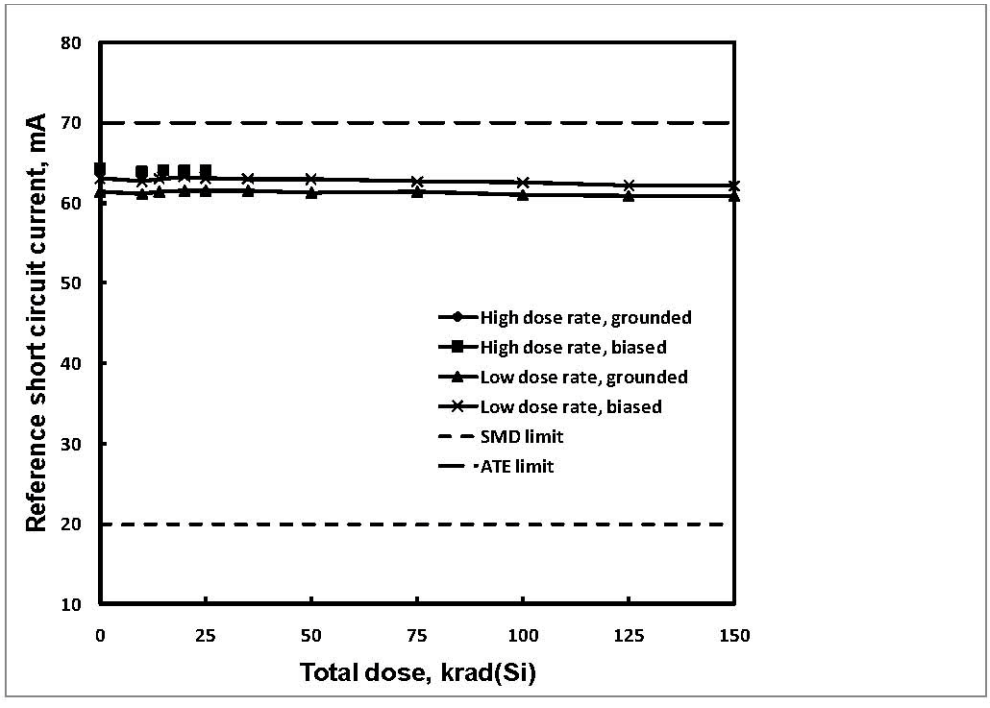


Fig. 10: IS-1825ASRH reference short circuit current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 20mA minimum; the 70mA upper bound is an ATE limit.

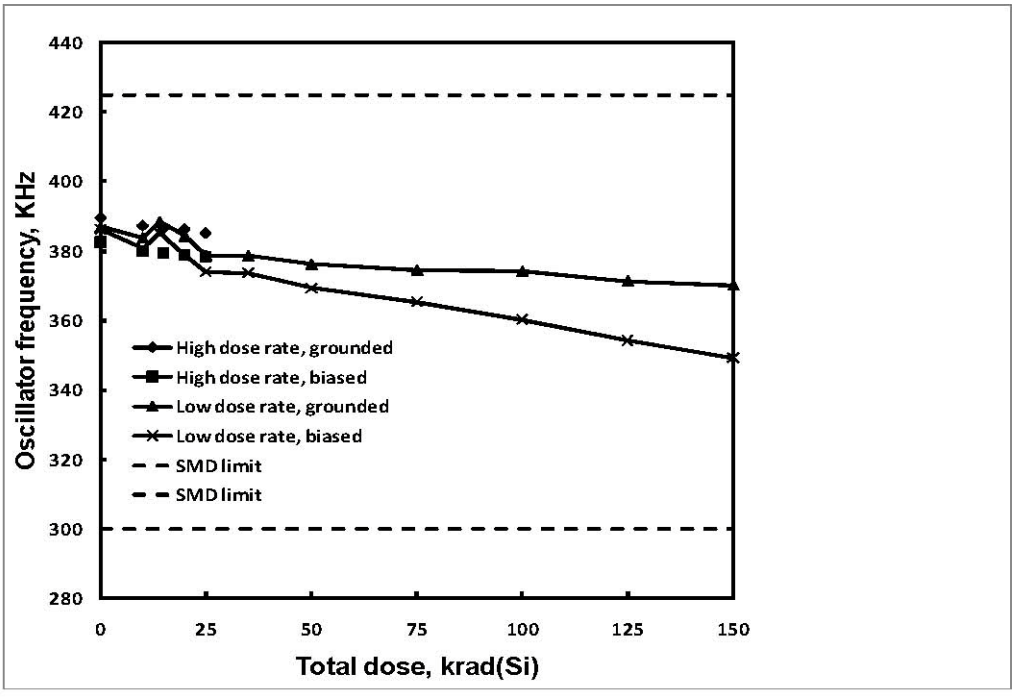


Fig. 11: IS-1825ASRH oscillator frequency as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 300KHz to 425KHz.

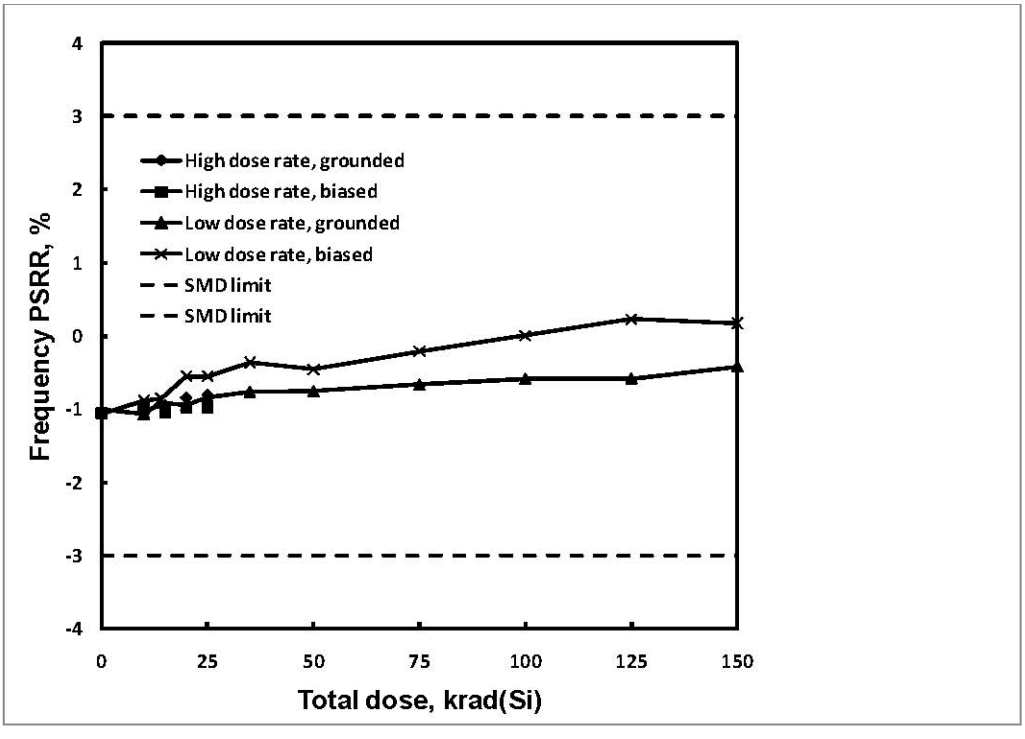


Fig. 12: IS-1825ASRH oscillator frequency power supply rejection ratio (PSRR), 12V to 20V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -3% to +3%.

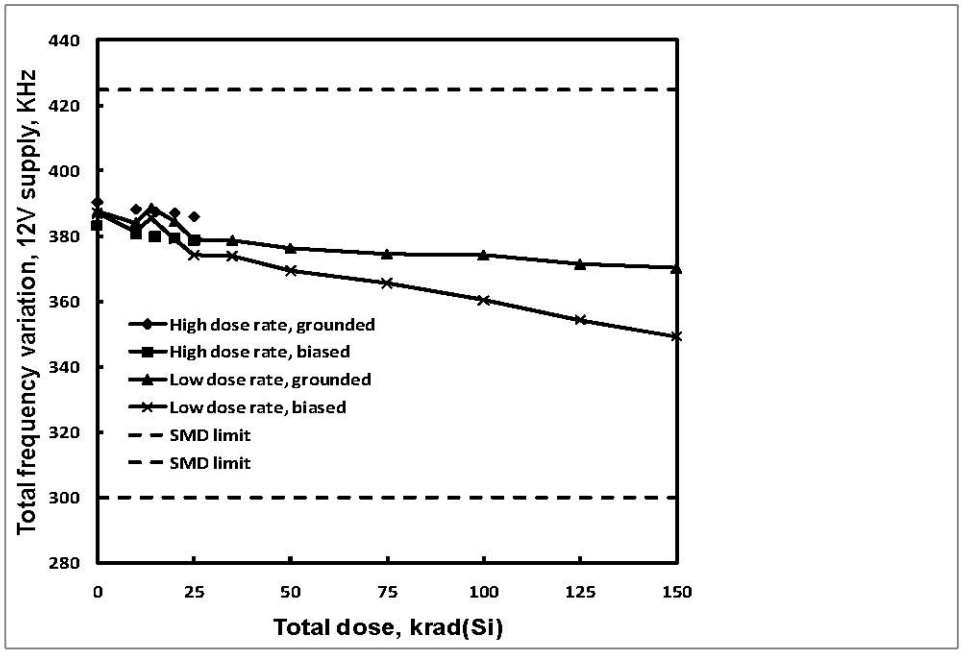


Fig. 13: IS-1825ASRH total frequency variation, 12V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 300KHz to 425KHz.

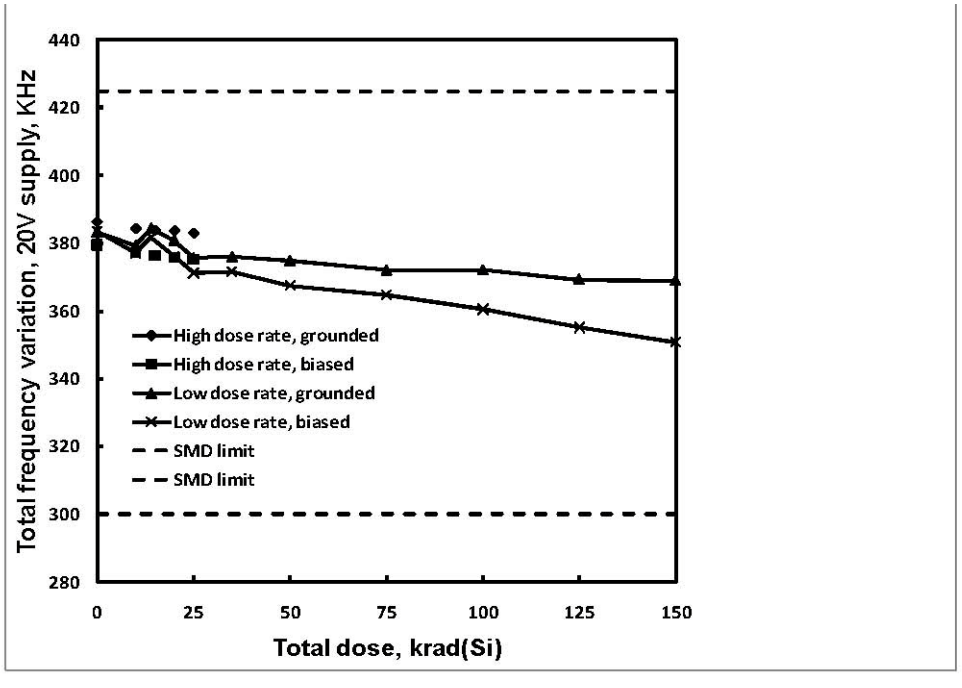


Fig. 14: IS-1825ASRH total frequency variation, 20V supply, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 300KHz to 425KHz.

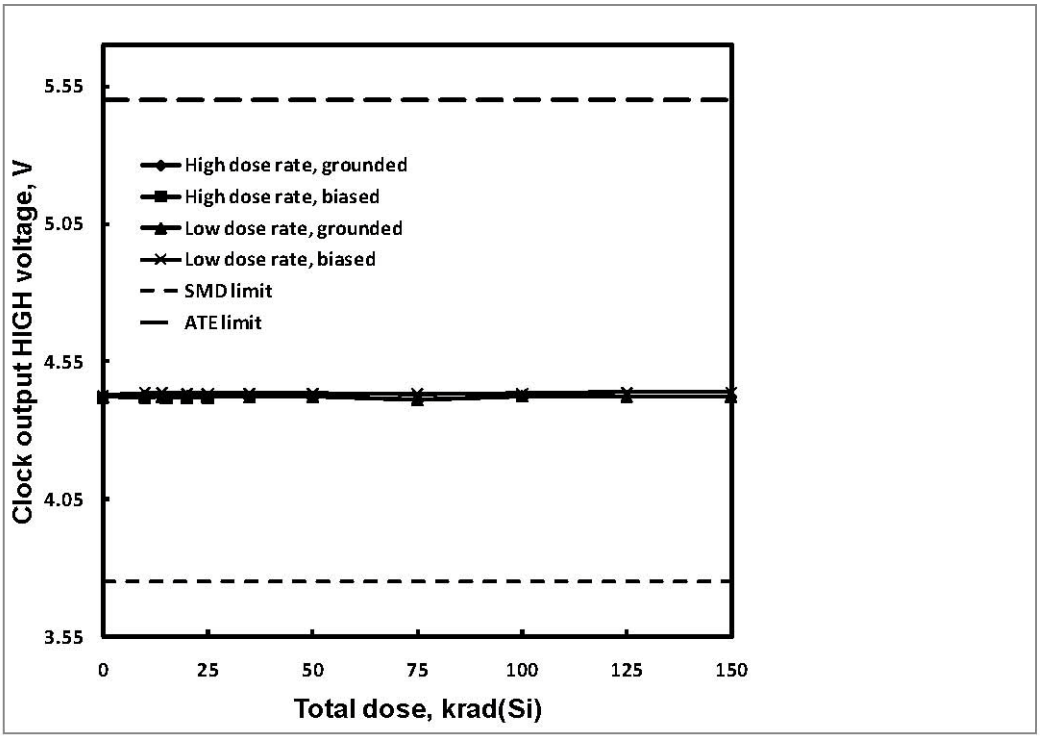


Fig. 15: IS-1825ASRH clock output HIGH voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 3.75V minimum; the 5.5V upper bound is an ATE limit.

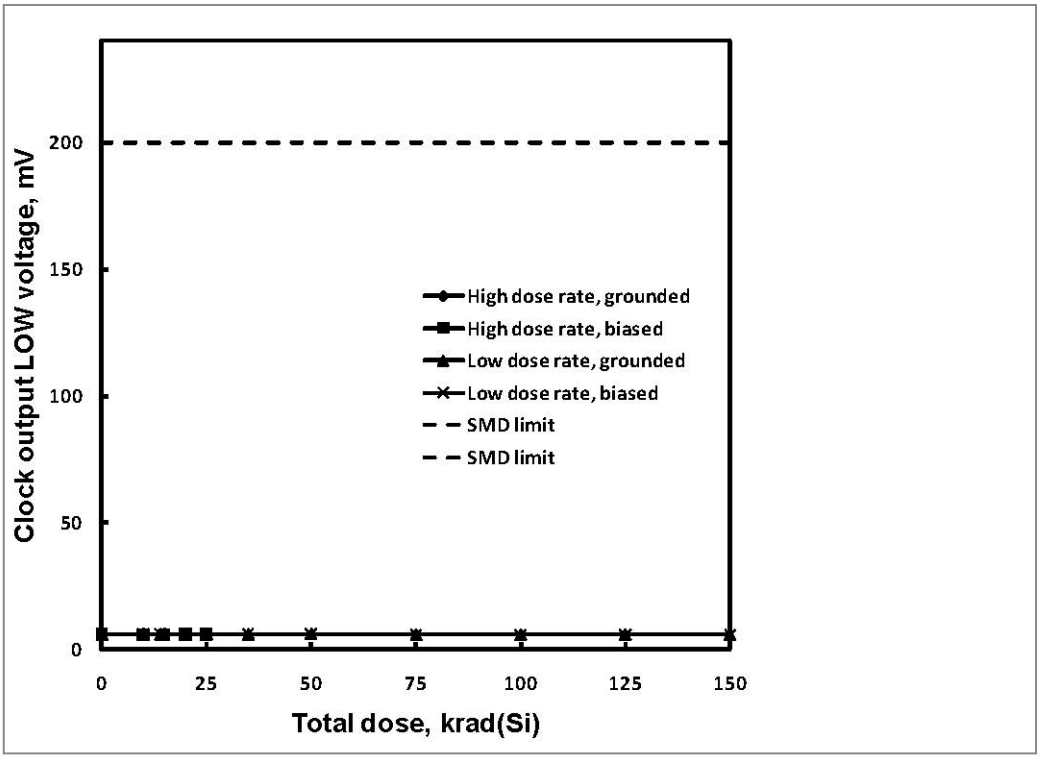


Fig. 16: IS-1825ASRH clock output LOW voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 200mV maximum.

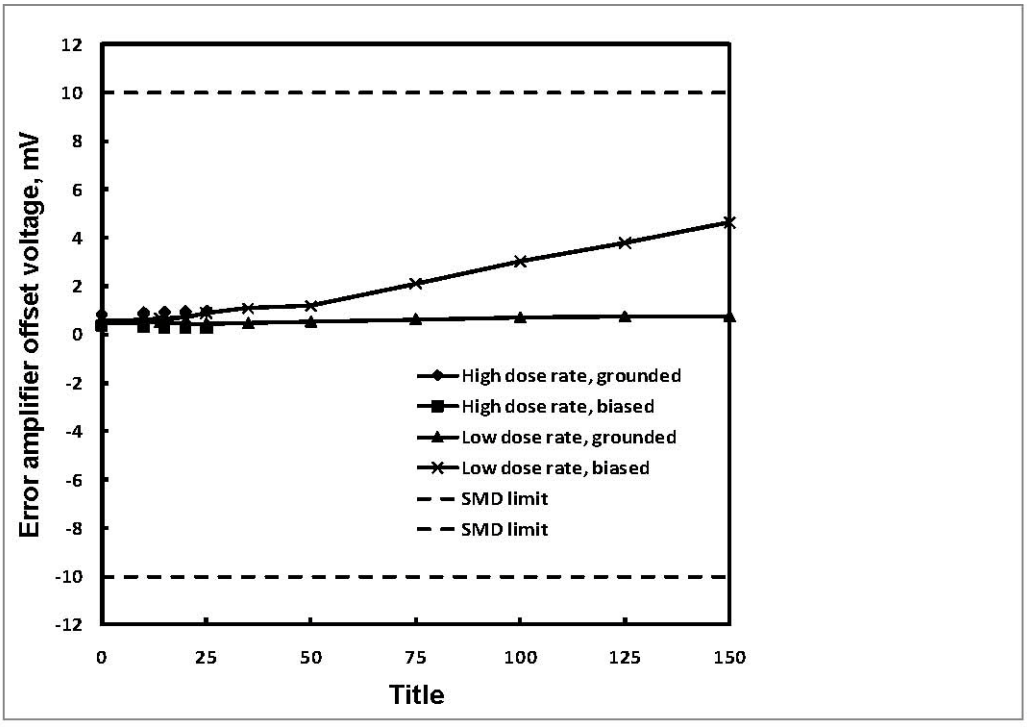


Fig. 17: IS-1825ASRH error amplifier input offset voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -10mV to 10mV.

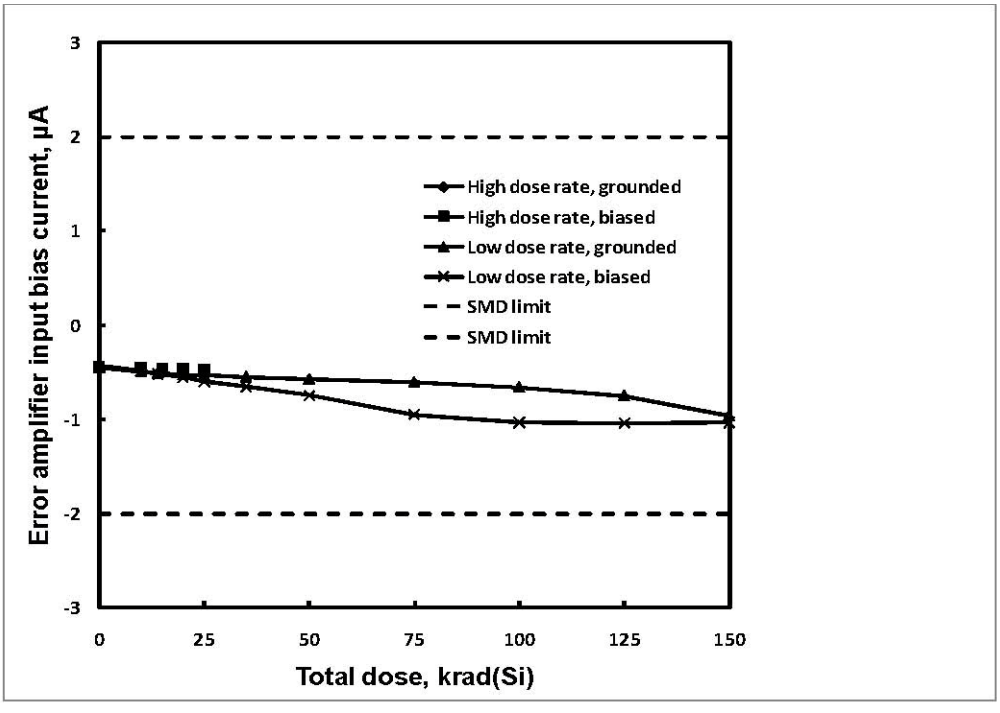


Fig. 18: IS-1825ASRH error amplifier input bias current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -2µA to 2µA.

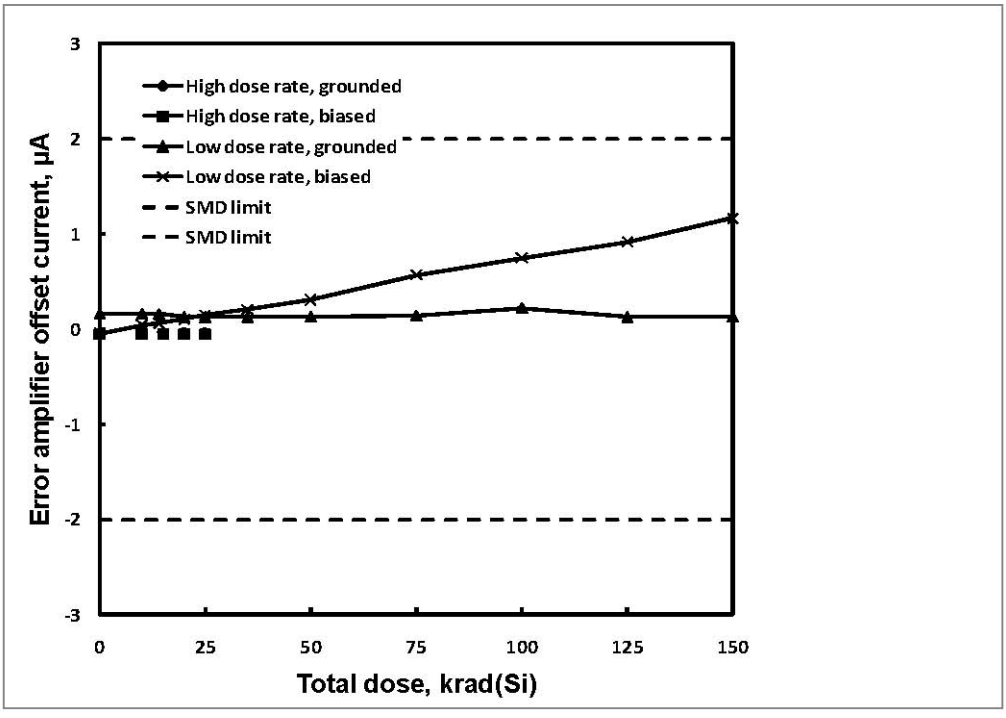


Fig. 19: IS-1825ASRH error amplifier input offset current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are -2µA to 2µA.

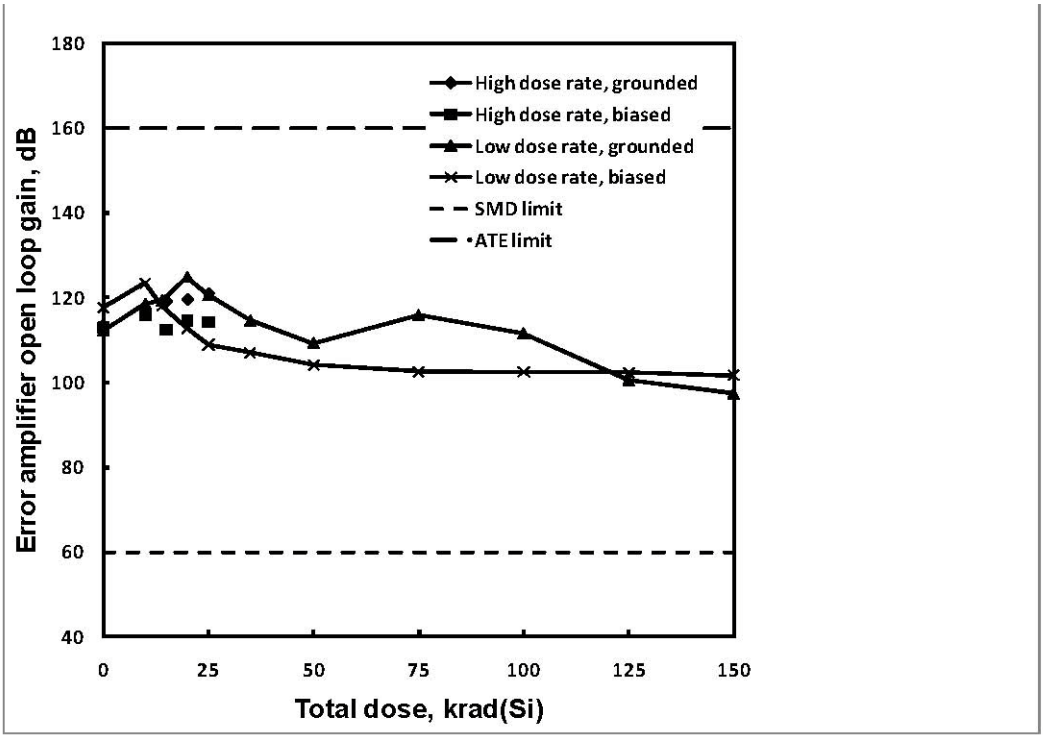


Fig. 20: IS-1825ASRH error amplifier open-loop voltage gain as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 60dB minimum; the 160dB upper bound is an ATE limit.

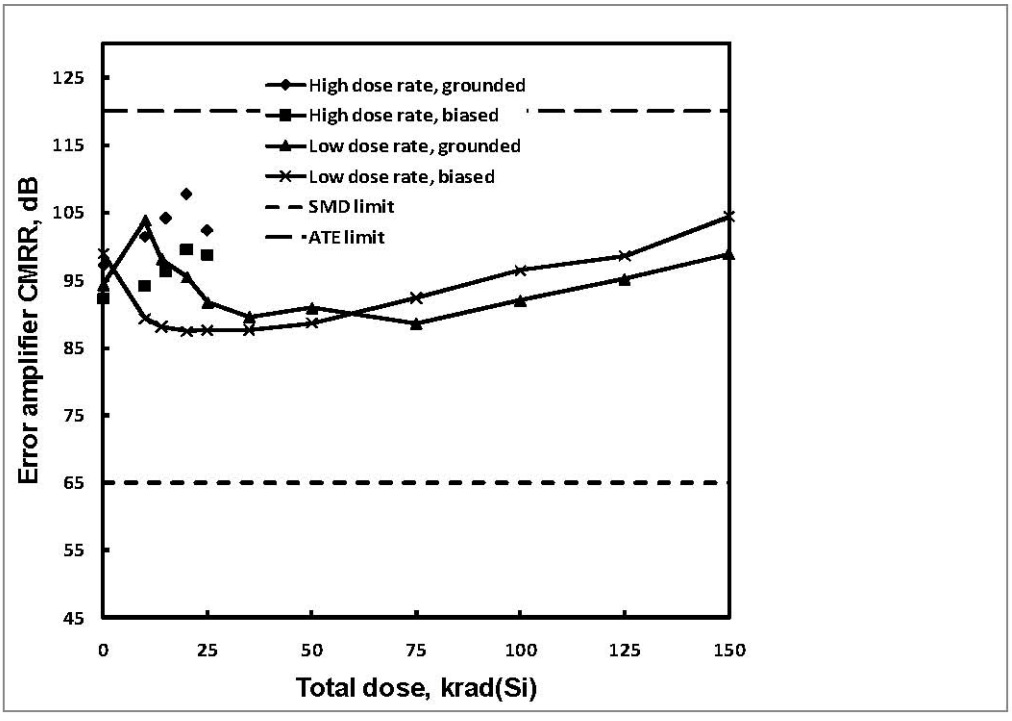


Fig. 21: IS-1825ASRH error amplifier common-mode rejection ratio (CMRR) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 65dB minimum; the 120dB upper bound is an ATE limit.

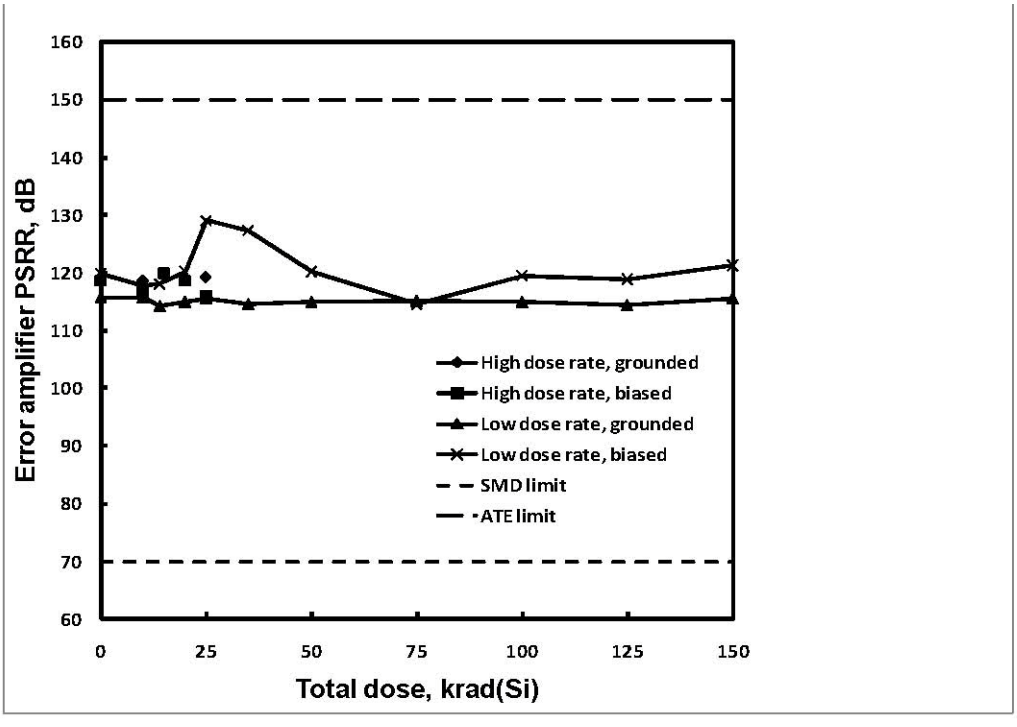


Fig. 22: IS-1825ASRH error amplifier power supply rejection ratio (PSRR) as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 70dB minimum; the 150dB upper bound is an ATE limit.

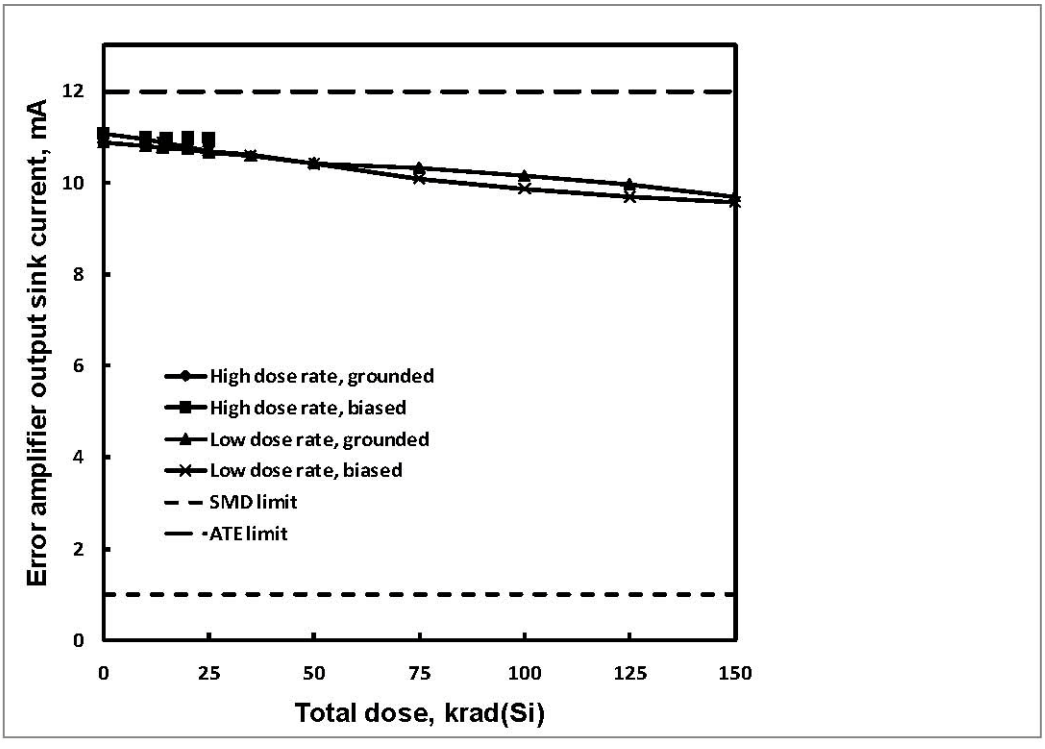


Fig. 23: IS-1825ASRH error amplifier output sink current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 1mA minimum; the 12mA upper bound is an ATE limit.

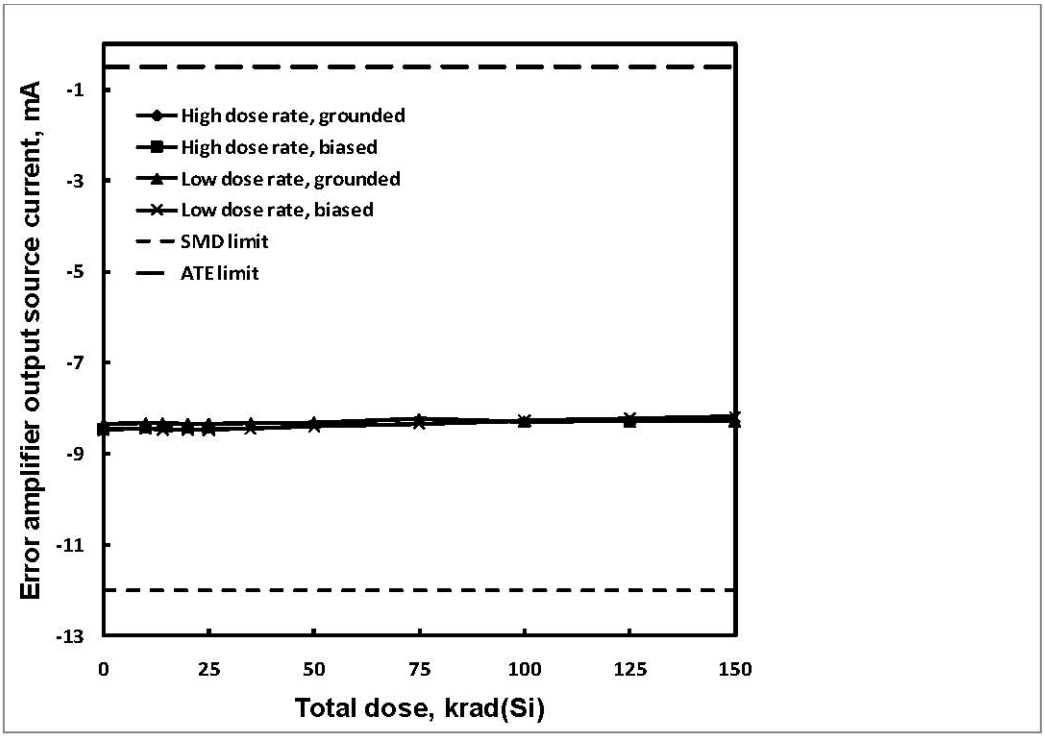


Fig. 24: IS-1825ASRH error amplifier output source current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is -0.5mA minimum; the -12mA lower bound is an ATE limit.

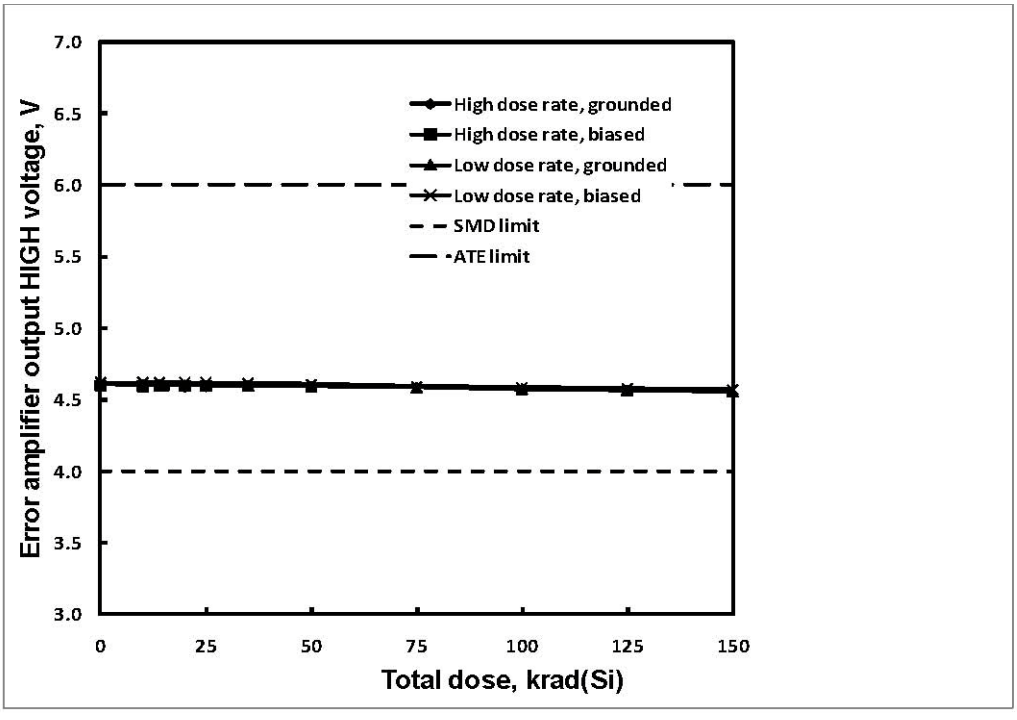


Fig. 25: IS-1825ASRH error amplifier output HIGH voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 4V minimum; the 6V upper bound is an ATE limit.

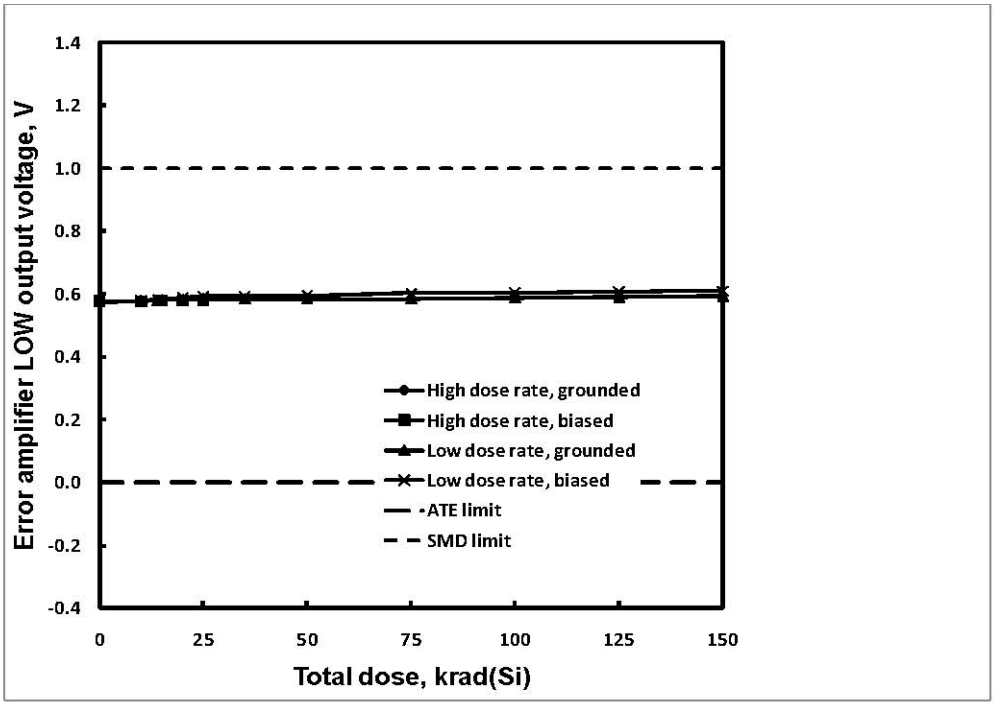


Fig. 26: IS-1825ASRH error amplifier output LOW voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 1V maximum; the 0V lower bound is an ATE limit.

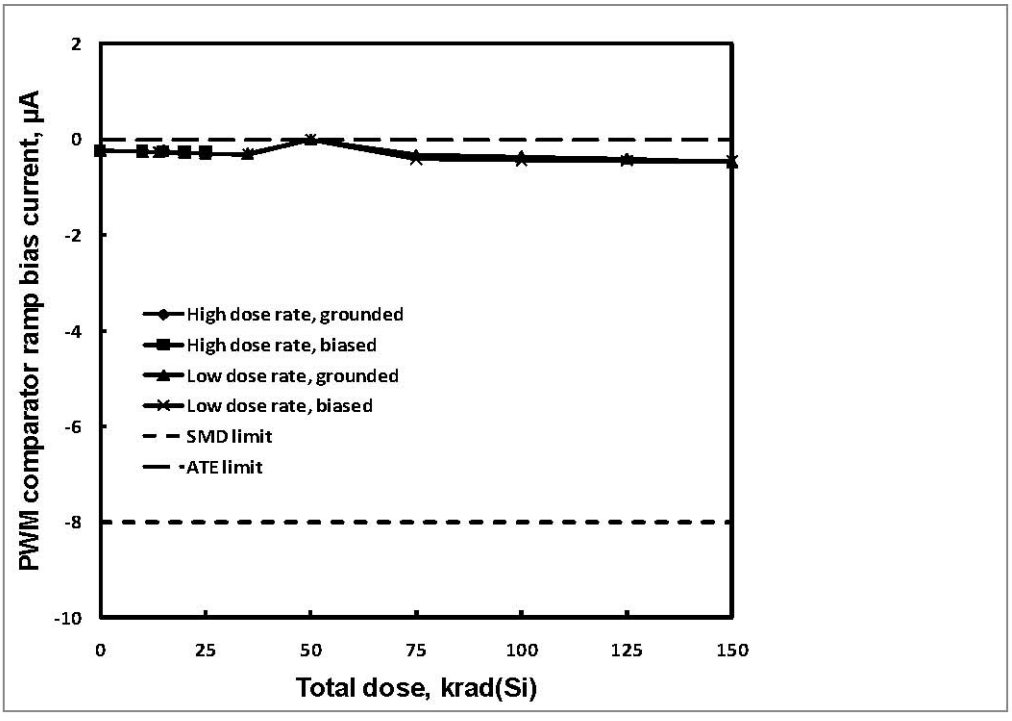


Fig. 27: IS-1825ASRH PWM comparator ramp bias current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is -8µA maximum; the 0µA lower bound is an ATE limit.

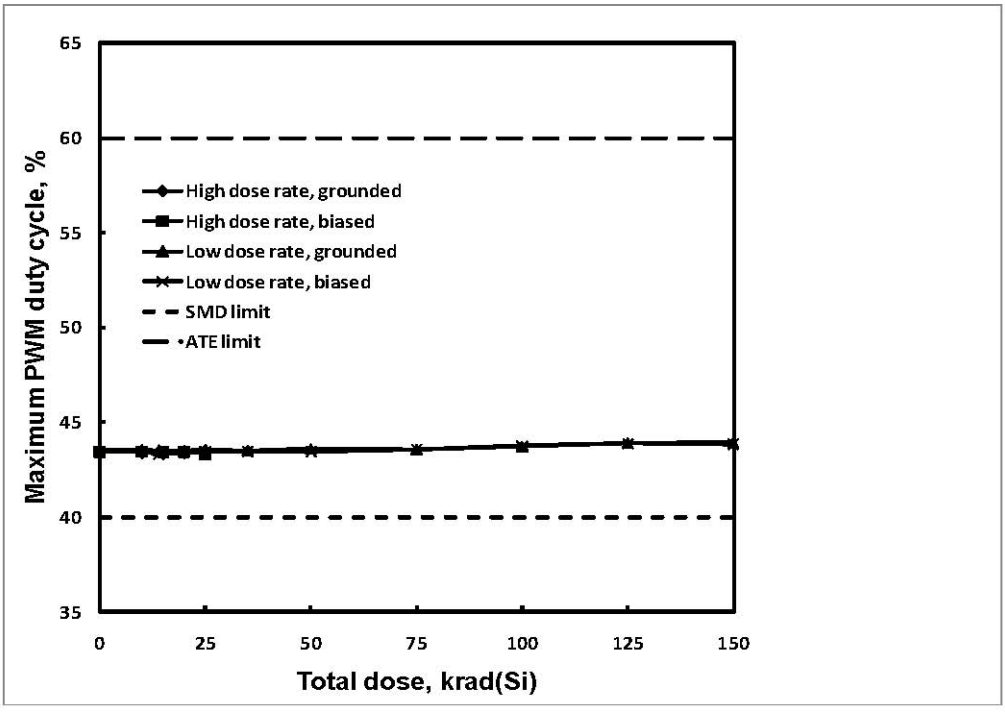


Fig. 28: IS-1825ASRH maximum PWM duty cycle, output A, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 40% minimum; the 60% upper bound is an ATE limit.

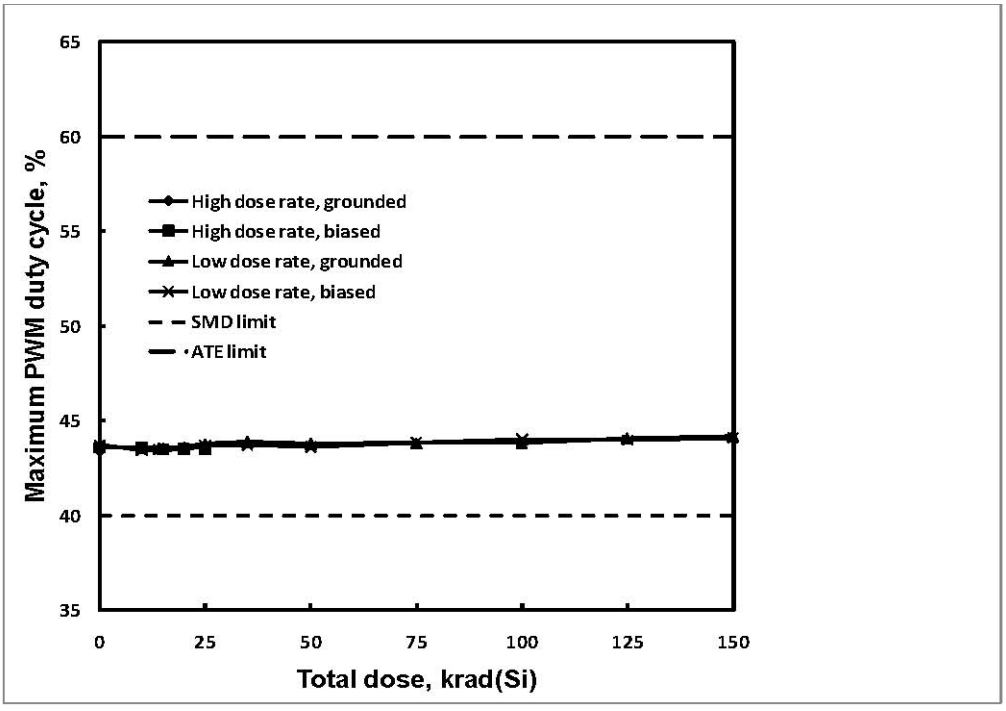


Fig. 29: IS-1825ASRH maximum PWM duty cycle, output B, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 40% minimum; the 60% upper bound is an ATE limit.

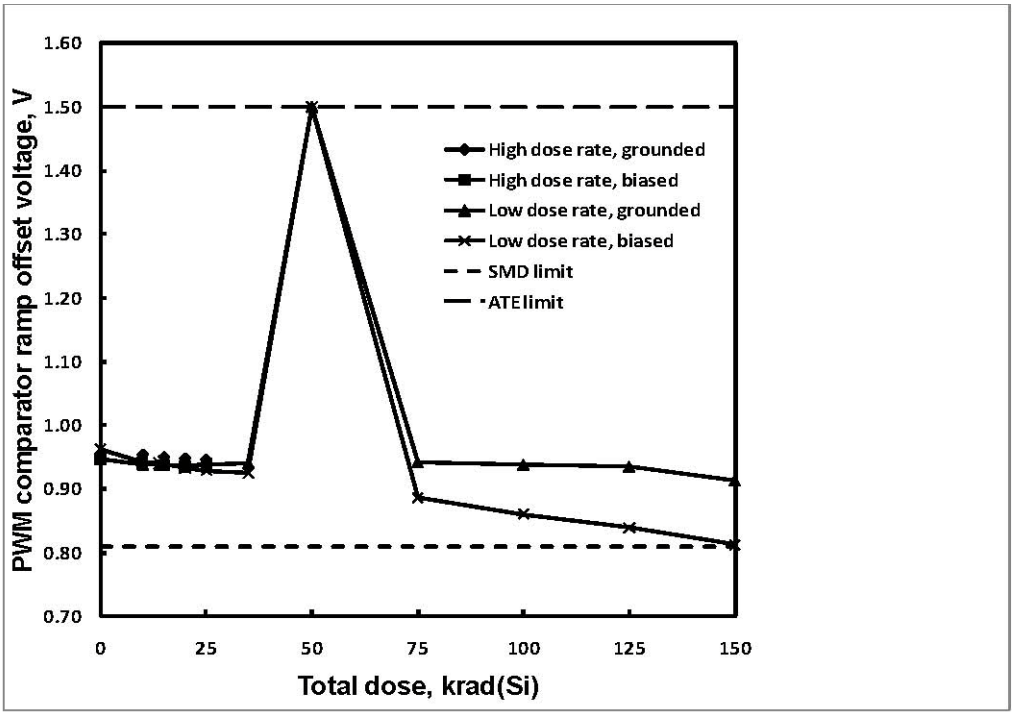


Fig. 30: IS-1825ASRH PWM comparator ramp offset voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 0.81V minimum; the 1.5V upper bound is an ATE limit.

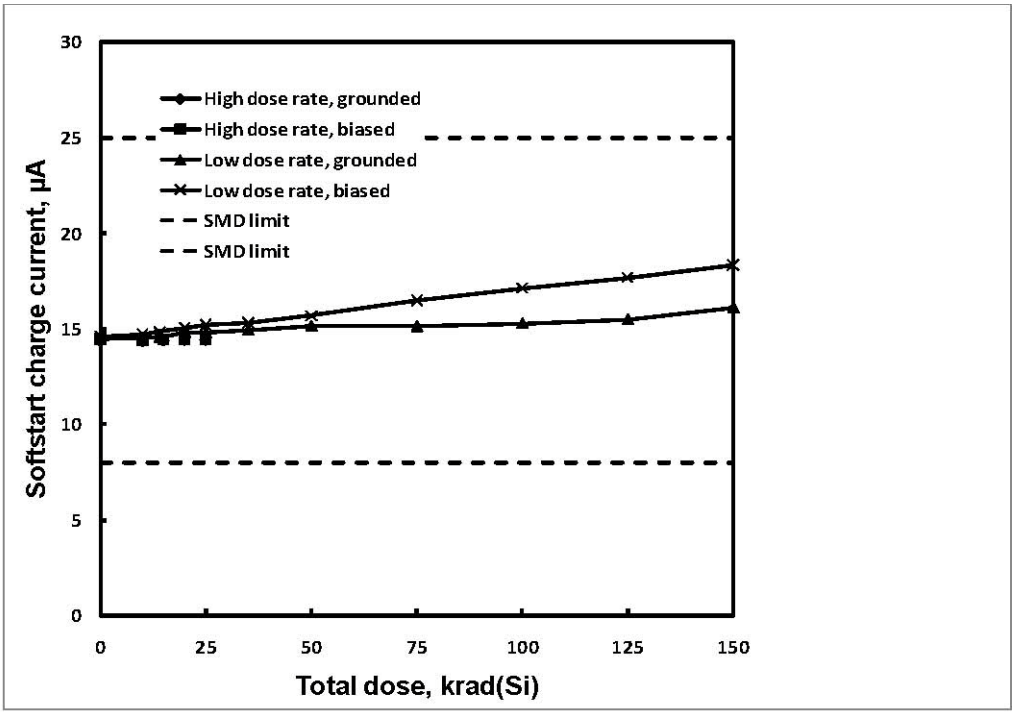


Fig. 31: IS-1825ASRH softstart charge current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 8µA to 25µA.

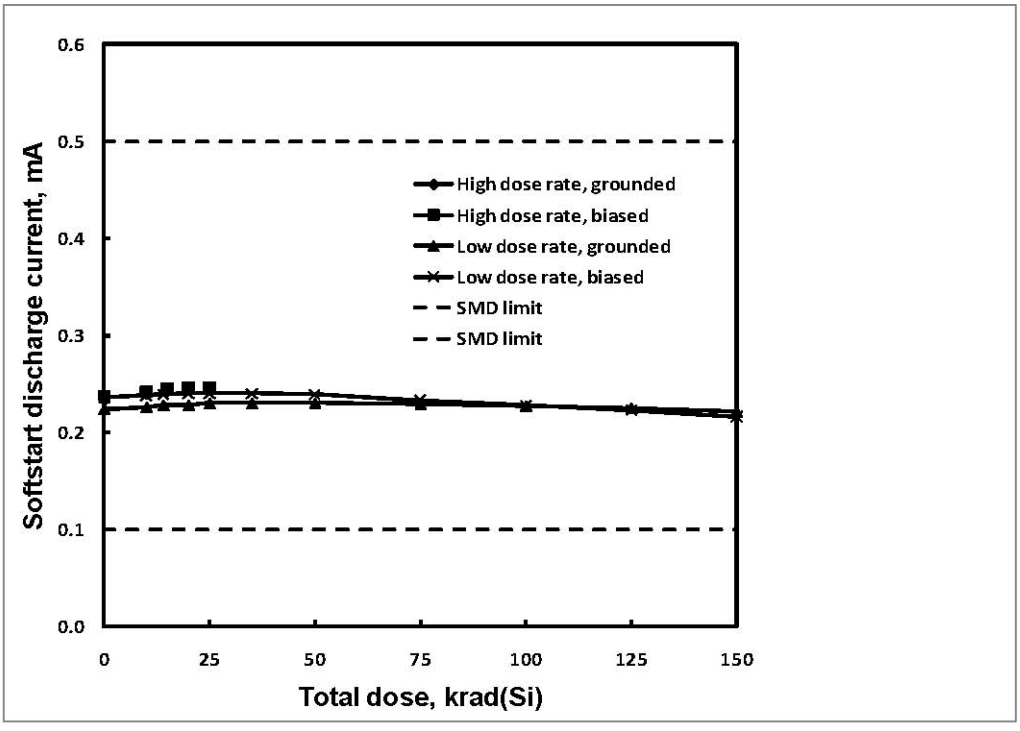


Fig. 32: IS-1825ASRH softstart discharge current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 0.1mA to 0.5mA.

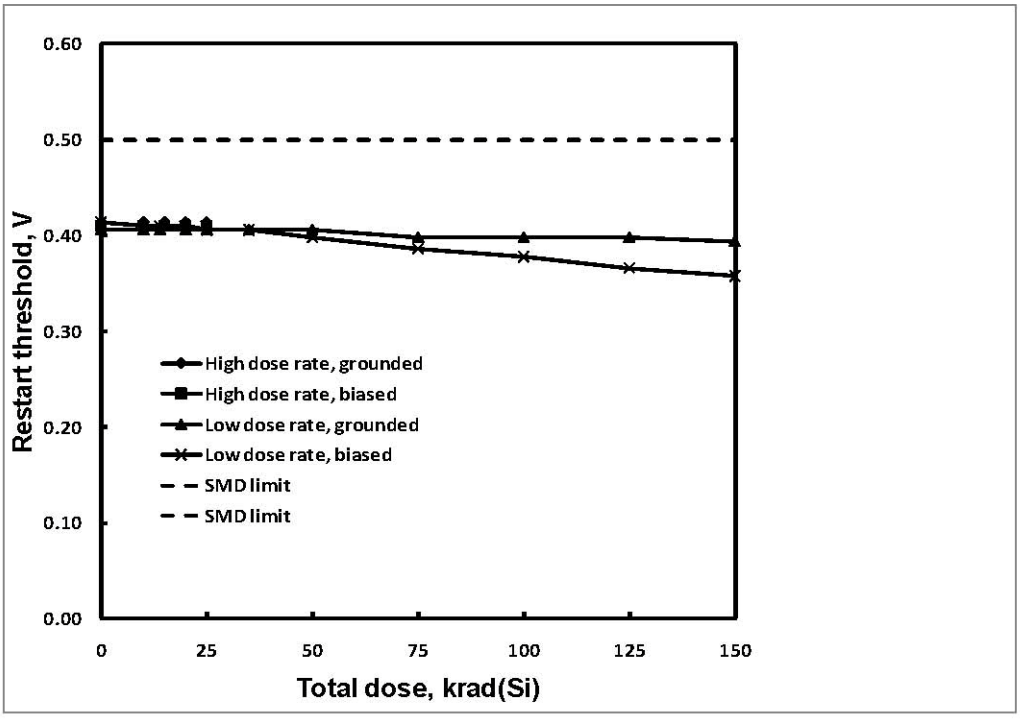


Fig. 33: IS-1825ASRH restart threshold as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 0.5V maximum.

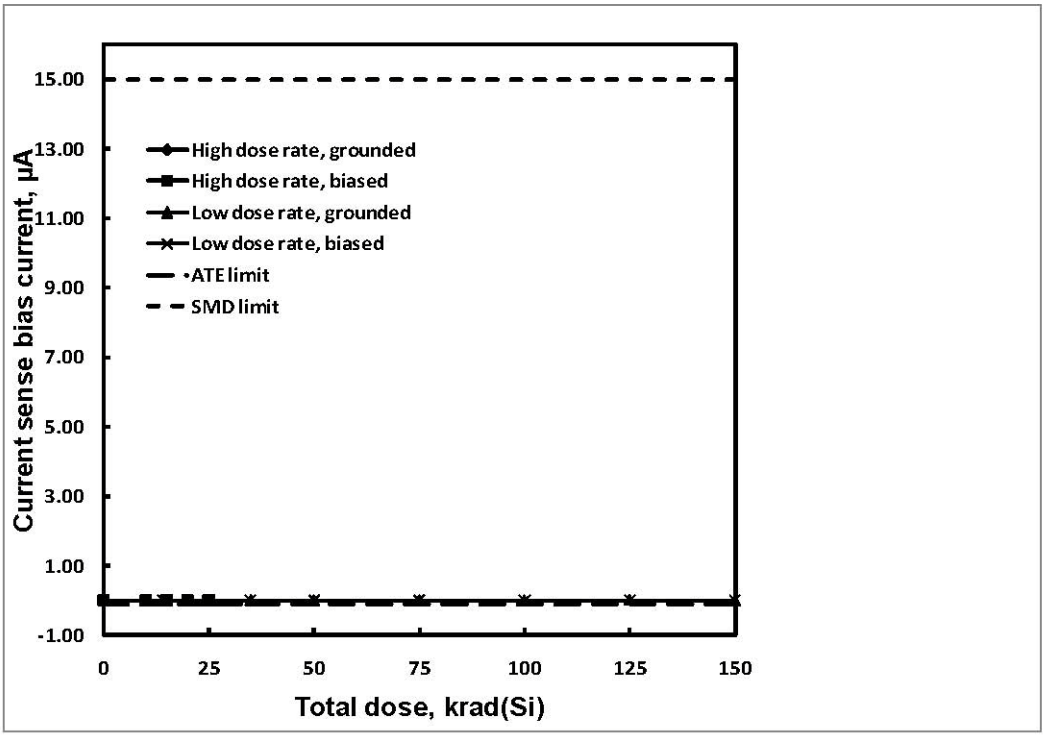


Fig. 34: IS-1825ASRH current sense bias current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 15µA maximum; the 0mA lower bound is an ATE limit.

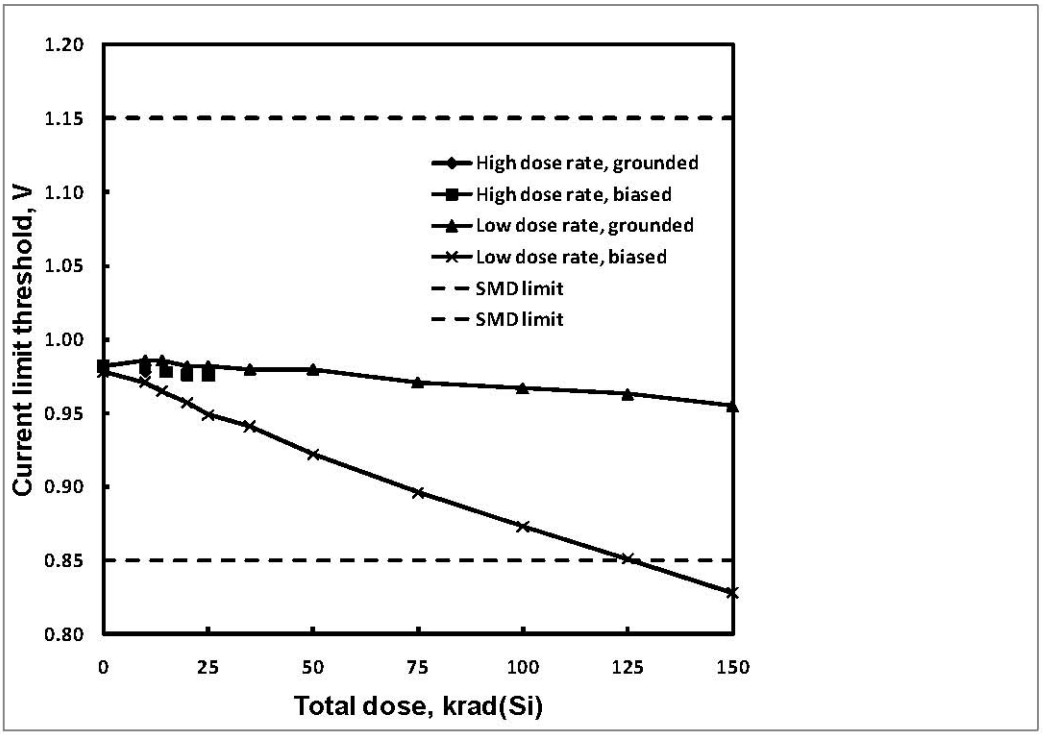


Fig. 35: IS-1825ASRH current limit threshold as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 0.85V to 1.15V.

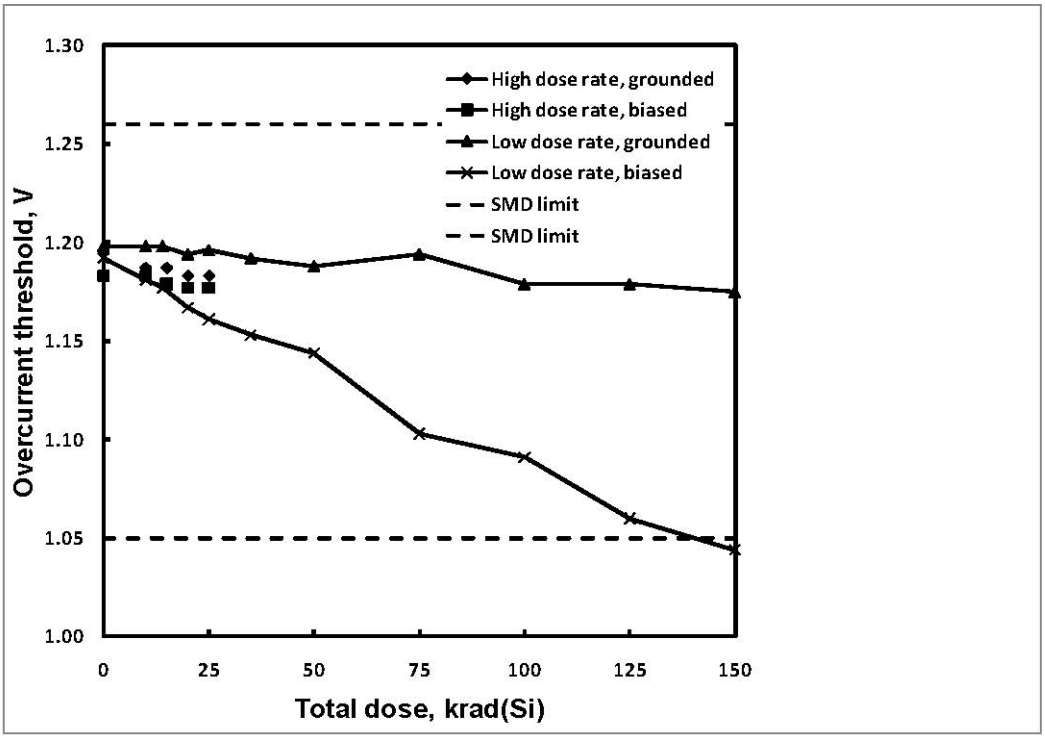


Fig. 36: IS-1825ASRH overcurrent threshold as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 1.05V to 1.26V.

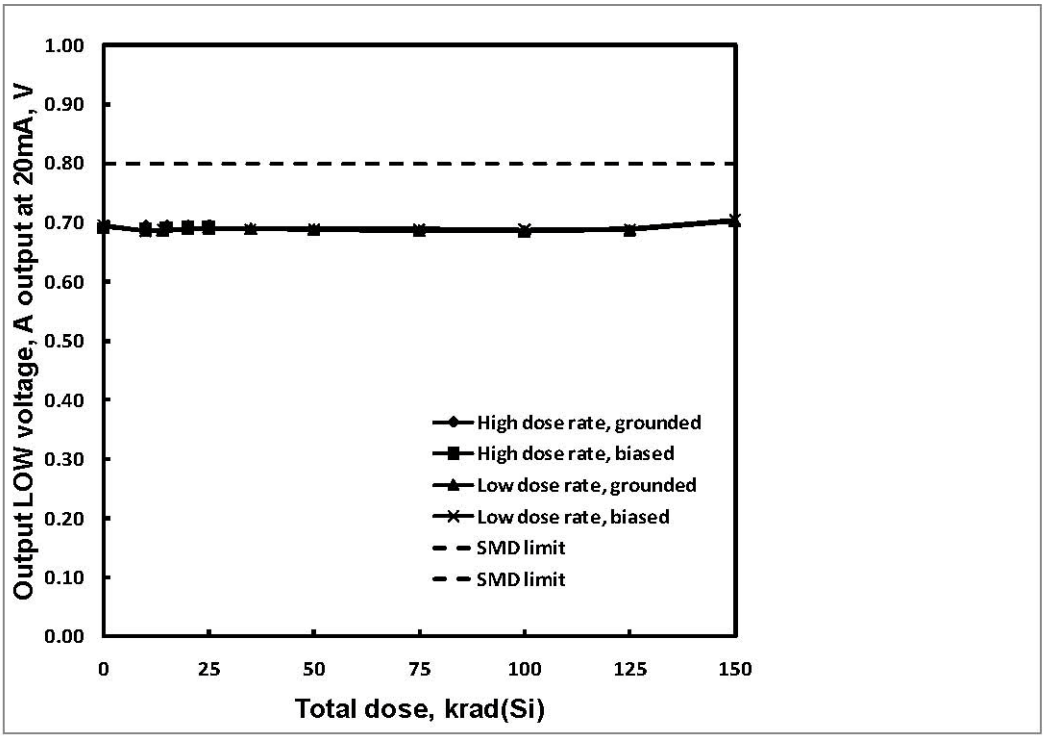


Fig. 37: IS-1825ASRH output LOW voltage, A output at 20mA, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 0.8V maximum.

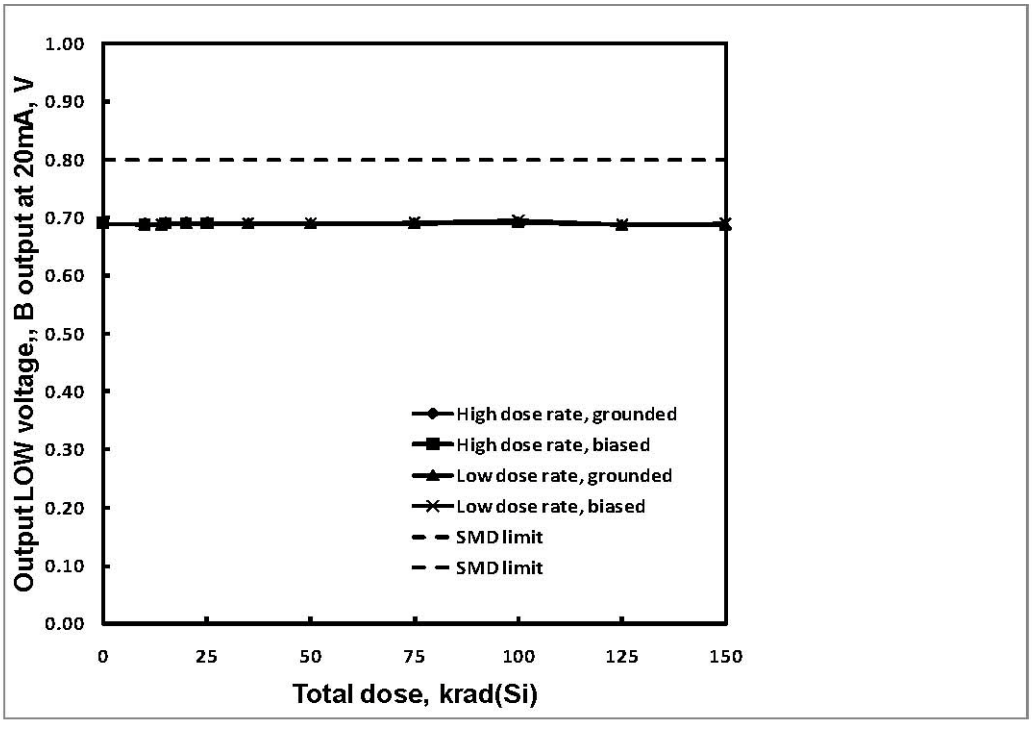


Fig. 38: IS-1825ASRH output LOW voltage, B output at 20mA, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 0.8V maximum.

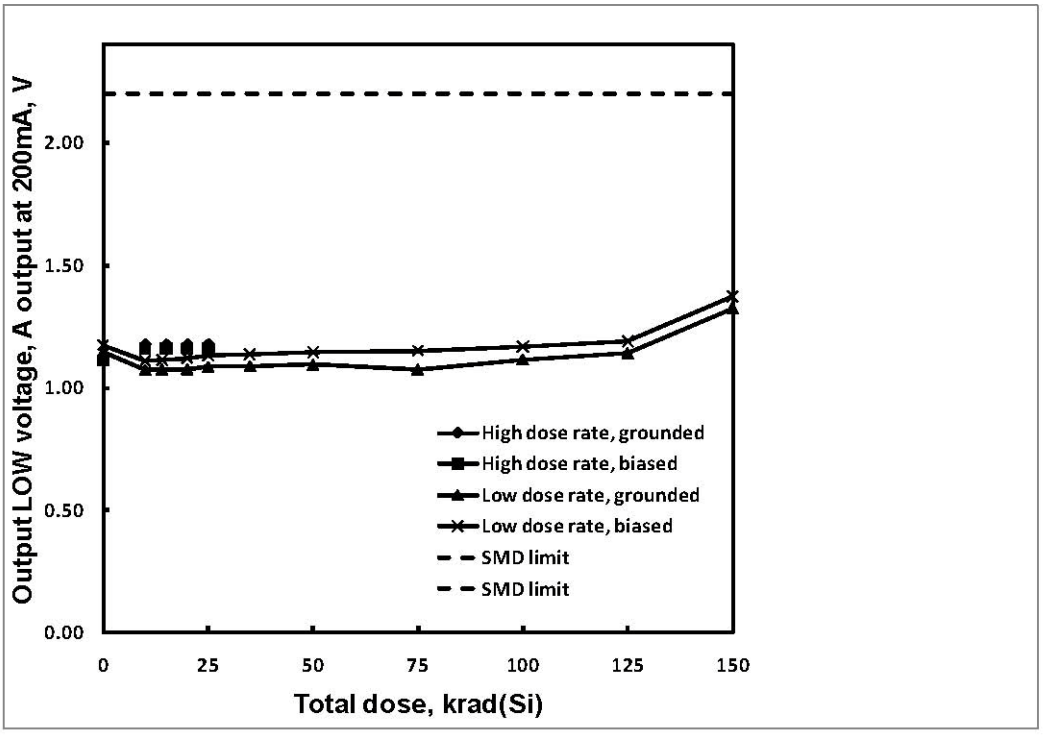


Fig. 39: IS-1825ASRH output LOW voltage, A output at 200mA, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 2.2V maximum.

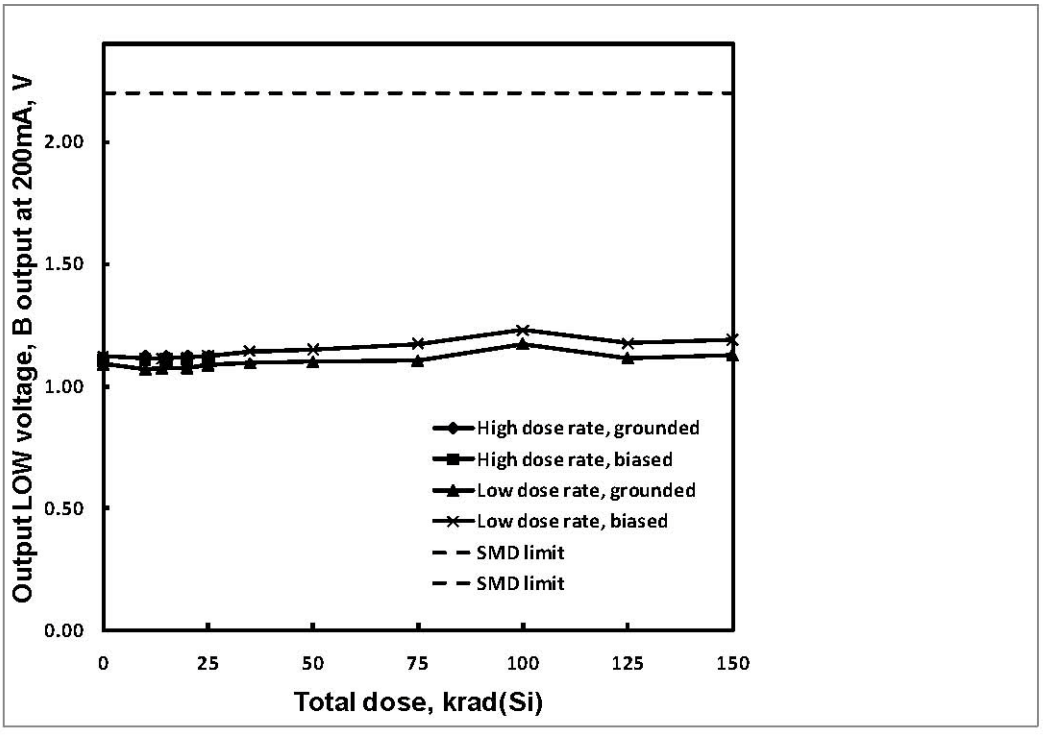


Fig. 40: IS-1825ASRH output LOW voltage, B output at 200mA, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 2.2V maximum.

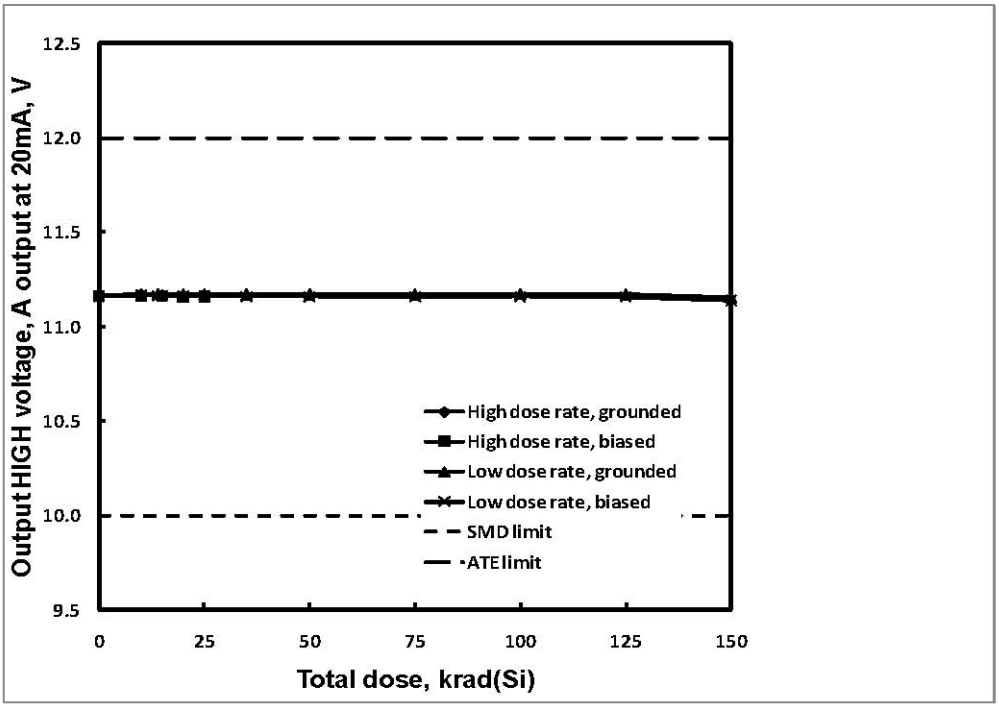


Fig. 41: IS-1825ASRH output HIGH voltage, A output at 20mA, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 10V minimum; the 12V upper bound is an ATE limit.

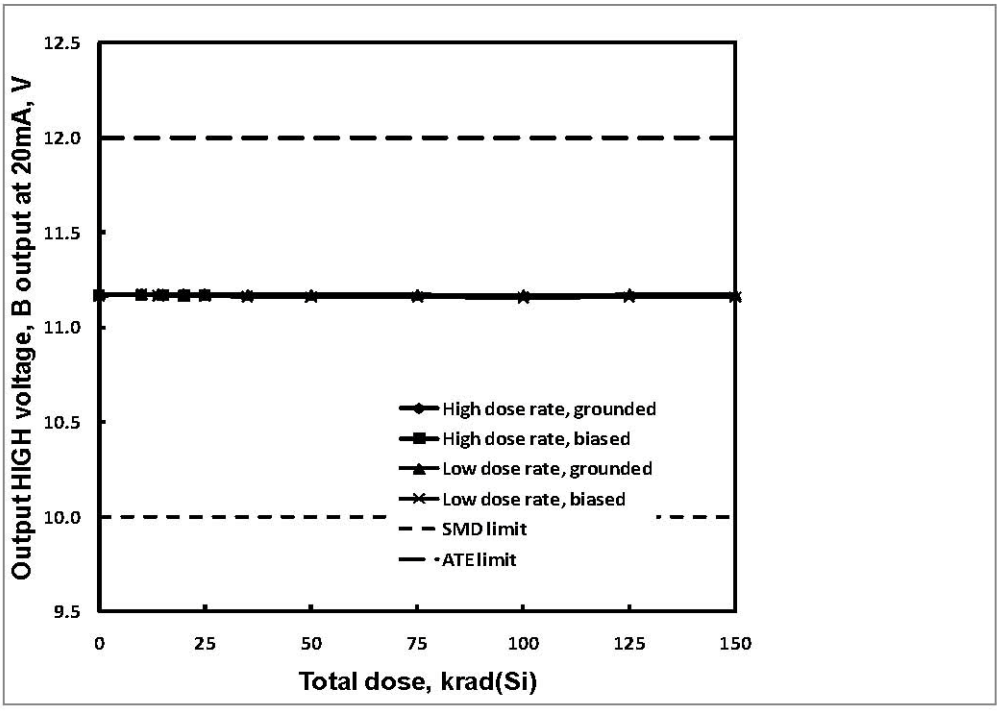


Fig. 42: IS-1825ASRH output HIGH voltage, B output at 20mA, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 10V minimum; the 12V upper bound is an ATE limit.

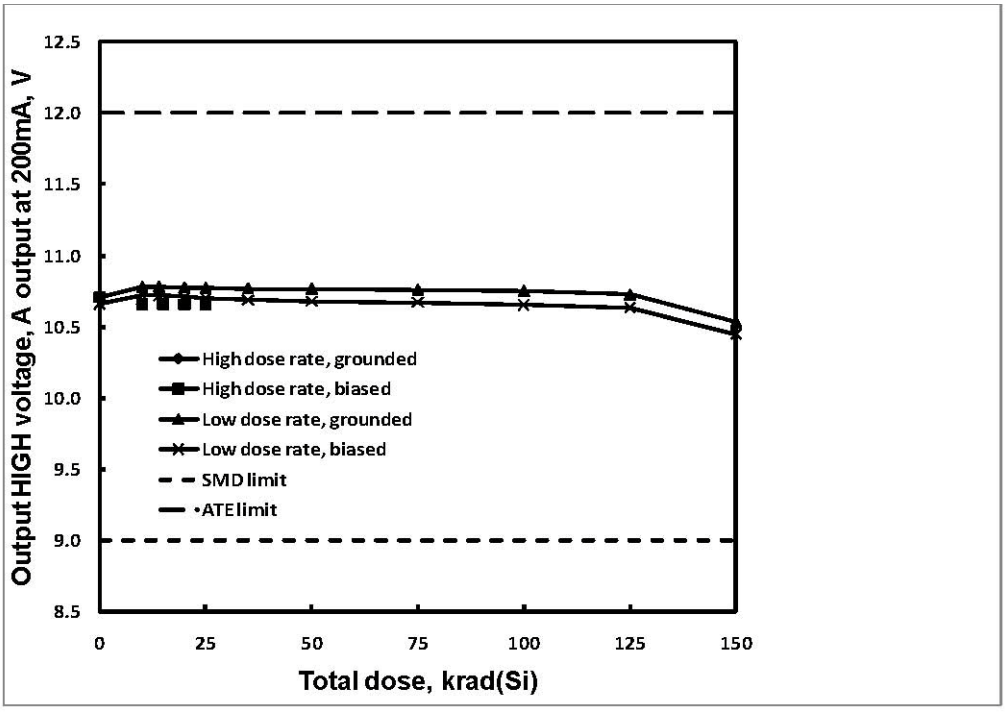


Fig. 43: IS-1825ASRH output HIGH voltage, A output at 200mA, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 9V minimum; the 12V upper bound is an ATE limit.

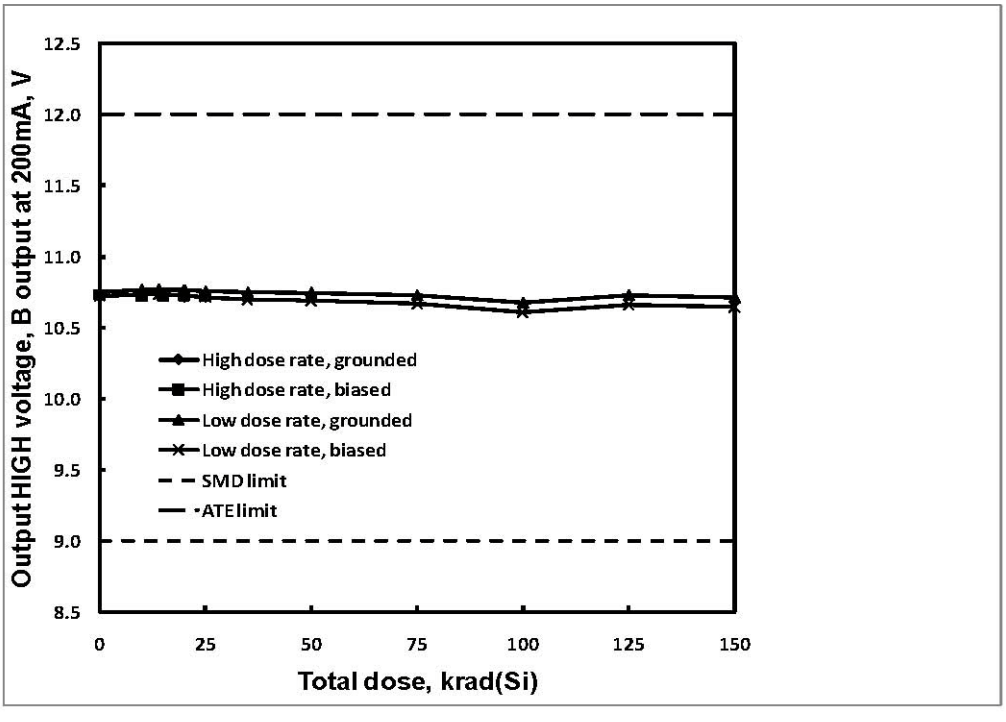


Fig. 44: IS-1825ASRH output HIGH voltage, B output at 200mA, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 9V minimum; the 12V upper bound is an ATE limit.

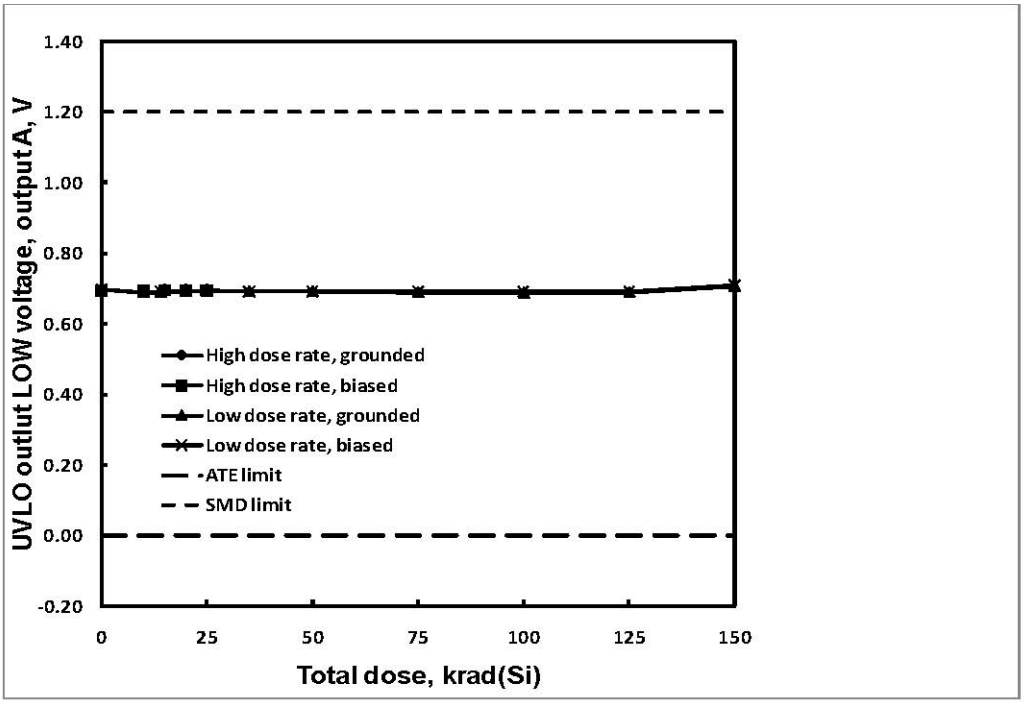


Fig. 45: IS-1825ASRH undervoltage lockout (UVLO) output LOW voltage, A output, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 1.2V maximum; the 0V lower bound is an ATE limit.

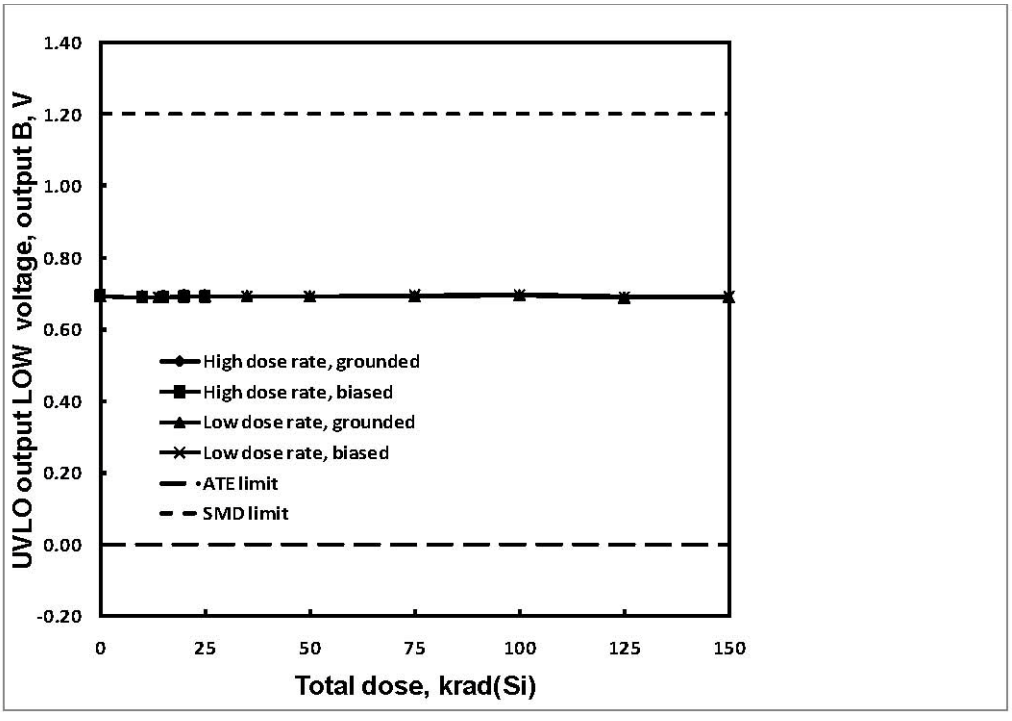


Fig. 46: IS-1825ASRH undervoltage lockout (UVLO) output LOW voltage, B output, as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 1.2V maximum; the 0V lower bound is an ATE limit.

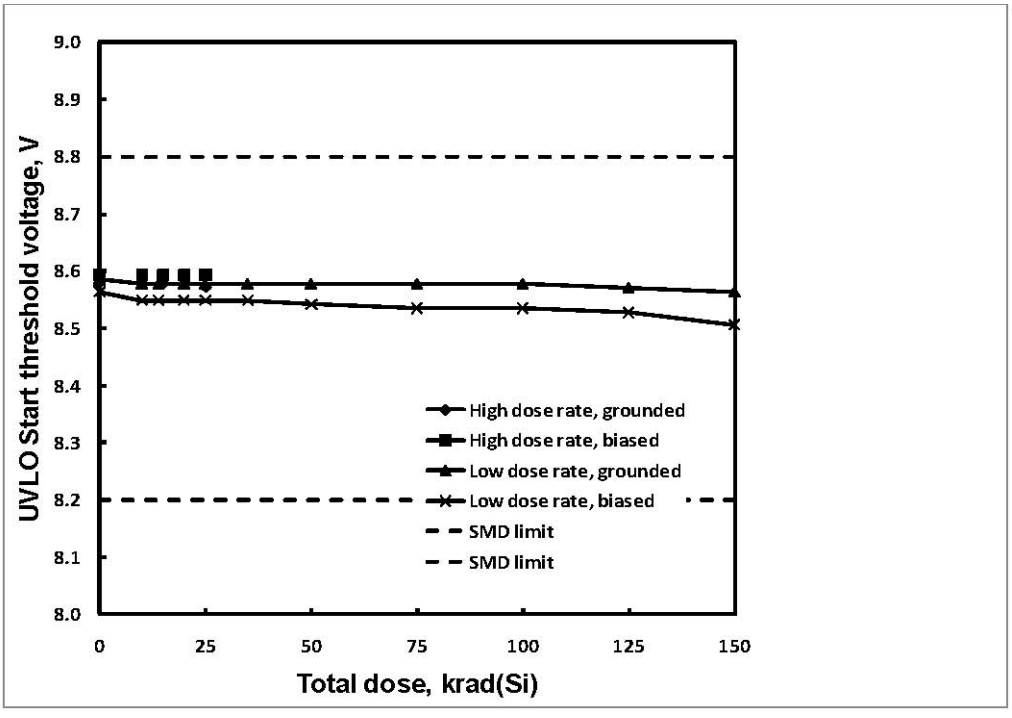


Fig. 47: IS-1825ASRH undervoltage lockout (UVLO) start threshold voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 8.2V to 8.8V.

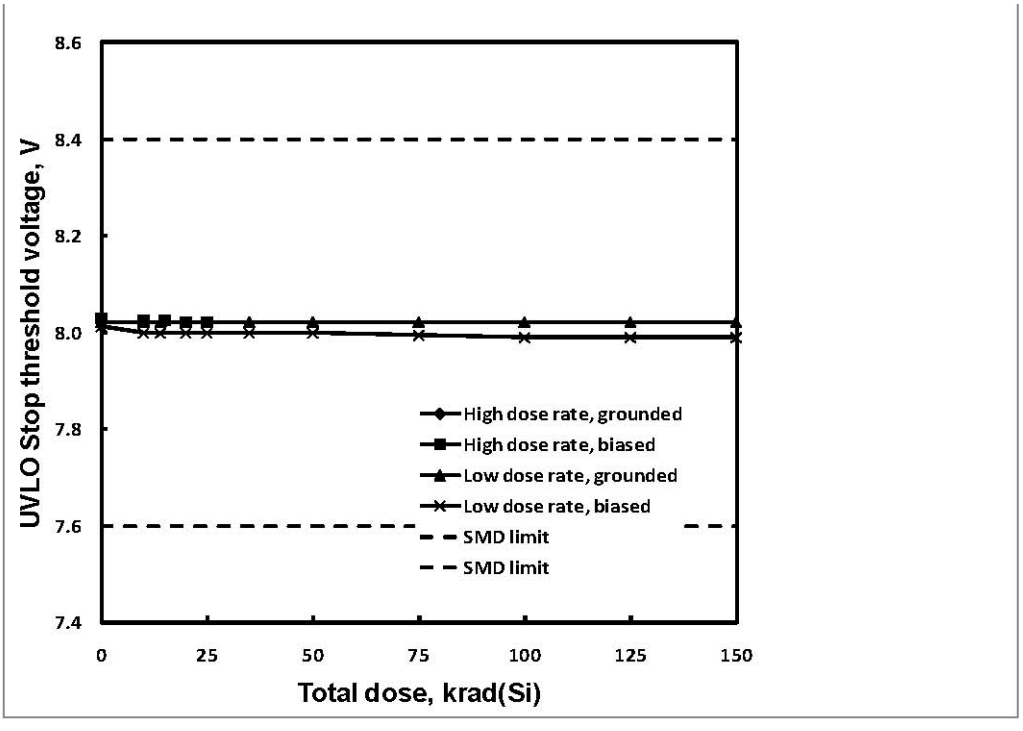


Fig. 48: IS-1825ASRH undervoltage lockout (UVLO) stop threshold voltage as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 7.6V to 8.4V.

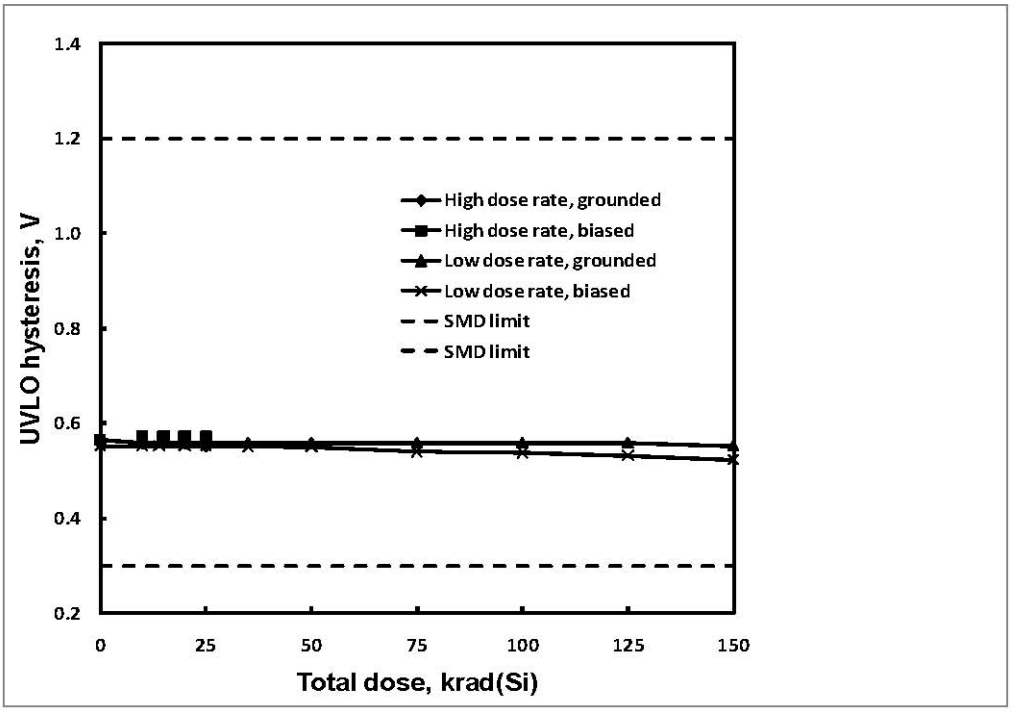


Fig. 49: IS-1825ASRH undervoltage lockout (UVLO) hysteresis as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limits are 0.3V to 1.2V.

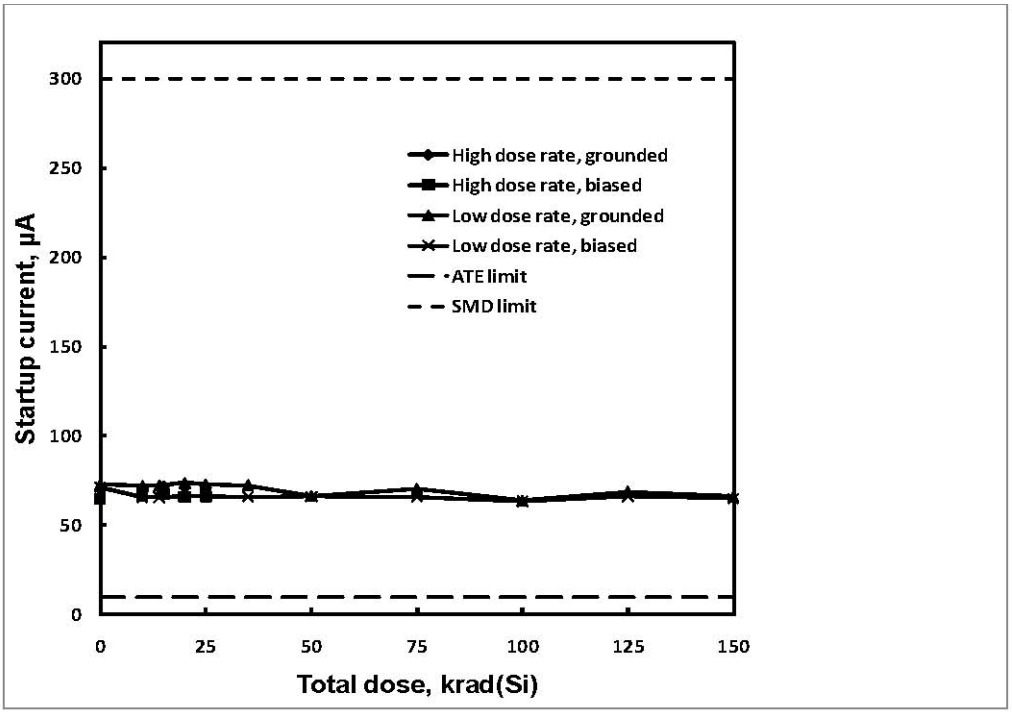


Fig. 50: IS-1825ASRH startup current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 300µA maximum; the 10µA lower bound is an ATE limit.

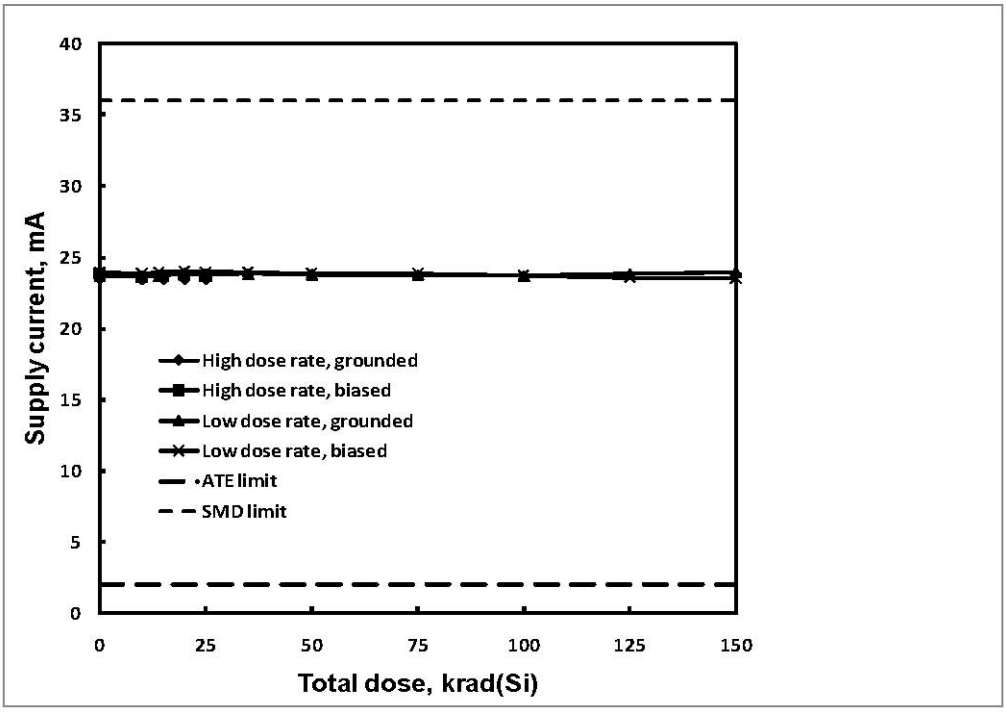


Fig. 51: IS-1825ASRH startup current as a function of total dose irradiation at low and high dose rate for the unbiased and biased cases. The post-irradiation SMD limit is 36mA maximum; the 2mA lower bound is an ATE limit.

6: Conclusion

This document reports results of a total dose test of the IS-1825ASRH dual output PWM. Parts were tested at low and high dose rate under biased and unbiased conditions as outlined in MILSTD-883 Test Method 1019.7, to a maximum total dose of 150krad(Si) at low dose rate and 25krad(Si) at high dose rate.

In 2003 the IS-1825ASRH was tested in collaboration with Harris Corporation using an early accelerated low dose test protocol, consisting of irradiation at 10rad(Si)/s at an ambient temperature of 100°C. Using this approach, the IS-1825ASRH was tested to 25krad(Si). Samples showed significant parametric degradation. The current test was undertaken to determine the response of the part to true low dose rate irradiation. A high dose rate test was run up to 25krad(Si) as a baseline.

The bias configuration used for both the high and low dose rate tests was modified from the current SMD configuration. This change was made due to concerns about disabling the oscillator through tying the RT terminal to 15V. As both configurations are static and are used to apply a DC electric field across the MOSFET device gate oxide, total dose tests for both configurations are expected to correlate well.

The great majority of parameters were very stable over low dose rate irradiation. After 150krad(Si) at low dose rate the error amplifier input offset voltage and input offset current median showed minor shifts but were well within the SMD limits. Also after 150krad(Si) at low dose rate, the PWM comparator ramp offset voltage, current limit threshold and overcurrent threshold medians were near their respective specification limits.

The part is considered moderately low dose rate sensitive but remains within the SMD post-irradiation limits to a maximum of 100krad(Si) in this environment. We also observed some bias sensitivity in the low dose rate results, with biased irradiation clearly worst-case.

7: Appendices

7.1: Reported parameters.

Fig.	Parameter	SMD limit, low	SMD limit, high	Units	Notes
3	Reference output voltage	4.92	5.28	V	
4	Line regulation	-20	+20	mV	
5	Load regulation	-50	+50	mV	
6	Total output variation	4.92	5.28	V	VS=12V, IL=1mA
7	Total output variation	4.92	5.28	V	VS=20V, IL=1mA
8	Total output variation	4.92	5.28	V	VS=12V, IL=10mA
9	Total output variation	4.92	5.28	V	VS=20V, IL=10mA
10	Reference short circuit current	20		mA	
11	Oscillator frequency	300	425	KHz	
12	Oscillator frequency PSRR	-3	+3	%	
13	Oscillator total frequency variation	300	425	KHz	VS=12V
14	Oscillator total frequency variation	300	425	KHz	VS=20V
15	Clock output HIGH voltage	3.75		V	
16	Clock output LOW voltage		0.2	V	
17	Error amplifier input offset voltage	-10	+10	mV	
18	Error amplifier input bias current	-2	+2	µA	
19	Error amplifier input offset current	-2	+2	µA	
20	Error amplifier open loop gain	60		dB	
21	Error amplifier common mode rejection ratio	65		dB	
22	Error amplifier power supply rejection ratio	70		dB	
23	Error amplifier output sink current	+1		mA	
24	Error amplifier output source current	-0.5		mA	
25	Error amplifier output HIGH voltage	4		V	
26	Error amplifier output LOW voltage		1	V	
27	Comparator ramp bias current		-8	µA	
28	Duty cycle range	40		%	Output A
29	Duty cycle range	40		%	Output B
30	Ramp offset	0.81		V	
31	Softstart charge current	8	25	µA	
32	Softstart discharge current	0.1	0.5	mA	
33	Restart threshold		0.5	V	
34	Current sense bias current		15	µA	

	35	Current limit threshold	0.85	1.15	V	
	36	Overcurrent threshold	1.05	1.26	V	
	37	Output LOW voltage	0.8		V	Output A, 20mA
	38	Output LOW voltage	0.8		V	Output B, 20mA
	39	Output LOW voltage	2.2		V	Output A, 200mA
	40	Output LOW voltage	2.2		V	Output B, 200mA
	41	Output HIGH voltage	10		V	Output A, 20mA
	42	Output HIGH voltage	10		V	Output B, 20mA
	43	Output HIGH voltage	9		V	Output A, 200mA
	44	Output HIGH voltage	9		V	Output B, 200mA
	45	UVLO output LOW voltage		1.2	V	Output A
	46	UVLO output LOW voltage		1.2	V	Output B
	47	Start threshold voltage	8.2	8.8	V	
	48	Stop threshold voltage	7.6	8.4	V	
	49	UVLO hysteresis	0.3	1.2	V	
	50	Startup current		300	µA	
	51	Supply current		36	mA	

Note 1: Limits are taken from Standard Microcircuit Drawing (SMD) 5962-02511.

8: Document revision history

Revision	Date	Pages	Comments
0	October 2010	All	Original issue
1	June 2012		Added references to the EH devices and the 1823A/BSRH