
RS-485 Drivers and Receivers

Functional Principles of RS-485 Drivers and Receivers

Abstract

The RS-485 standard specifies the electrical characteristics of differential drivers and receivers in multi-point networks but does not explain their functional principles. This document explains how the differential line signals are generated by the driver and processed by the receiver.

Contents

1. Driver Functional Principle	2
2. Receiver Functional Principle	3
3. Revision History	4

List of Figures

Figure 1. Driver with Drive Logic and H-Bridge Output	2
Figure 2. Driver Differential and Common-Mode Output Voltages	2
Figure 3. Mixed, Differential, and Common-Mode Representations of an RS-485 Driver	3
Figure 4. Input Voltage Divider with Comparator	3
Figure 5. Input Voltage Attenuation and Biasing	3

1. Driver Functional Principle

An RS-485 driver consists of a drive logic and four output transistors (Q1 to Q4) in an H-bridge configuration. The drive logic becomes active when the driver enable pin (DE) is asserted high.

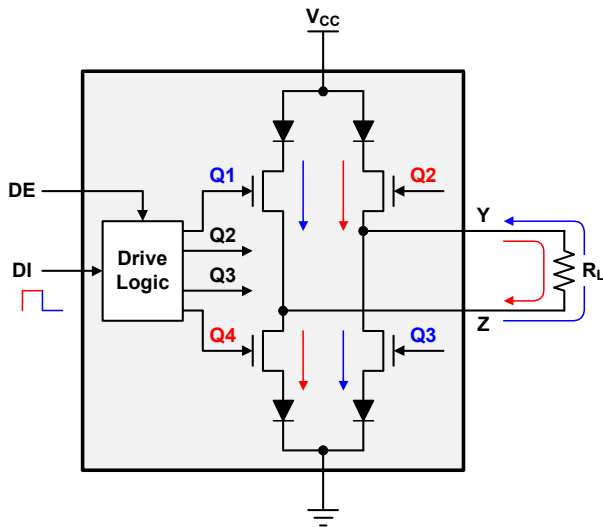


Figure 1. Driver with Drive Logic and H-Bridge Output

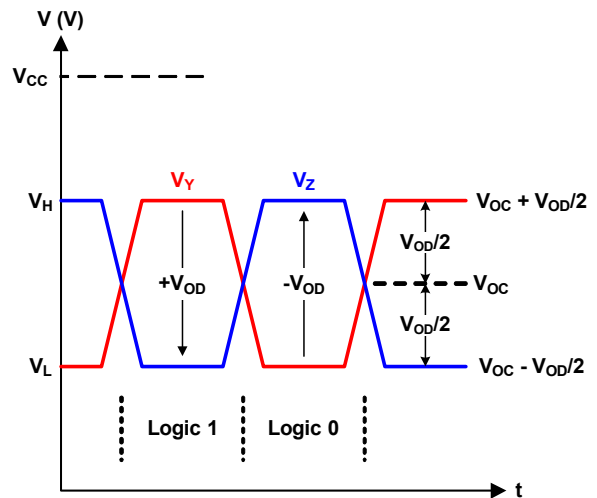


Figure 2. Driver Differential and Common-Mode Output Voltages

A high applied to the data input (DI) turns on Q2 and Q4 and disables Q1 and Q3. This configuration causes current to flow through R_L from Output Y to Output Z. A low applied to DI turns Q2 and Q4 off and enables Q1 and Q3, which causes the current to flow in the opposite direction, from Z to Y.

Each transistor has a diode in series to prevent reverse leakage current from flowing into the transistor if the bus voltage either rises above V_{CC} or drops below ground. When a driver drives a loaded bus, the forward voltages of the diodes and the voltage drops across the $r_{DS(ON)}$ resistance of the transistors causing the output voltages, V_Y and V_Z , to never reach the supply rails. Instead, both outputs switch alternately between the high and low voltage levels, V_H and V_L (Figure 2).

In general, the differential output voltage, V_{OD} , is the difference between the high and low-level output voltages:

$$(EQ. 1) \quad V_{OD} = V_H - V_L$$

However, in practice V_{OD} is defined as $V_Y - V_Z$, so V_Y is referenced to V_Z . For $V_Y > V_Z$, V_{OD} is positive and represents a binary 1 or logic high at DI. For $V_Y < V_Z$, V_{OD} is negative and indicates a binary 0 or logic low at DI.

As both outputs switch within the positive voltage range, the DC-component is common to both outputs. This voltage is the driver output common-mode voltage, V_{OC} , and is defined in Equation 2:

$$(EQ. 2) \quad V_{OC} = \frac{V_H + V_L}{2}$$

Inserting Equation 1 into Equation 2 presents the output voltages in their common-mode and differential components:

$$(EQ. 3) \quad V_H = V_{OC} + \frac{V_{OD}}{2} \quad \text{and} \quad V_L = V_{OC} - \frac{V_{OD}}{2}$$

The driver can therefore be shown as a common-mode voltage source superimposed by two complementary, differential voltages:

$$(EQ. 4) \quad V_Y = V_{OC} \pm \frac{V_{OD}}{2} \quad \text{and} \quad V_Z = V_{OC} \mp \frac{V_{OD}}{2}$$

These depictions will come in handy when evaluating a driver’s output drive capability, or explaining the removal of common-mode voltages through galvanic isolation ([Figure 3](#)).

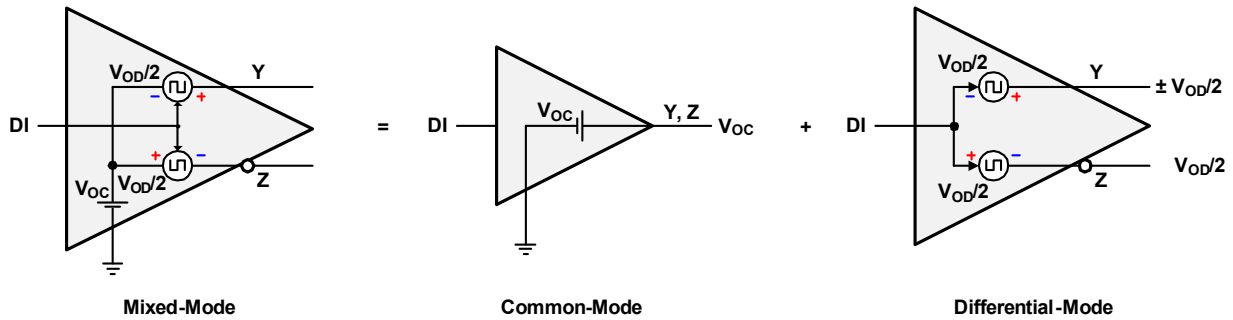


Figure 3. Mixed, Differential, and Common-Mode Representations of an RS-485 Driver

2. Receiver Functional Principle

An RS-485 receiver must be able to detect small differential bus signals as small as $\pm 200\text{mV}$ in the presence of large common-mode voltages that range from -7V to $+12\text{V}$. To detect these signals, the receiver consists of an input voltage divider with biasing stage, followed by a differential comparator. Its simplified equivalent circuit diagram is shown in [Figure 1 on page 2](#).

Here the voltage divider action between the input resistor, R_{IN} , and the biasing resistors, R_B , attenuate the line voltage by a gain factor of about $1/10$ to $1/12$. The attenuated input signal is then biased or level-shifted to approximately $V_{CC}/2$. This level-shift is necessary to enable the single-supply comparator to process large negative voltages.

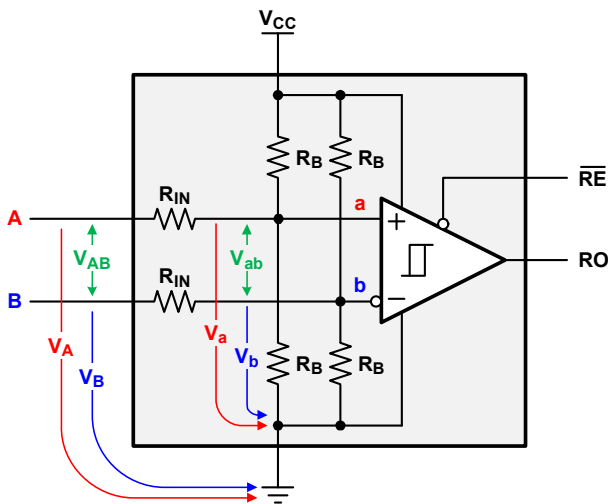


Figure 4. Input Voltage Divider with Comparator

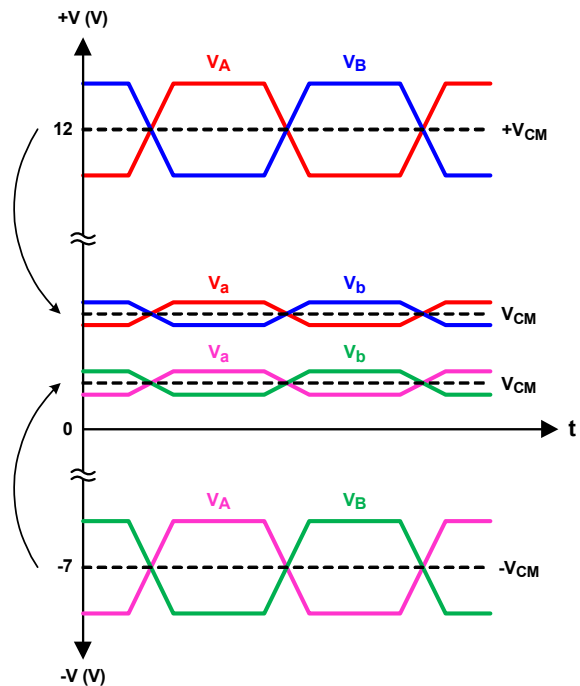


Figure 5. Input Voltage Attenuation and Biasing

[Figure 5](#) shows how large positive and negative line voltages are attenuated and then level-shifted into the positive operating voltage range of the comparator. Expressing the line voltages V_A and V_B through their common-mode and differential components: $V_A = V_{CM} + V_D/2$ and $V_B = V_{CM} - V_D/2$ respectively, the internal comparator input voltages are:

$$(EQ. 5) \quad V_a = \left(V_{CM} + \frac{V_D}{2} \right) \cdot G_1 + V_{CC} \cdot G_2 \quad \text{and} \quad V_b = \left(V_{CM} - \frac{V_D}{2} \right) \cdot G_1 + V_{CC} \cdot G_2$$

where G_1 is the gain factor of the voltage divider and G_2 is the gain factor of the biasing stage.

The comparator input voltage is $V_{ab} = V_a - V_b = V_D \cdot G_1$, which is purely differential. Because the comparator only reacts to differential inputs, all common-mode and biasing voltage components are rejected.

Note: Internal biasing references the receiver input voltages to receiver ground, so it is not necessary to connect the driver and a remote receiver with a ground wire.

RS-485 is therefore known as a true 2-wire bus.

3. Revision History

Rev.	Date	Description
1.00	Jun.25.19	Updated equations 3 and 5. Updated disclaimer. Applied new format.
0.00	Apr.26.17	Initial release

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(Rev.4.0-1 November 2017)

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