RJK0452DPB

40V, 45A, 3.5mΩ max.
Silicon N Channel Power MOS FET
Power Switching

Features
- High speed switching
- Capable of 4.5 V gate drive
- Low drive current
- High density mounting
- Low on-resistance $R_{D\!S\!(on)} = 2.8 \text{ mΩ typ. (at } V_{GS} = 10 \text{ V)}$
- Pb-free
- Halogen-free

Outline
RENESAS Package code: PTZZ0005DA-A
(Package name: LFPAK)

Application
- Switching Mode Power Supply

Absolute Maximum Ratings

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source voltage</td>
<td>$V_{DSS}$</td>
<td>40</td>
<td>V</td>
</tr>
<tr>
<td>Gate to source voltage</td>
<td>$V_{GS}$</td>
<td>±20</td>
<td>V</td>
</tr>
<tr>
<td>Drain current</td>
<td>$I_D$</td>
<td>45</td>
<td>A</td>
</tr>
<tr>
<td>Drain peak current</td>
<td>$I_D(pulse)$</td>
<td>180</td>
<td>A</td>
</tr>
<tr>
<td>Body-drain diode reverse drain current</td>
<td>$I_{BR}$</td>
<td>45</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche current</td>
<td>$I_{AP}$</td>
<td>22.5</td>
<td>A</td>
</tr>
<tr>
<td>Avalanche energy</td>
<td>$E_{AS}$</td>
<td>40.5</td>
<td>mJ</td>
</tr>
<tr>
<td>Channel dissipation</td>
<td>$P_{ch}$</td>
<td>55</td>
<td>W</td>
</tr>
<tr>
<td>Channel to Case Thermal Resistance</td>
<td>$\theta_{ch-C}$</td>
<td>2.27</td>
<td>°C/W</td>
</tr>
<tr>
<td>Channel temperature</td>
<td>$T_{ch}$</td>
<td>150</td>
<td>°C</td>
</tr>
<tr>
<td>Storage temperature</td>
<td>$T_{stg}$</td>
<td>−55 to +150</td>
<td>°C</td>
</tr>
</tbody>
</table>

Notes:
1. PW ≤ 10 ms, duty cycle ≤ 1%
2. Value at $T_{ch} = 25^\circ \text{C}$, $R_g ≥ 50 \Omega$
3. $T_c = 25^\circ \text{C}$

This product is for the low voltage drive (≤ 10V).
If the driving voltage is over 10 V under normal conditions, please use the product for high gate to source cutoff voltage ($V_{GS\!(off)}$) which characteristics has been improved.
# Electrical Characteristics

\( (T_a = 25^\circ\text{C}) \)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Drain to source breakdown voltage</td>
<td>( V_{\text{BR(DSS)}} )</td>
<td>40</td>
<td>—</td>
<td>—</td>
<td>V</td>
<td>( I_D = 10 \text{ mA}, V_{GS} = 0 \text{ V} )</td>
</tr>
<tr>
<td>Gate to source leak current</td>
<td>( I_{\text{GS}} )</td>
<td>—</td>
<td>—</td>
<td>( \pm 0.1 )</td>
<td>( \mu \text{A} )</td>
<td>( V_{GS} = \pm 20 \text{ V}, V_{DS} = 0 \text{ V} )</td>
</tr>
<tr>
<td>Zero gate voltage drain current</td>
<td>( I_{\text{DSS}} )</td>
<td>—</td>
<td>—</td>
<td>1</td>
<td>( \mu \text{A} )</td>
<td>( V_{DS} = 40 \text{ V}, V_{GS} = 0 \text{ V} )</td>
</tr>
<tr>
<td>Gate to source cutoff voltage</td>
<td>( V_{\text{GS(off)}} )</td>
<td>1.2</td>
<td>—</td>
<td>2.5</td>
<td>V</td>
<td>( V_{DS} = 10 \text{ V}, I_D = 1 \text{ mA} )</td>
</tr>
<tr>
<td>Static drain to source on state resistance</td>
<td>( R_{\text{DS(on)}} )</td>
<td>—</td>
<td>2.8</td>
<td>3.5</td>
<td>m( \Omega )</td>
<td>( I_D = 22.5 \text{ A}, V_{GS} = 10 \text{ V} ) ( ^{\text{Note4}} )</td>
</tr>
<tr>
<td>Forward transfer admittance</td>
<td>(</td>
<td>y_{FS}</td>
<td>)</td>
<td>—</td>
<td>108</td>
<td>—</td>
</tr>
<tr>
<td>Input capacitance</td>
<td>( C_{\text{iss}} )</td>
<td>—</td>
<td>4030</td>
<td>—</td>
<td>pF</td>
<td>( V_{DS} = 10 \text{ V}, V_{GS} = 0 \text{ V}, ) ( f = 1 \text{ MHz} )</td>
</tr>
<tr>
<td>Output capacitance</td>
<td>( C_{\text{oss}} )</td>
<td>—</td>
<td>650</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Reverse transfer capacitance</td>
<td>( C_{\text{rss}} )</td>
<td>—</td>
<td>270</td>
<td>—</td>
<td>pF</td>
<td></td>
</tr>
<tr>
<td>Total gate charge</td>
<td>( Q_g )</td>
<td>—</td>
<td>26</td>
<td>—</td>
<td>nC</td>
<td>( V_{DD} = 10 \text{ V}, V_{GS} = 4.5 \text{ V}, I_D = 45 \text{ A} )</td>
</tr>
<tr>
<td>Gate to source charge</td>
<td>( Q_{gs} )</td>
<td>—</td>
<td>12</td>
<td>—</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>Gate to drain charge</td>
<td>( Q_{gd} )</td>
<td>—</td>
<td>6.6</td>
<td>—</td>
<td>nC</td>
<td></td>
</tr>
<tr>
<td>Turn-on delay time</td>
<td>( t_{\text{on}} )</td>
<td>—</td>
<td>18</td>
<td>—</td>
<td>ns</td>
<td>( V_{GS} = 10 \text{ V}, I_D = 22.5 \text{ A}, ) ( V_{DD} \approx 10 \text{ V}, R_L = 0.44 \text{ ( \Omega )}, R_g = 4.7 \text{ ( \Omega )} )</td>
</tr>
<tr>
<td>Rise time</td>
<td>( t_r )</td>
<td>—</td>
<td>6.0</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Turn-off delay time</td>
<td>( t_{\text{off}} )</td>
<td>—</td>
<td>65</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Fall time</td>
<td>( t_f )</td>
<td>—</td>
<td>8.5</td>
<td>—</td>
<td>ns</td>
<td></td>
</tr>
<tr>
<td>Body–drain diode forward voltage</td>
<td>( V_{DF} )</td>
<td>—</td>
<td>0.83</td>
<td>1.1</td>
<td>V</td>
<td>( I_F = 45 \text{ A}, V_{GS} = 0 \text{ V} ) ( ^{\text{Note4}} )</td>
</tr>
<tr>
<td>Body–drain diode reverse recovery time</td>
<td>( t_{\text{rr}} )</td>
<td>—</td>
<td>35</td>
<td>—</td>
<td>ns</td>
<td>( I_F = 45 \text{ A}, V_{GS} = 0 \text{ V} ) ( di_i/dt = 100 \text{ A/( \mu \text{s} )} )</td>
</tr>
</tbody>
</table>

Notes: 4. Pulse test
Main Characteristics

![Power vs. Temperature Derating](image1)

- Channel Dissipation vs. Case Temperature
- Power vs. Temperature Derating

![Maximum Safe Operation Area](image2)

- Maximum Safe Operation Area
- Operation in this area is limited by $R_{DS(on)}$

![Typical Output Characteristics](image3)

- Typical Output Characteristics
- $V_{DS} = 10\, V$

![Typical Transfer Characteristics](image4)

- Typical Transfer Characteristics
- $V_{GS} = 4.5\, V$

![Drain to Source Saturation Voltage vs. Gate to Source Voltage](image5)

- Drain to Source Saturation Voltage vs. Gate to Source Voltage
- $V_{DS} = 10\, V$

![Static Drain to Source on State Resistance vs. Drain Current](image6)

- Static Drain to Source on State Resistance vs. Drain Current
- Operation in this area is limited by $R_{DS(on)}$

![Channel Dissipation vs. Case Temperature](image7)

- Channel Dissipation vs. Case Temperature
- $Tc = 25\, ^\circ C$

![Operation in this area is limited by $R_{DS(on)}$](image8)

- Operation in this area is limited by $R_{DS(on)}$
- $1\, \mu s$

![Input Characteristics](image9)

- Input Characteristics
- $PW = 10\, ms$

![DC Operation](image10)

- DC Operation
- $1\, ms$
Normalized Transient Thermal Impedance vs. Pulse Width

Avalanche Test Circuit

Avalanche Waveform

E_{AS} = \frac{1}{2} L \cdot I_{AP}^2 \cdot \frac{V_{DSS}}{V_{DSS} - V_{DD}}

Switching Time Test Circuit

Switching Time Waveform

Vin Monitor

Vout Monitor

D.U.T.

V_{DS} Monitor

R_g

L

V_{DSS}

Vin 15 V

60 \Omega

V_{DD}

D.U.T.

R_g

Vin 10 V

D.U.T.

R_L

V_{DS}

V_{DSS} - 10 V

Vin 10 V

10% 90%

V_{out}

10% 90%

V_{in}

10% 90%

t_{d(on)}

t_r

t_{d(off)}
### Package Dimensions

<table>
<thead>
<tr>
<th>Package Name</th>
<th>JETTA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>Mass [Typ]</th>
</tr>
</thead>
<tbody>
<tr>
<td>LPPAK</td>
<td>SC-100</td>
<td>P122003C0-A</td>
<td>LPPARV</td>
<td>0.080g</td>
</tr>
</tbody>
</table>

Unit: mm

![Package Diagram]

(Ni/Pd/Au plating)

### Ordering Information

<table>
<thead>
<tr>
<th>Part No.</th>
<th>Quantity</th>
<th>Shipping Container</th>
</tr>
</thead>
<tbody>
<tr>
<td>RJK0452DPB-00-J5</td>
<td>2500 pcs</td>
<td>Taping</td>
</tr>
</tbody>
</table>
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