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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A013A/E	Rev.	1.00
Title	Revised information of S7G2 User's Manual from Rev.1.20		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S7 Series S7G2	Lot No. All lots	Reference Document	S7G2 User's Manual: Microcontrollers, Rev.1.20		

1. 59.3.8 PWM Delay Generation Circuit Timing

[Before]

Item	Min	Typ	Max	Unit	Test condition
Resolution	-	260	-	ps	PCLKD = 120MHz
DNL*1	-	±2.0	-	LSB	-

[After]

Item	Min	Typ	Max	Unit	Test condition
Operation frequency	80	-	120	MHz	-
Resolution	-	260	-	ps	PCLKD = 120MHz
DNL*1	-	±2.0	-	LSB	-

2. Table 59.33 Graphics LCD Controller timing and Figure 59.74 LCD output rise and fall times

[Before]

Table 59.33 Graphics LCD Controller timing

Conditions:
LCD_CLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
LCD_DATA: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Typ	Max	Unit	Test conditions
LCD_EXTCLK input clock frequency		t_{Ecyc}	-	-	60*1	MHz	Figure 59.71
LCD_EXTCLK input clock low pulse width		t_{WL}	0.45	-	0.55	t_{Ecyc}	
LCD_EXTCLK input clock high pulse width		t_{WH}	0.45	-	0.55		
LCD_CLK output clock frequency		t_{Lcyc}	-	-	60*1	MHz	Figure 59.72
LCD_CLK output clock low pulse width		t_{LOL}	0.4	-	0.6	t_{Lcyc}	Figure 59.72
LCD_CLK output clock high pulse width		t_{LOH}	0.4	-	0.6	t_{Lcyc}	Figure 59.72
LCD data output delay timing	_A or _B combinations*2	t_{DD}	–3.5	-	4	ns	Figure 59.73
	_A and _B combinations*3		–5.0	-	5.5		
LCD data output rise time (0.8 to 2.0 V)		t_{Dr}	-	-	2		Figure 59.74
LCD data output fall time (2.0 to 0.8 V)		t_{Df}	-	-	2		

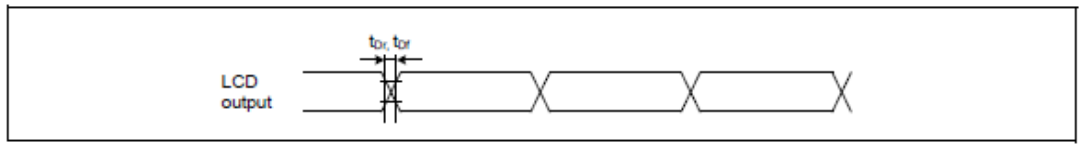

Figure 59.74 LCD output rise and fall times

[After]

Table 59.33 Graphics LCD Controller timing

Conditions:
LCD_CLK: High drive output is selected in the port drive capability bit in the PmnPFS register.
LCD_DATA: Middle drive output is selected in the port drive capability bit in the PmnPFS register.

Item		Symbol	Min	Typ	Max	Unit	Test conditions
LCD_EXTCLK input clock frequency		t_{Ecyc}	-	-	60*1	MHz	Figure 59.71
LCD_EXTCLK input clock low pulse width		t_{WL}	0.45	-	0.55	t_{Ecyc}	
LCD_EXTCLK input clock high pulse width		t_{WH}	0.45	-	0.55		
LCD_CLK output clock frequency		t_{Lcyc}	-	-	60*1	MHz	Figure 59.72
LCD_CLK output clock low pulse width		t_{LOL}	0.4	-	0.6	t_{Lcyc}	Figure 59.72
LCD_CLK output clock high pulse width		t_{LOH}	0.4	-	0.6	t_{Lcyc}	Figure 59.72
LCD data output delay timing	_A or _B combinations*2	t_{DD}	–3.5	-	4	ns	Figure 59.73
	_A and _B combinations*3		–5.0	-	5.5		

"Figure 59.74 LCD output rise and fall times" are deleted

3. 33. USB 2.0 High-Speed Module (USBHS)

3.1. USBHS block diagram

[Before]

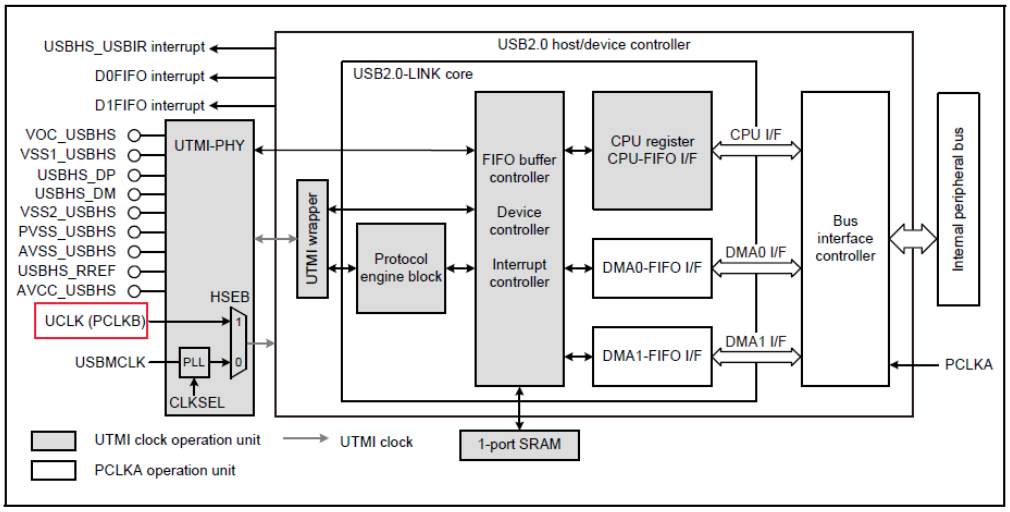

Figure 33.1 USBHS block diagram

[After]

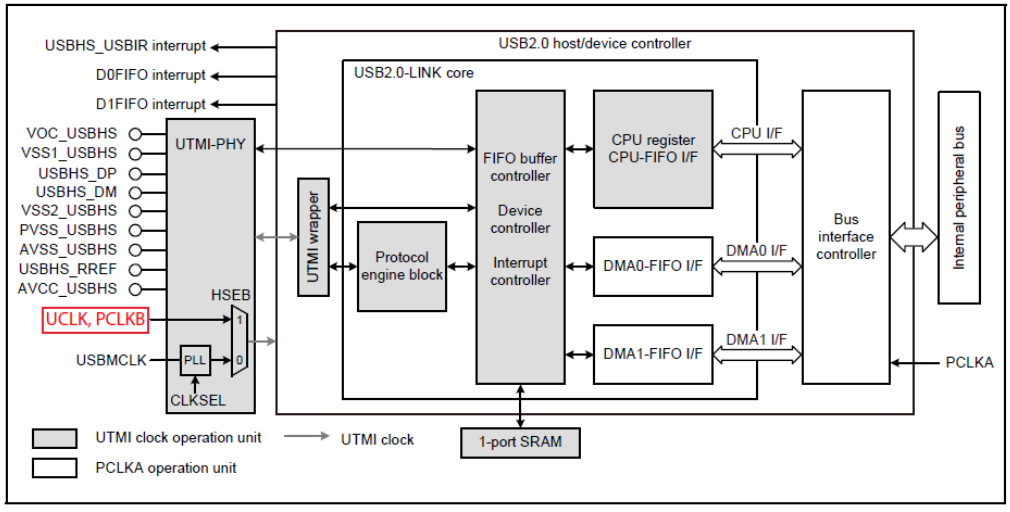

Figure 33.1 USBHS block diagram

3.2. 33.2.1 System Configuration Control Register (SYSCFG)

[Before]

USBE bit (USBHS Operation Enable)

The USBE bit enables or disables operation of USBHS.

Changing the USBE bit from 1 to 0 initializes the bits listed in Table 33.3. Only change this bit after specifying the input clock in the PHYSET.CLKSEL[1:0] bits and confirming that the PLLSTA.PLLLOCK flag is 1. In CL-only mode, change the USBE bit after setting the PHYSET.HSEB bit to 1. For the clock settings, see section 33.3.3, Supplying the Clock.

[After]

USBE bit (USBHS Operation Enable)

The USBE bit enables or disables operation of USBHS.

Changing the USBE bit from 1 to 0 initializes the bits listed in Table 33.3. Only change this bit after specifying the input clock in the PHYSET.CLKSEL[1:0] bits and confirming that the PLLSTA.PLLLOCK flag is 1. In CL-only mode, change the USBE bit after setting the PHYSET.HSEB bit to 1. At that time, the UCLK must be set to 48 MHz and PCLKB must be set to 60 MHz. For the clock settings, see section 33.3.3, Supplying the Clock.

3.3. 33.2.17 PHY Setting Register (PHYSET)

[Before]

HSEB bit (CL-only mode)

In CL-only mode, the USBHS requires supply clocks of 48 MHz generated in the Clock Generation Circuit. For the clock supply method, see section 9, Clock Generation Circuit.

[After]

HSEB bit (CL-only mode)

In CL-only mode, the USBHS requires supply clocks of 48 MHz and 60MHz generated in the Clock Generation Circuit. For the clock supply method, see section 9, Clock Generation Circuit.

3.4. 33.3.3 Supplying the Clock

2nd box in Figure 33.2 PHY clock settings.

[Before]

Peripheral settings: mainly USB clock supply

- Supply 60 MHz or 48 MHz in CL-only mode
- Supply 20 MHz or 24 MHz in non CL-only mode

[After]

Peripheral settings: mainly USB clock supply

- Supply 60 MHz and 48 MHz in CL-only mode
- Supply 20 MHz or 24 MHz in non CL-only mode

4. 33.2.9 D0FIFO Port Selection Register (D0FIFOSEL)
D1FIFO Port Selection Register (D1FIFOSEL)

[Before]

DREQE Bit (DMA/DTC Transfer Request Enable)

The DREQE bit enables or disables issuing of DMA or DTC transfer requests. To enable DMA or DTC transfer requests, set this bit to 1 after setting the CURPIPE[3:0] bits. To change the CURPIPE[3:0] setting, first set this bit to 0.

[After]

DREQE Bit (DMA/DTC Transfer Request Enable)

The DREQE bit enables or disables issuing of DMA or DTC transfer requests. Only change the settings of DREQE bit when the CURPIPE[3:0] bits are 0000b.To enable the DMA/DTC transfer request, set this bit to 1 after setting the CURPIPE[3:0] bits to 0000b, and then set the CURPIPE[3:0] bits to the PIPE number for the transfer.

5. 25.4.7 When Selecting AGT0 Underflow as the Count Source

[Before]

(1) Procedure for starting operation

1. Set AGT0 and AGT1.
2. Start the count operation of AGT0.
3. Start the count operation of AGT1.

(2) Procedure for stopping operation

1. Stop the count operation of AGT1.
2. Stop the count operation of AGT0.

[After]

(1) Procedure for starting operation

1. Set AGT0 and AGT1.
2. Start the count operation of AGT1.
3. Start the count operation of AGT0.

(2) Procedure for stopping operation

1. Stop the count operation of AGT0.
2. Stop the count operation of AGT1.
3. Stop the count source clock of AGT1. (Write "000b" in AGT1.AGTMR1.TCK[2:0] bits)