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RENESAS TECHNICAL UPDATE

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Title	Revised information of S7G2 User's Manual from Rev.1.00		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S7 Series S7G2	Lot No. All lots	Reference Document	S7G2 User's Manual: Microcontrollers, Rev.1.00		

1. 9.2.11 High-Speed On-Chip Oscillator Wait Control Register (HOCOWTCR)

• Modified the explanation of HSTS[2:0] as the following.

[Before]

The HSTS[2:0] bits must always be set to 110b.

[After]

HSTS[2:0] bits must be set to 110b. However, when using SCI0 in Snooze mode, HSTS[2:0 must be set to 010b.

2. 11.2.1 Standby Control Register (SBYCR)

• Modified the explanation of SSBY bit as the following.

[Before]

When using the HOCO clock to enter Software Standby mode, STCONR.STCON[1:0] must be set to 00b, and HOCOWTCR.STCON[2:0] must be set to 110b. This is not required when using SCI0 in Snooze mode.

[After]

When using the HOCO clock to enter Software Standby mode, STCONR.STCON[1:0] must be set to 00b, and HOCOWTCR.HSTS[2:0] must be set to 110b. However, when using SCI0 in Snooze mode, HOCOWTCR.HSTS[2:0] must be set to 010b.

3. 59.2.5 Operating and Standby Current

• Added Note 5 for normal mode and sleep mode at the table 59.7.

[Before]

59.2.5 Operating and Standby Current

Table 59.7 Operating and standby current (1/2)

Item				Symbol	LDO mode			DCDC mode			Unit	Test conditions
					Min	Typ	Max	Min	Typ	Max		
Supply current*1	High-speed mode	Maximum*2		I_{CC}	-	-	330	-	-	140	mA	ICLK = 240 MHz PCLKA = 120 MHz*6 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*4			-	45	-	-	24	-		
		Normal mode*3	All peripheral clocks enabled, code executing from flash		-	75	-	-	38	-		
			All peripheral clocks disabled, code executing from flash		-	32	-	-	18	-		
		Sleep mode*4			-	25	150	-	15	75		
		Increase during BGO operation	Data flash P/E		-	7	-	-	7	-		
			Code flash P/E		-	10	-	-	10	-		
	Low-speed mode*4				-	4.4	-	-	3	-		ICLK = 1 MHz
	Subosc-speed mode*4				-	3	-	-	2	-		ICLK = 32.768 kHz
	Software Standby mode				-	2.4	110	-	1.2	55		-
	mode	Power supplied to Standby SRAM and USB resume detecting unit			-	37	255	-	37	255	µA	VBAT ≠ VCC*7
					-	37	285	-	37	285		VBAT = VCC
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low-power function disabled		-	25	50	-	25	50		VBAT ≠ VCC*7
					-	25	80	-	25	80		VBAT = VCC
			Power-on reset circuit low-power function enabled		-	16	35	-	16	35		VBAT ≠ VCC*7
					-	16	65	-	16	65		VBAT = VCC

[After]

59.2.5 Operating and Standby Current

Table 59.7 Operating and standby current (1/2)

Item				Symbol	LDO mode			DCDC mode			Unit	Test conditions
					Min	Typ	Max	Min	Typ	Max		
Supply current*1	High-speed mode	Maximum*2		I_{CC}	-	-	330	-	-	140	mA	ICLK = 240 MHz PCLKA = 120 MHz*6 PCLKB = 60 MHz PCLKC = 60 MHz PCLKD = 120 MHz FCLK = 60 MHz BCLK = 120 MHz
		CoreMark®*4			-	45	-	-	24	-		
		Normal mode*3	All peripheral clocks enabled, code executing from flash		-	75	-	-	38	-		
			All peripheral clocks disabled, code executing from flash *5		-	32	-	-	18	-		
		Sleep mode*4 *5			-	25	150	-	15	75		
		Increase during BGO operation	Data flash P/E		-	7	-	-	7	-		
			Code flash P/E		-	10	-	-	10	-		
	Low-speed mode*4				-	4.4	-	-	3	-		ICLK = 1 MHz
	Subosc-speed mode*4				-	3	-	-	2	-		ICLK = 32.768 kHz
	Software Standby mode				-	2.4	110	-	1.2	55		-
	mode	Power supplied to Standby SRAM and USB resume detecting unit			-	37	255	-	37	255	µA	VBAT ≠ VCC*7
					-	37	285	-	37	285		VBAT = VCC
		Power not supplied to SRAM or USB resume detecting unit	Power-on reset circuit low-power function disabled		-	25	50	-	25	50		VBAT ≠ VCC*7
					-	25	80	-	25	80		VBAT = VCC
			Power-on reset circuit low-power function enabled		-	16	35	-	16	35		VBAT ≠ VCC*7
					-	16	65	-	16	65		VBAT = VCC

Note 5. FCLK, BCLK, PCLKA, PCLKB, PCLKC, and PCLKD are set to be divided by 64 (3.75 MHz).

4. 43.2.4 Data Stop Register (SD_STOP)

• Modified the explanation of the the STP bit.

[Before]

Set STP to 0 after the response end flag sets.

[After]

Set STP to 0 after the access end flag sets.

5. 11.1 Overview

• Modified Note 13 in the table 11.2.

[Before]

Note 13. When using the Programmable Gain Amplifiers, MSTPDn (n = 14,15) must be set to 0.

[After]

Note 13. When using the Programmable Gain Amplifiers, MSTPDn (n = 15,16) must be set to 0.

6. 32.2.36 PHY Cross Point Adjustment Register (PHYSLEW)

[Before]

Bit	Symbol	Bit name	Description	R/W
b0	SLEWR00	Driver Cross Point Adjustment 00	0: Host controller mode 1: Device controller mode.	R/W
b1	SLEWR01	Driver Cross Point Adjustment 01	0: Device controller mode 1: Host controller mode.	R/W
b2	SLEWF00	Driver Cross Point Adjustment 00	0: Setting prohibited 1: Host or device controller mode.	R/W
b3	SLEWF01	Driver Cross Point Adjustment 01	0: Device controller mode 1: Host controller mode.	R/W

[After]

Bit	Symbol	Bit name	Description	R/W
b0	SLEWR00	Driver Cross Point Adjustment 00	0: Reserved 1: Host or device controller mode.	R/W
b1	SLEWR01	Driver Cross Point Adjustment 01	0: Host or device controller mode 1: Reserved.	R/W
b2	SLEWF00	Driver Cross Point Adjustment 00	0: Reserved 1: Host or device controller mode.	R/W
b3	SLEWF01	Driver Cross Point Adjustment 01	0: Host or device controller mode 1: Reserved.	R/W

7. 59.3.11 SPI Timing

• Modified the title of the figure 59.46.

[Before]

Figure 59.46 SPI timing for master when CPHA = 1 and the bit rate is set to PCLKA/2

[After]

Figure 59.46 SPI timing for master when CPHA = 1

8. 23.3.4 Automatic Dead Time Setting Function

[Before]

GPT32EH0 to GPT32EH3 and GPT32E4 to GPT32E7

When GTDVm buffer operation is enabled: GTDVUm can be written at anytime.

When GTDVm buffer operation is disabled: To change GTDVUm to a new value, first stop the GPT using the CST bit in the GTCR register.

GPT328 to GPT3213

While GPT is running, changing the GTDVm values is prohibited. To change GTDVm to a new value, first stop the GPT using the CST bit in the GTCR register.

[After]

GPT32EH0 to GPT32EH3 and GPT32E4 to GPT32E7

When GTDVm buffer operation is enabled: GTDVm can be written at anytime.

When GTDVm buffer operation is disabled: To change GTDVm to a new value, first stop the GPT using the CST bit in the GTCR register.

GPT328 to GPT3213

While GPT is running, changing the GTDVU values is prohibited. To change GTDVU to a new value, first stop the GPT using the CST bit in the GTCR register.

9. 23.10.2 GTCCRn Settings during Compare Match Operation (n = A to F)

[Before]

(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following constraints. If the constraints are not satisfied, correct output waveforms with secured dead time might not be obtained.

• In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR – GTDVD

• In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVD

Similarly, the GTCCRE and GTCCRF registers must be set to satisfy the following constraints. If the constraints are not satisfied, correct output waveforms with secured dead time might not be obtained.

• In up-counting: GTCCRE < GTCCRF, GTCCRE > GTDVU, GTCCRF < GTPR – GTDVD

• In down-counting: GTCCRE > GTCCRF, GTCCRE < GTPR – GTDVU, GTCCRF > GTDVD

[After]

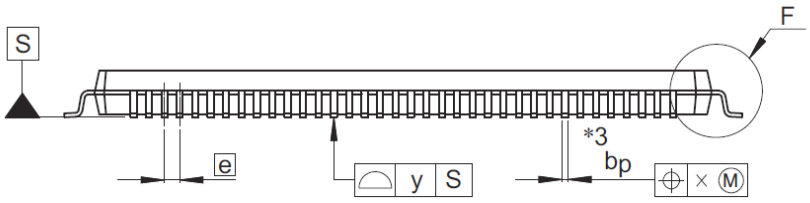
(3) When automatic dead time setting is made in saw-wave one-shot pulse mode

The GTCCRC and GTCCRD registers must be set to satisfy the following constraints. If the constraints are not satisfied, correct output waveforms with secured dead time might not be obtained.

• In up-counting: GTCCRC < GTCCRD, GTCCRC > GTDVU, GTCCRD < GTPR - GTDVD
• In down-counting: GTCCRC > GTCCRD, GTCCRC < GTPR – GTDVU, GTCCRD > GTDVD

10. Appendix 2. Package Dimensions

• Modified figure 2.5, 144-pin LQFP



[Before]

Reference symbol	Dimensions in millimeters		
	Min	Nom	Max
:	:	:	:
y	-	-	0.08
:	:	:	:

[After]

Reference symbol	Dimensions in millimeters		
	Min	Nom	Max
:	:	:	:
y	-	-	0.10
:	:	:	:

11. 20.2.1 Port Control Register 1

[Before]

20.2.1 Port Control Register 1 (PCNTR1)

PDR selects the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on Port m is associated with a PORTm.PDR bit. The I/O direction can be specified in 1-bit units.

[After]

20.2.1 Port Control Register 1 (PCNTR1/PODR/PDR)

Port Control Register 1 is a 32- and 16-bit readable/writable register that controls port direction and port output data. PCNTR1 specifies both the port direction and the output data, in 32-bit units. PDR (PCNTR1 bits [15:0]) and PODR (PCNTR1 bits [31:16]) specify port direction and port output data, respectively, and are accessed in 16-bit units.

PDR selects the input or output direction for individual pins on the associated port when the pins are configured as general I/O pins. Each pin on Port m is associated with a PORTm.PDR bit. The I/O direction can be specified in 1-bit units.

12. 20.2.2 Port Control Register 2

[Before]

20.2.2 Port Control Register 2 (PCNTR2)

PIDR reflects the individual pin states of the port, regardless of the values set in PORTm.PIDR and PORTm.PDR. When PORTm.PMR = 1 or PORTm.PDR = 1, the read data is don't-care.

[After]

20.2.2 Port Control Register 2 (PCNTR2/EIDR/PIDR)

Port Control Register 2 provides read access to the port input data and the port event input data using 32-bit or 16-bit access. PCNTR2 provides access to both the port input data and the port event input data, in 32-bit units. PIDR (PCNTR2 bits [15:0]) and EIDR (PCNTR2 bits [31:16]) provide port input data and port event input data, respectively, and are accessed in 16-bit units.

PIDR reflects the individual pin states of the port, regardless of the values set in PORTm.PMR and PORTm.PDR. When PORTm.PMR = 1 or PORTm.PDR = 1, the read data is don't-care.

13. 20.2.3 Port Control Register 3

[Before]

20.2.3 Port Control Register 3 (PCNTR3)

POSR changes PODR when set by a software write. For example, for P100, when PORT1.POSR00 = 1, PORT1.PODR00 outputs 1. Bits associated with non-existent pins are reserved.

[After]

20.2.3 Port Control Register 3 (PCNTR3/PORR/POSR)

Port Control Register 3 is a 32- and 16-bit writable register that controls setting or resetting of the port output data. PCNTR3 controls both setting or resetting of the port output data, and is set in 32-bit units. POSR (PCNTR3 bits 15:0]) and PORR (PCNTR3 bits [31:16]) control setting and resetting of port output data, respectively, and are accessed in 16-bit units.

POSR changes PODR when set by a software write. For example, for P100, when PORT1.POSR00 = 1, PORT1.PODR00 outputs 1. Bits associated with non-existent pins are reserved.

14. 20.2.4 Port Control Register 4

[Before]

20.2.4 Port Control Register 4 (PCNTR4)

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100, if PORT1.EOSR00 is set to 1 when ELC_PORTx occurs, PORT1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value must always be 0. P200 is input only, so PORT2.PCNTR3 bit [0] is reserved.

[After]

20.2.4 Port Control Register 4 (PCNTR4/EORR/EOSR)

Port Control Register 4 is a 32- and 16-bit readable/writable register that controls setting or resetting of the port output data by event input from the ELC. PCNTR4 controls both setting and resetting of the port output data by event input from the ELC, and is set in 32-bit units. EOSR (PCNTR4 bits [15:0]) and EORR (PCNTR4 bits [31:16]) control setting and resetting of output data by event input from the ELC, respectively, and are accessed in 16-bit units.

EOSR changes PODR when set because an ELC_PORTx signal occurs. For example, for P100, if PORT1.EOSR00 is set to 1 when ELC_PORTx occurs, PORT1.PODR00 outputs 1. Bits associated with non-existent pins are reserved. The write value must always be 0. P200 is input only, so PORT2.PCNTR3 bit [0] is reserved.

15. 20.2.5 Port mn Pin Function Select Register (PmnPFS) (m = 0 to 9, A, B; n = 00 to 15)

[Before]

20.2.5 Port mn Pin Function Select Register (PmnPFS) (m = 0 to 9, A, B; n = 00 to 15)

The PDR, PIDR, and PODR bits serve the same function as PCNTR. When these bits are read, the PCNTR value is read.

[After]

20.2.5 Port mn Pin Function Select Register (PmnPFS/PmnPFS_HA/PmnPFS_BY) (m = 0 to 9, A, B; n = 00 to 15)

Port mn Pin Function Select Register is a 32-, 16-, and 8-bit readable/writable control register that selects the port mn pin functions. PmnPFS is accessed in 32-bit units.

PmnPFS is set by 32-bit units. PmnPFS_HA (PmnPFS bits [15:0]) is accessed in 16-bit units. PmnPFS_BY (PmnPFS bits [7:0]) is accessed in 8-bit units.

The PDR, PIDR, and PODR bits serve the same function as PCNTR. When these bits are read, the PCNTR value is read.

16. 2.10.3 Connecting Sequence and JTAG/SWD Authentication

[Before]

Because the OCD emulator is protected by the JTAG/SWD authentication mechanism, the OCD might be required to input the ID code to the authentication registers. The OSIS value in the option-setting memory determines whether the code is required.

(1) When OSIS is all 1s (default)

OCD authentication is not required and the OCD can use the AHB-AP without authentication.

(omitted)

(2) When OSIS is not all 1s

OCD authentication is required and the OCD must write the unlock code to IAUTH registers 0 to 3 in OCDREG before using the AHB-AP.

[After]

Because the OCD emulator is protected by the JTAG/SWD authentication mechanism, the OCD might be required to input the ID code to the authentication registers. The OSIS value in the option-setting memory determines whether the code is required.

After the negation of reset, a 8.5 µs wait time is required before comparing the OSIS value at the time of cold start.

(1)When MSB of OSIS is 0 (Bit 127 = 0)

The ID code is always non-matching, and connection to the on-chip debugger is prohibited.

(2) When OSIS is all 1s (default)

OCD authentication is not required and the OCD can use the AHB-AP without authentication.

(omitted)

(3) When OSIS is “ALeRASE” in ASCII code

1. The content of the user flash area will be erased at once. See section 54, Flash Memory details.

(4) When OSIS is not all 1s

OCD authentication is required and the OCD must write the unlock code to IAUTH registers 0 to 3 in OCDREG before using the AHB-AP.

17. 52.3.3 DED Error Generation

[Before]

When either the DED2ERR bit in the DED2STS register or the DED1ERR bit in the DED2STS is set to 1, a DED error is generated. The DED error can be specified as a non-maskable interrupt or reset in the DEDOAD register. When the debugger is connected, non-maskable interrupts and resets do not occur.

[After]

When either the DED2ERR bit in the DED2STS register or the DED1ERR bit in the DED2STS is set to 1, a DED error is generated. The DED error can be specified as a non-maskable interrupt or reset in the DEDOAD register.

18. 52.3.5 SRAM Error Sources

[Before]

Table 52.2 SRAM error sources

Interrupt source	DTC activation	DMAC activation
DED error (SRAM0 area with DED)	Not possible	Not possible
Parity error (SRAM0 area without DED, SRAM1, SRAMSH)	Not possible	Not possible

Note: Resets and non-maskable interrupts are not generated when a debugger is connected. Other DED functions are not affected by the debugger.

[After]

Table 52.2 SRAM error sources

Interrupt source	DTC activation	DMAC activation
DED error (SRAM0 area with DED)	Not possible	Not possible
Parity error (SRAM0 area without DED, SRAM1, SRAMSH)	Not possible	Not possible

19. 34.13.6 Constraints on Clock Synchronous Transmission in Clock Synchronous and Simple SPI Modes

[Before]

When the external clock source is used as a synchronization clock, the following constraints apply.

(1) Start of transmission

Update TDR through the CPU, DMAC, or DTC and wait for at least five PCLKA cycles before allowing the transmit clock to be input, see Figure 34.77.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock (bit [7]) (see Figure 34.77).

When updating TDR after bit [7] has started to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock (bit [7]) to four PCLKA cycles or longer (see Figure 34.77).

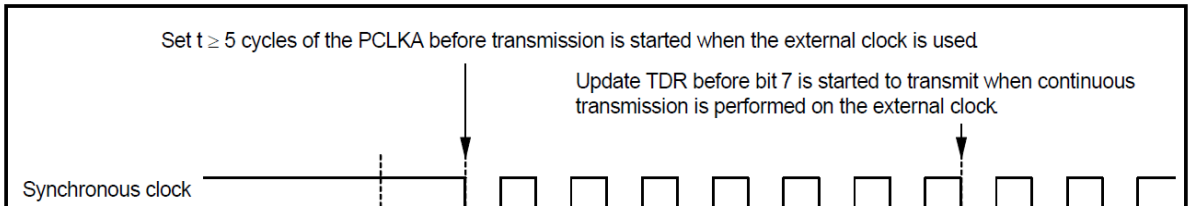


Figure 34.77 Constraints on use of external clock in clock synchronous transmission

[After]

When the external clock source is used as a synchronization clock, the following constraints apply.

(1) Start of transmission

Wait at least the following time from writing transmit data to TDR to the start of the external clock input:

1 PCLK cycle + data output delay time for the slave (t_{DO}) + setup time for the master (t_{SU}). See Figure 34.77.

(2) Continuous transmission

Write the next transmit data to TDR or TDRHL before the falling edge of the transmit clock (bit [7]) (see Figure 34.77).

When updating TDR after bit [7] has started to transmit, update TDR while the synchronization clock is in the low-level period, and set the high-level width of the transmit clock (bit [7]) to four PCLKA cycles or longer (see Figure 34.77).

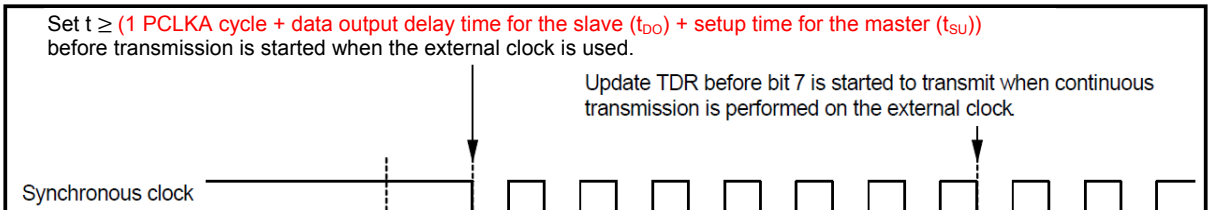


Figure 34.77 Constraints on use of external clock in clock synchronous transmission

20. 41.2.1 Control Register (SSICR)

[Before]

Bit	Symbol	Bit name	Description	R/W
:	:	:	:	:
b9	PDTA	Parallel Data Allocation *3	When data word length is 8 or 16 bits: 0: Transfer lower bits of parallel data (SSIFTDR, SSIFRDR) before upper bits 1: Transfer upper bits of parallel data (SSIFTDR, SSIFRDR) before lower bits. When data word length is 18, 20, 22, or 24 bits: 0: Parallel data (SSIFTDR, SSIFRDR) left-aligned 1: Parallel data (SSIFTDR, SSIFRDR) right-aligned.	R/W

[After]

Bit	Symbol	Bit name	Description	R/W
:	:	:	:	:
b9	PDTA	Parallel Data Allocation *3	When data word length is 8 or 16 bits: 0: Parallel data allocated at the lower bytes/half word (SSIFTDR, SSIFRDR) are transferred prior to the upper bytes/half word 1: Parallel data allocated at the upper bytes/half word (SSIFTDR, SSIFRDR) are transferred prior to the lower bytes/half word. When data word length is 18, 20, 22, or 24 bits: 0: Parallel data (SSIFTDR, SSIFRDR) left-aligned 1: Parallel data (SSIFTDR, SSIFRDR) right-aligned.	R/W

21. 11.10.7 Timing of WFI Instruction

[Before]

It is possible for the WFI instruction to be executed before I/O register writes are complete, in which case operation might not proceed as intended. This can happen if the WFI is placed immediately after a write to an

I/O register. To avoid this problem, read back the register that was written to confirm that the write has completed.

[After]

It is possible for the WFI instruction to be executed before I/O register and CS/SDRAM area writes are complete, in which case operation might not proceed as intended. This can happen if the WFI is placed immediately after a write to an I/O register and CS/SDRAM area. To avoid this problem, read back the register and CS/SDRAM area that was written to confirm that the write completed.

22. 22.2.1 POEG Group n Setting Register (POEGGn) (n = A to D)

• Modify the IOCE bit to rewrite bit name and description, step comparison as follows:

[Before]

Bit	Symbol	Bit name	Description	R/W
b5	IOCE	Enable for GPT or ACMPHS Output-Disable Request	0: Disable output-disable requests from GPT disable request or comparator interrupt 1: Enable output-disable requests from GPT disable request or comparator interrupt.	R/W*2

Note 2. Can be modified only once after a reset.

[After]

Bit	Symbol	Bit name	Description	R/W
b5	IOCE	Enable for GPT Output-Disable Request	0: Disable output-disable requests from GPT disable request 1: Enable output-disable requests from GPT disable request.	R/W*2

Note 2. Can be modified only once after a reset.

23. 34.2.23 IIC Mode Register 3 (SIMR3)

[Before]

SIMR3.IICSTIF bit description

[Clearing conditions]

• On writing 0 to the bit, while always checking to confirm that it is 0.

• On writing 0 to the SIMR1.IICM bit, when operation is not in simple IIC mode.

• On writing 0 to the SCR.TE bit.

[After]

SIMR3.IICSTIF bit description

[Clearing conditions]

• On writing 0 to the bit. After writing 0 to the IICSTIF bit, read the bit to check that it is actually set to 0.

• On writing 0 to the SIMR1.IICM bit when operation is not in simple IIC mode.

• On writing 0 to the SCR.TE bit.

24. 11.8.4 Snooze Operation Example

[Before]

Table 11.10 is max transfer rate of SCI0 in Snooze mode.

Table 11.10 HOCO: ± 2.4% (Ta = -20 to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency					
	LOCO is operating			LOCO is not operating		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			2400		
2						
4						
8						
16	1200					
32	1200					
64				1200		

[After]

Table 11.10 is max transfer rate of SCI0 in Snooze mode.

Table 11.10 HOCO: ± 2.4% (Ta = -20 to 105°C) (Unit: bps)

Maximum division ratio of ICLK, PCLKA, PCLKB, PCLKC, PCLKD, FCLK, BCLK, and TRCLK	HOCO frequency					
	LOCO is operating			LOCO is not operating		
	16 MHz	18 MHz	20 MHz	16 MHz	18 MHz	20 MHz
1	2400			600		
2						
4						
8	1200					
16						
32						
64						

Note: When SCI0 is used in Snooze mode, the following setting must be used: BGDM = 0, ABCS = 0, ABCSE = 0.
See section 34, Serial Communications Interface (SCI) for details.

25. 34.3.8 Serial Data Transmission in Asynchronous Mode

[Before]

(2) FIFO selected

1. The SCI transfers data from FTDRL*1 to TSR when data is written to FTDRL*1 in the SCIn_TXI interrupt handling routine. It can write transmit data bytes stored in the 16-FTDRL register. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE and the TIE bits in the SCR are set to 1 simultaneously by a single instruction.

(omitted)

6. If data is not set in FTDRL*3, the TEND flag in SSR_FIFO is set to 1, the stop bit is sent, and the mark state is entered in which 1 is output. If the TEIE bit in SCR is 1 at this time, the TEND flag in SSR_FIFO is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Write data not to FTDRH and FTDRL but to the FTDRH and FTDRL registers when 9-bit data length is selected.

[After]

(2) FIFO selected

1. The SCI transfers data from FTDRL[*1] to TSR when data is written to FTDRL[*1] in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE and TIE bits in the SCR are set to 1 simultaneously by a single instruction.

(omitted)

6. If data is not set in FTDRL[*3], the TEND flag in SSR_FIFO is set to 1, the stop bit is sent, and the mark state is entered in which 1 is output. If the TEIE bit in SCR is 1 at this time, the TEND flag in SSR_FIFO is set to 1 and an SCIn_TEI interrupt request is generated.

Note 1. Write data to the FTDRH and FTDRL registers when 9-bit data length is selected.

26. 34.5.4 Serial Data Transmission in Clock Synchronous Mode

[Before]

(2) FIFO selected

1. The SCI transfers data from FTDRL[*1] to TSR when data is written to FTDRL[*1] in the SCIn_TXI interrupt handling routine. It can write non-transmit data that is stored in the 16-bit FTDRL register. The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit in SCR is set to 1 but only after the TIE bit in SCR is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.

[After]

(2) FIFO selected

1. The SCI transfers data from FTDRL[*1] to TSR when data is written to FTDRL[*1] in the SCIn_TXI interrupt handling routine. The amount of data that can be written to FTDRL is 16 minus FDR.T[4:0] bytes .The SCIn_TXI interrupt request at the beginning of transmission is generated when the TE bit in SCR is set to 1 but only after the TIE bit in SCR is also set to 1 or when these two bits are set to 1 simultaneously by a single instruction.

27. 34.5.6 Simultaneous Serial Data Transmission and Reception in Clock Synchronous Mode

[Before]

(2) FIFO selected

Figure 34.44 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode at FIFO selected.

(omitted)

To switch from receive mode to simultaneous transmit and receive mode, check that the SCI completes the reception. Set the RIE and RE bits to 0. Check that the receive error flags ORER, FER, and PER in SSR_FIFO are 0, and then set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously by a single instruction.

[After]

(2) FIFO selected

Figure 34.44 shows an example flow of simultaneous serial transmit and receive operations in clock synchronous mode at FIFO selected.

(omitted)

To switch from receive mode to simultaneous transmit and receive mode:

1. Check that the SCI completes the reception.
2. Set the RIE and RE bits to 0.
3. Check that the receive error flag ORER in SSR_FIFO is 0, then set the TIE, RIE, TE, and RE bits in SCR to 1 simultaneously by a single instruction.