Date: May 12, 2016

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A002A/E	Rev.	1.00
Title	Restriction and revised information of S7 Series from the previous Rev.0.85		Information Category	Technical Notification		
Applicable Product	Synergy S7 Series S7G2	Lot No. All lots	Reference Document	S7G2 User's Manual: Microcontrollers, Rev.1.00		

1. Restriction about the frequency of PCLKA and PCLKD for the EIDR bit

• Modified section 20.2.2, Port Control Register 2 (PCNTR2).

[Before]

No description

[After]

Note 2: When using GPT, ETHERC, SCI, or SPI as an event trigger, set peripheral operating frequency under the following conditions:

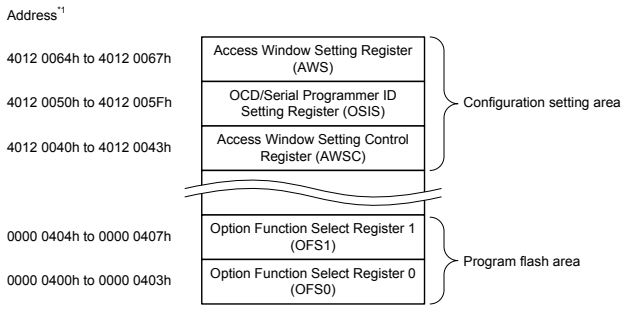
When using GPT, PCLKD ≤ 60 MHz.

When using ETHERC, SCI, or SPI, PCLKA ≤ 60 MHz.

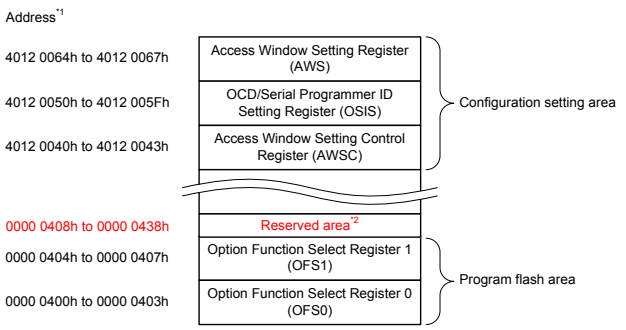
2. Restriction when using option-setting memory area

• Updated Figure 7.1, Option-setting memory area, and added Note 2 in this figure.

[Before]



[After]



Note 1. The option-setting memory must be allocated to the flash user area.
Note 2. Do not access reserved area.

3. Restriction about the oscillation stop detection function

• Modified Table 9.1, Specifications of the Clock Generation Circuit for the clock sources.

[Before]

No description

[After]

Note 1. Selectable from 10 to 20 when oscillation stop detection function is enabled and input frequency less than 12 MHz is used.

Note 2. Except the condition in note 1, oscillation stop detection function is available by CAC.

• Modified section 9.2.4, PLL Clock Control Register (PLLCCR).

[Before]

No description

[After]

Note 3. PLLMUL[5:0] should be set up to 20 when oscillation stop detection function is enabled and input frequency less than 12 MHz is used.

The example of setting for PLL

Input frequency [MHz]	PLLMUL[5:0]	Multiplication ratio	PLL output[MHz]
12MHz	B'010011	10	120
12MHz	B'100110	20	240

4. Restriction about ELCON bit setting timing

• Modified section 19.4.3, Settings for the Module-Stop Function.

[Before]

ELC operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For more information, see Table 19.3 and section 11, Low-Power Modes.

[After]

ELC operation can be disabled or enabled using Module Stop Control Register C (MSTPCRC). The ELC is initially stopped after reset. Releasing the module-stop state enables access to the registers. For more information, see Table 19.3 and section 11, Low-Power Modes. The ELCON bit must be set to 0 before ELC operation is disabled using the MSTPCRC register.

Information: Event Link Controller Register (ELCR)

Bit	Symbol	Bit name	Description	R/W
b7	ELCON	All Event Link Enable	0: Disable ELC function 1: Enable ELC function.	R/W

5. Restriction about PLL clock source using UCLK

• Modified section 9.2.4, PLL Clock Control Register (PLLCCR).

[Before]

No description

[After]

Note 4: PLSRCSEL must be set to 0 when using UCLK.

Information: PLL Clock Control Resister (PLLCR)

Bit	Symbol	Bit name	Description	R/W
b4	PLSRCSEL	PLL Clock Source Select	0: Main clock oscillator*4 1: HOCO.	R/W

Note 4. PLSRCSEL must be set to 0 when using UCLK.

• Modified section 9.7.6, USB Clock (UCLK).

[Before]

The USB clock, UCLK, is the operating clock for the USBFS module. A 48-MHz clock must be supplied to the USBFS module. When the module is used, the UCLK clock must be specified as 48 MHz. Specify the frequency in the following bits:

• UCK[2:0] bits in SCKDIVCR2

• CKSEL[2:0] bits in SCKSCR

• PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR

• HOCOFRQ[1:0] bits in OFS1

[After]

The USB clock, UCLK, is the operating clock for the USBFS module. A 48-MHz clock must be supplied to the USBFS module. When the module is used, the UCLK clock must be specified as 48 MHz. Specify the frequency in the following bits:

• UCK[2:0] bits in SCKDIVCR2

• CKSEL[2:0] bits in SCKSCR

• PLLMUL[5:0] and PLIDIV[1:0] bits in PLLCCR

6. Restriction when VBAT equals to VCC

• Modified section 12.1.4, Tamper Pin Detection.

[Deleted the following sentence]

Note: When the battery backup function is not used, the VBATT pin must be connected to the VCC pin.

• Modified section 12.4, Usage Notes.

[Deleted the following sentence]

1. When the VBATT pin is not used, you must connect it to the VCC pin.

• Modified Table 20.3, Handling of unused pins in section 20.4, Handling of Unused Pin.

[Added the VBATT row to Table 20.3]

Pin name	Description
VBATT	Connect to VCC or VSS. Power consumption from the point of view of it is recommended to connect to the VSS.*4

Note 4. For details on electrical characteristics, see section 59, Electrical Characteristics.

• Updated Table 59.7, Operating and standby current.

[Before]

Table 59.7 Operating and standby current

Item				Symbol	LDO mode			DCDC mode			Unit	Test condition
					Min	Typ	Max	Min	Typ	Max		
Supply current	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit		Icc	-	37	255	-	37	255	μA	
		Power not supplied to SRAM and USB resume detecting unit	Power-on reset circuit low-power function disabled		-	25	50	-	25	50		
			Power-on reset circuit low-power function enabled		-	16	35	-	16	35		

[After]

Table 59.7 Operating and standby current

Item				Symbol	LDO mode			DCDC mode			Unit	Test condition
					Min	Typ	Max	Min	Typ	Max		
Supply current	Deep Software Standby mode	Power supplied to Standby SRAM and USB resume detecting unit		Icc	-	37	255	-	37	255	μA	VBAT ≠VCC*7
					-	37	285	-	37	285		VBAT = VCC
		Power not supplied to SRAM and USB resume detecting unit	Power-on reset circuit low-power function disabled		-	25	50	-	25	50		VBAT ≠VCC*7
					-	25	80	-	25	80		VBAT = VCC
			Power-on reset circuit low-power function enabled		-	16	35	-	16	35		VBAT ≠VCC*7
					-	16	65	-	16	65		VBAT = VCC

Note 7. When VCC is < VDETBATT and > (VBATT + 0.6 V), the injected current connects from the VCC to the VBATT pin through an internal diode.

7. Restriction about module-stop for 12-Bit A/D Converter (ADC12)

• Added an additional section in section 11, Low-Power Modes.

11.10.16 Module-Stop Function for ADC12

When entering Software Standby mode, it is recommended to set ADC12 module-stop (MSTPD15 or MSTPD16 bit) state to reduce power consumption. In this case, the ADC12 can be available in Snooze mode with releasing the ADC12 module-stop using the DTC. Similarly, set module-stop using the DTC before returning to the Software Standby mode from the Snooze mode.

In addition, when using the analog voltage input source (IVCMP2 or IVCMP3) of ACMPHS in the Software Standby mode, do not set the ADC12 module-stop.

8. Restriction about PLL reference clock by HOCO

• Updated notes in Table 9.2, Specifications of the Clock Generation Circuit for the internal clocks.

[Before]

Note: If PLL reference clock source is HOCO, PLL multiplication setting must be set to120 to 240 MHz in consideration of HOCO frequency (min/max).

[After]

Note: Clocks have a permissible frequency range (See Table 9.2).

Flash memory and SRAM also have a permissible operating frequency range in each wait cycle setting. (See section 52, SRAM, section 54, Flash Memory)

Those clock frequency ranges must be satisfied even if the HOCO has its maximum or minimum frequency. (See section 59, Electrical Characteristics).

Information: The example of setting for PLL

HOCOFRQ[1:0]	FLL	HOCO Max frequency [MHz]	PLLMUL[5:0]	Multiplication ratio	PLL output frequency [MHz]
B'00 :16MHz	OFF	16.39	B'011100	14.5	237.7
B'01: 18MHz	OFF	18.44	B'011001	13	239.7
B'10: 20MHz	OFF	20.48	B'010110	11.5	235.5

9. Restriction about insertion of recovery cycles for Buses

• Added section 15.5.3, Insertion of Recovery Cycles.

[Before]

No description

[After]

15.5.3 Insertion of Recovery Cycles

10. Restriction about SDRAMC setting procedure when bus width is 8 bits

• Added Note 1 in Figure 15.43, SDRAMC setting procedure.

[Before]

No description

[After]

Note 1. When the SDRAM bus width is 8 bits, set the SDCCR.BSIZE [1:0] bits to 10b before setting the SDICR register.

11. Restriction about FSPR bit in AWSC

• Updated FSPR bit in section 7.2.3, Access Window Setting Control Register (AWSC).

[Before]

Bit	Symbol	Bit name	Description	R/W
b28	FSPR	Protection of Access Window and Startup Area Select Function	This bit controls programming of the program/erase protection for the access window, the Startup Area Select flag (AWS.BTFLG), and the temporary boot swap. 0: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the startup area select flag (AWS.BTFLG) is invalid. Executing the configuration clear command is invalid. Writing to the startup area select bits (SAS[1:0]) in the FSUAC register is invalid. 1: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the Startup Area Select flag (AWS.BTFLG) is valid. Executing the configuration clear command is valid. Writing to the Startup Area Select bits (SAS[1:0]) in the FSUAC register is valid.	R

[After]

Bit	Symbol	Bit name	Description	R/W
b28	FSPR	Protection of Access Window and Startup Area Select Function	This bit controls programming of the program/erase protection for the access window, the Startup Area Select flag (AWS.BTFLG), and the temporary boot swap. Once this bit is set to 0, it cannot be changed to 1. 0: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the startup area select flag (AWS.BTFLG) is invalid. Writing to the startup area select bits (SAS[1:0]) in the FSUAC register is invalid. 1: Executing the configuration setting command for programming the access window (FAWE[10:0], FAWS[10:0]) and the Startup Area Select flag (AWS.BTFLG) is valid. Writing to the Startup Area Select bits (SAS[1:0]) in the FSUAC register is valid.	R

12. Additional information for I/O buffer Specification

• Modified section 20.5.5, I/O Buffer Specification.

[Before]

20.5.5 I/O Buffer Specification

The P402, P403, and P404 pins can be used as the RTC input pins RTCICn, where n = 0 to 2. When these input pins are enabled in the VBTICTLR register, the output function of these pins is forced to disable. Therefore, the VBTICTLR register must be set to 0 to use the port function.

Note: The VBTICTLR register is not initialized on reset. For more information, see section 11, Low Power Mode.

[After]

20.5.5 I/O Buffer Specification

The P402, P403, and P404 can be used as the RTC input, AGT input and other peripheral functions.

Table 20.4 lists the P402, P403, P404 specifications.

<<Table 20.4 P402, P403, P404 specifications>>

These RTC and AGT inputs are controlled by the VBTICTLR register. And this register is the highest priority which selecting the functions. See Figure 20.5.

In addition, the VBTICTLR register is not initialized on reset. Therefore, when not using the RTC or AGT inputs, the corresponding bit of VBTICTLR register must be set to 0 after reset.

For more information on the VBTICTLR register, see section 12.2.2, VBATT Input Control Register (VBTICTLR).

• Added a paragraph after Table 25.2, AGT I/O pins in section 25.1, Overview.

[Before]

No description

[After]

AGTIO can be controlled by the VBTICTLR register. For more information, see section 12.2.2, VBATT Input Control Register (VBTICTLR) and section 20.5.5, I/O Buffer Specification.

13. Updated the electrical characteristics of SPI

• Data input hold time in Table 59.25, SPI timing was updated as follows:

[Before]

Item			Symbol	Min	Max	Unit	Test condition
SPI	Data input hold time	Master	t_{HF}	0	-	ns	-
		Slave	t_H	20	-		

[After]

Item			Symbol	Min	Max	Unit	Test condition
SPI	Data input hold time	Master	t_{HF} *4	0	-	ns	-
			t_H	t_{Pcyc}	-		
		Slave	t_H	20	-		

Note 4. PCLKA division ratio set to 1/2

• Figure 59.45, SPI timing for master when CPHA = 0 and the bit rate is set to PCLKA/2 was updated as follows:

[Before] t_H

[After] t_{HF}

14. Other revised items (from Rev.0.85 to Rev.1.00)

• Revised items are shown in the table below. See Rev.1.0 of the User Manual for detail.

Chapter	Points in Rev.1.0
1. Overview	Updated VREFH and VREFL descriptions in Table 1.16, Pin functions
2. CPU	Updated the component name for address E00F F000h and E00F F004h in Table 2.7, ROM entries in the CoreSight ROM table
7. Option-Setting Memory	Updated the Note in section 7.2.2, Option Function Select Register 1 (OFS1)
9. Clock Generation Circuit	Added section 9.2.13, FLL Control Register 1 (FLLCR1)
	Added section 9.2.14, FLL Control Register 2 (FLLCR2)
	Added a second note in section 9.2.26, HOCO User Trimming Control Register (HOCOUTCR)
11. Low-Power Modes	Added Note 19. to Table 11.2, Operating Conditions of Each Power Consumption Mode Added Note
	Added section 11.10.13, Conditions of CTSU in Snooze Mode
	Updated section 11.10.14, ELC Events in Snooze Mode
	Added Note 3. to Table 11.3, Interrupt sources for canceling Snooze, Software Standby, and Deep Software Standby modes
	Updated description in section 11.2.9, Snooze End Control Register (SNZEDCR)
12. Battery Backup Function	Updated Note 4. in section 12.4, Usage Notes
13. Register Write Protection	Added HOCOWTCR, FLLCR1, and FLLCR2 to Table 13.1, Association between PRCR bits and registers to be protected
14. Interrupt Controller Unit (ICU)	Updated Table 14.4, Event table
15. Buses	Updated section 15.3.6, CSn Wait Control Register 2 (CSnWCR2) (n = 0 to 7)
	Updated section 15.6.7, Self-Refresh
	Updated Figure 15.37, Example timing for self-refresh cycle in Deep Software Standby mode
	Updated Table 15.3, External bus specifications
	Updated MXC[1:0] description in section 15.3.15, SDRAM Address Register (SDADR)
	Updated Table 15.18, Address multiplexing
	Updated Table 15.4, External bus I/O pins
18. Data Transfer Controller (DTC)	Updated address range in section 18.2.8, DTC Vector Base Register (DTCVBR)

Chapter	Points in Rev.1.0
20. I/O Ports	Updated Table 20.2, I/O port functions
	Updated R/W permission for b5 to b0 in section 20.2.6, Write-Protect Register (PWPR)
	Updated section 20.5.4, Notes on Using Analog Functions
	Added section 20.7, Notes on the PmnPFS Register Setting
	Updated Table 20.10, Register settings for I/O pin functions on Port 2
	Updated Table 20.13, Register settings for I/O pin functions on Port 4
	Updated Table 20.15, Register settings for I/O pin functions on Port 5
21. Key Interrupt Function (KINT)	Updated section 21.4, Usage Notes
26. Realtime Clock (RTC)	Updated section 26.2.20, Frequency Register (RFRH/RFRL)
27. Watchdog Timer (WDT)	Updated UNDFF and REFEF descriptions in section 27.2.3, WDT Status Register (WDTSR)
28. Independent Watchdog Timer (IWDT)	Updated UNDFF and REFEF descriptions in section 28.2.2, IWDT Status Register (IWDTSR)
32. USB 2.0 Full-Speed Module (USBFS)	Added 8-bit access to section 32.2.4, CFIFO Port Register (CFIFO/CFIFOL), D0FIFO Port Register (D0FIFO/D0FIFOL), and D1FIFO Port Register (D1FIFO/D1FIFOL)
33. USB 2.0 High-Speed Module (USBHS)	Added 16-bit access to section 33.2.7, CFIFO Port Register (CFIFO), D0FIFO Port Register (D0FIFO), and D1FIFO Port Register (D1FIFO)
34. Serial Communication Interface (SCI)	Updated the initial value and access permission for bit [1] in section 34.2.14, Serial Status Register for Non-Smart Card Interface and FIFO Mode (SSR_FIFO) (SCMR.SMIF = 0 and FCR.FM = 1)
	Updated the initial value and access permission for bit [6] in section 34.2.31, Serial Port Register (SPTR)
37. Controller Area Network (CAN) Module	Updated Note 1. in section 37.2.2, Bit Configuration Register (BCR)
40. Cyclic Redundancy Check (CRC) Calculator	Updated description for CRCSA[13:0] in section 40.2.5, Snoop Address Register (CRCSAR)
46. 12-Bit A/D Converter (ADC12)	Updated Table 46.1, ADC12 specifications
	Updated Table 46.14, List of ACMPHS pins that cannot be selected during A/D conversion
50. Capacitive Touch Sensing Unit (CTSU)	Updated bit [15] CTSUICOMP in section 50.2.20, CTSU Error Status Register (CTSUERRS)
	Updated section 50.4.5, TSCAP Pin
59. Electrical Characteristics	Added section 59.16, Joint European Test Action Group (JTAG)
	Added section 59.17, Serial Wire Debug (SWD)
	Added section 59.18, Embedded Trace Macro Interface (ETM)
	Updated Table 59.13, Clock timing except for sub-clock oscillator
	Updated Table 59.40, A/D conversion characteristics for unit 0
	Updated Table 59.41, A/D conversion characteristics for unit 1
	Updated Table 59.5, I/O I_{OH}, I_{OL}
All	Modified pin name as follows: - Deleted # from pin names - CTSn and RTSn became CTSn_RTSn