Introduction

This application note describes the operation of a sample embedded firmware project to demonstrate the transmission and reception of high-speed serial data, greater than 3Mb/s, using the on-board serial peripheral interface (SPI) module and DMA. The sample is designed to be operated on two RSK+RZA1H development boards.

Target Device

RZ/A1H

When applying the sample program covered in this application note to another microcontroller, modify the program according to the specifications for the target microcontroller and conduct an extensive evaluation of the modified program.

The following documents in Table 1-1 apply to the RSK+RZA1H Group. Make sure to refer to the latest versions of these documents. The newest versions of the documents listed may be obtained from the Renesas Electronics Web site.

<table>
<thead>
<tr>
<th>Document Type</th>
<th>Description</th>
<th>Document Title</th>
<th>Document No.</th>
</tr>
</thead>
<tbody>
<tr>
<td>User’s Manual</td>
<td>Describes the technical details of the RSK hardware.</td>
<td>RSK+RZA1H User’s Manual</td>
<td>R20UT3007EG</td>
</tr>
<tr>
<td>Quick Start Guide</td>
<td>Provides simple instructions to setup the RSK and run the first sample, on a single A4 sheet.</td>
<td>RSK+RZA1H Quick Start Guide</td>
<td>R20UT3006EG</td>
</tr>
<tr>
<td>Schematics</td>
<td>Full detail circuit schematics of the RSK.</td>
<td>RSK+RZA1H Schematics</td>
<td>R20UT2586EG</td>
</tr>
<tr>
<td>Hardware Manual</td>
<td>Provides technical details of the RSK+RZA1H microcontroller.</td>
<td>RSK+RZA1H Group User’s Manual: Hardware</td>
<td>R01UH0403EJ</td>
</tr>
</tbody>
</table>

Table 1-1 Relevant Documents
1. **List of Abbreviations**

List of abbreviations used in this document is available in Table 1-1.

<table>
<thead>
<tr>
<th>Abbreviation</th>
<th>Full Form</th>
</tr>
</thead>
<tbody>
<tr>
<td>CPU</td>
<td>Central processing unit</td>
</tr>
<tr>
<td>CRC</td>
<td>Cyclic redundancy check</td>
</tr>
<tr>
<td>DACK</td>
<td>Transfer request acknowledge signal</td>
</tr>
<tr>
<td>DMAC</td>
<td>Direct memory access controller</td>
</tr>
<tr>
<td>DMAC3</td>
<td>Direct memory access controller channel 3</td>
</tr>
<tr>
<td>DMAC5</td>
<td>Direct memory access controller channel 5</td>
</tr>
<tr>
<td>GND</td>
<td>Ground reference</td>
</tr>
<tr>
<td>IIC</td>
<td>Inter-integrated circuit</td>
</tr>
<tr>
<td>IRQ</td>
<td>Interrupt request</td>
</tr>
<tr>
<td>MISO</td>
<td>Master in slave out</td>
</tr>
<tr>
<td>MOSI</td>
<td>Master out slave in</td>
</tr>
<tr>
<td>NOR</td>
<td>NOR flash memory</td>
</tr>
<tr>
<td>OSTM</td>
<td>Operating system timer</td>
</tr>
<tr>
<td>RAM</td>
<td>Random access memory</td>
</tr>
<tr>
<td>RSK</td>
<td>Renesas starter kit</td>
</tr>
<tr>
<td>RSPCK</td>
<td>RSPI clock</td>
</tr>
<tr>
<td>RSPIC</td>
<td>Renesas serial peripheral interface</td>
</tr>
<tr>
<td>RSPI RX</td>
<td>RSPI receive buffer</td>
</tr>
<tr>
<td>RSPI TX</td>
<td>RSPI transfer buffer</td>
</tr>
<tr>
<td>RSPI1</td>
<td>Renesas serial peripheral interface channel 1</td>
</tr>
<tr>
<td>RSPI4</td>
<td>Renesas serial peripheral interface channel 4</td>
</tr>
<tr>
<td>SSL</td>
<td>Slave select</td>
</tr>
</tbody>
</table>

*Table 1-1 List of Abbreviations*
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2. Specifications

The DMAC can be used in place of the CPU to perform high-speed transfers between external devices that have DACK, external memory, on-chip memory, memory-mapped external devices, and on-chip peripheral modules.

This application note explains how to use the RZ/A1H DMA controller for transmission and reception of data via the RSPI module. The sample application uses a DMAC channel to transmit ASCII data from on-chip RAM memory to the transfer buffer of RSPI. This data is sent through MISO or MOSI pin depending on whether the RSK is configured as a master or a slave device. A different DMA channel is used to load the received data into RAM. The movement of data between RSPI and on-chip RAM is carried out using only DMAC without any CPU intervention.

<table>
<thead>
<tr>
<th>Peripheral Function</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>DMAC5</td>
<td>DMAC5 will be configured to transfer data from RSPI4 RX to RAM.</td>
</tr>
<tr>
<td>DMAC3</td>
<td>DMAC3 will be configured to transfer data from RAM to RSPI4 TX.</td>
</tr>
<tr>
<td>RSPI4</td>
<td>Used for serial transmission.</td>
</tr>
<tr>
<td>RSPI1</td>
<td>Used for communication with the PMOD LCD screen.</td>
</tr>
<tr>
<td>OSTM</td>
<td>Used to create a timer to measure the transfer rate</td>
</tr>
</tbody>
</table>

Table 2-1 Peripheral Function to be Used and Their Uses

![Figure 2-1 Outline of Operation for Two Devices](image)

The arrows in Figure 2-1 indicate the direction of data flow.
3. Operating Check Conditions
The sample code described in this application note has been checked under the conditions listed in Table 3-1.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller used</td>
<td>RZA1H (R7S721001)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>- Maximum operating frequency : 400MHz</td>
</tr>
<tr>
<td></td>
<td>- Image processing clock : 266.67MHz</td>
</tr>
<tr>
<td></td>
<td>- Internal bus clock : 133.33MHz</td>
</tr>
<tr>
<td></td>
<td>- Peripheral clock1 : 66.67MHz</td>
</tr>
<tr>
<td></td>
<td>- Peripheral clock0 : 33.33MHz</td>
</tr>
<tr>
<td>RSK Operating voltage</td>
<td>5.0V</td>
</tr>
<tr>
<td>Integrated development environment</td>
<td>e*studio version 4.0.1.007</td>
</tr>
<tr>
<td>C Compilers</td>
<td>KPIT GNUARM-NONE_EABI Toolchain v14.02</td>
</tr>
<tr>
<td>Board used</td>
<td>RSK+RZ/A1H board</td>
</tr>
</tbody>
</table>

Table 3-1 Operating Check Conditions
4. Description of Hardware

The sample is intended to be run on the RSK+RZA1H. For more information on the RSK+RZA1H hardware please refer to the User’s Manual (R20UT3007EG) and the RSK+RZA1H schematics (R20UT2586EG).

4.1 List of Pins to be used

Table 4-1 lists the pins to be used and their functions.

<table>
<thead>
<tr>
<th>Port Name</th>
<th>Signal Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P2_8</td>
<td>P2_8_RSPCK4</td>
<td>Input/output</td>
<td>Used for RSPI4 clock input or output</td>
</tr>
<tr>
<td>P2_9</td>
<td>P2_9_SSL40</td>
<td>Input/output</td>
<td>Used for RSPI4 slave select</td>
</tr>
<tr>
<td>P2_10</td>
<td>P2_10_MOSI4</td>
<td>Input/output</td>
<td>Used for RSPI4 MOSI</td>
</tr>
<tr>
<td>P2_11</td>
<td>P2_8_MISO4</td>
<td>Input/output</td>
<td>Used for RSPI4 MISO</td>
</tr>
<tr>
<td>P11_12</td>
<td>P11_12_RSPCK1</td>
<td>Output</td>
<td>Used for PMOD CLK line</td>
</tr>
<tr>
<td>P4_15</td>
<td>PMOD_RST</td>
<td>Output</td>
<td>Used for PMOD command line</td>
</tr>
<tr>
<td>P3_7</td>
<td>PMOD_PIN10</td>
<td>Output</td>
<td>Used to for PMOD Command line</td>
</tr>
<tr>
<td>P1_9</td>
<td>IRQ3</td>
<td>Input</td>
<td>SW1. Connects to an IRQ input for user controls</td>
</tr>
<tr>
<td>P1_8</td>
<td>IRQ2</td>
<td>Input</td>
<td>SW2. Connects to an IRQ input for user controls</td>
</tr>
<tr>
<td>P1_11</td>
<td>IRQ5</td>
<td>Input</td>
<td>SW3. Connects to an IRQ input for user controls</td>
</tr>
</tbody>
</table>

Table 4-1 Pins to be Used and their Functions
4.2 Configuration

Please make sure that both used boards have the following settings.

4.2.1 Switches

Ensure that SW4 has the settings shown in Table 4-2.

<table>
<thead>
<tr>
<th>SW4</th>
<th>SW4-1</th>
<th>SW4-2</th>
<th>SW4-3</th>
<th>SW4-4</th>
<th>SW4-5</th>
<th>SW4-6</th>
<th>SW4-7</th>
<th>SW4-8</th>
</tr>
</thead>
<tbody>
<tr>
<td>State</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
<td>OFF</td>
</tr>
</tbody>
</table>

Table 4-2 SW4 Settings

Ensure that SW6 has the settings shown in Table 4-3.

<table>
<thead>
<tr>
<th>SW6</th>
<th>SW6-1</th>
<th>SW6-2</th>
<th>SW6-3</th>
<th>SW6-4</th>
<th>SW6-5</th>
<th>SW6-6</th>
</tr>
</thead>
<tbody>
<tr>
<td>State</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

Table 4-3 SW6 Settings

4.2.2 Jumpers

All Jumpers shall not be fitted with the following exceptions:

- JP11 1-2 connected
- JP12 1-2 connected
- JP21 1-2 connected
- JP18 1-2 connected
4.2.3 Resistor Modifications
No resistor modification from the default RSK state is required for this sample code.

4.2.4 Connections
For transmission and reception to take place over two boards, the connections outlined in Table 4-4 are required.

<table>
<thead>
<tr>
<th>RSK 1</th>
<th>RSK 2</th>
<th>Function</th>
</tr>
</thead>
<tbody>
<tr>
<td>CN15_1</td>
<td>CN15_1</td>
<td>MISO to MISO</td>
</tr>
<tr>
<td>CN15_3</td>
<td>CN15_3</td>
<td>MOSI to MOSI</td>
</tr>
<tr>
<td>CN15_5</td>
<td>CN15_5</td>
<td>RSPCK to RSPCK</td>
</tr>
<tr>
<td>CN15_7</td>
<td>CN15_7</td>
<td>SSL to SSL</td>
</tr>
<tr>
<td>GND</td>
<td>GND</td>
<td>GND to GND</td>
</tr>
</tbody>
</table>

Table 4-4 Board to Board Connection

4.2.5 Caution
When carrying out transmission and reception between two boards, please make sure that there is a connection between the grounds of the two boards. I.e. any GND on board 1 to any GND on board 2. Not connecting the two grounds could result in track and/or component damage.
5. Description of Software

The sample application covered in this application note uses the DMAC to move the data between RSPI data buffer and the on-board RAM. DMAC3 is used to move data from the on-chip RAM to RSPI data buffer while DMAC5 is used to move data from RSPI data buffer to the on-chip RAM. If data is written to RSPI data buffer, it automatically gets transferred to the RSPI TX. However, if the RSPI data buffer is read, data is automatically fetched from the RSPI RX. The progress/outcome of the transmission and reception is displayed on PMOD.

5.1 Operation Outline

The operation outline of the sample code is described below in sections (a) to (f).

(a) Display introduction message

![Figure 5-1 Introduction Message](image)

(b) Switch press

- Wait for either SW2 or SW3 press.

(c) Display chosen mode and initialise RSPI4 accordingly

- If SW2 was pressed initialise, RSPI4 in master mode. The display should resemble **Figure 5-2**.

![Figure 5-2 Display after SW2 Press](image)
- IF SW3 was pressed, initialise RSPI4 in slave mode. The display should look like Figure 5-3.

![Figure 5-3 Display after SW3 Press](image)

(d) Wait for SW1 to be pressed on the master RSK.

(e) Enable transmission

- Take first time stamp. Wait for DMA channel three to complete. The PMOD should look like Figure 5-4.

![Figure 5-4 Display During Transfer](image)

(f) Display transmission rate and check received data integrity

- Take another time stamp and calculate data rate. On transfer completion PMOD should look like Figure 5-5.

![Figure 5-5 Display After Transmission and Reception](image)
5.2 Data Integrity

This sample code uses an extremely efficient and fast implementation of CRC16 algorithm as a means of error checking. The data that is sent from one RSK to another has a CRC value appended to it. The receiving board will calculate the CRC value of the received data and compare the result to the appended CRC. If the CRC values do not match, the PMOD display will resemble to Figure 5-6.

To alter the amount of data to be transferred the user can configure a macro (DATA_SIZE), which is found in ‘configuration.h’. The CRC value will be calculated for the new data size. However, if DATA_SIZE is to be set to more than 100000, please make sure to update the size and add appropriate number of bytes to the array ‘g_dmac_src_data_internalram’ found in ‘data.c’.

Figure 5-6 Corrupted Data
5.3 Flow Charts

Figure 5-7 shows the overall flow of the sample program described in this application note.

![Flow Chart Diagram]

Initialise hardware - hdwinit().
Calculate CRC value - calc_crc().
Register a function to be called on switch press – set_switch_press_callback().
Display instructions – display_instruction().
Start OS timer – R_OSTM_Open().

Figure 5-7 Overall Flow
5.3.1 Peripheral Initialisation

Figure 5-8 shows the hdwinit() function flow.

Figure 5-8 Initialisation Function

hdwinit()

Initialises IIC interface
R_RIIC_rza1h_rsk_init()

Initialises LED Peripheral
R_LED_init()

Initialises SPI1 interface
R_SPI_init()

Initialises switches peripheral
switches_init()

Initialises LCD Peripheral
R_LCD_Init()

Initialises OSTM Peripheral
R_OSTM_Init()

Configure DMAC5 to receive data
dmac_receive_spi4rx()

Configure DMAC3 to send data
dmac_send_spi4tx()

End

Please see section 5.3.2

Please see section 5.3.2
5.3.2 DMA Configuration

Figure 5-9 shows the DMA configuration.

- `dma_send_spi4tx()` / `dma_receive_spi4rx()`
- Disable existing transfers and clear interrupt and interrupt flag.
- Set up DMA transfer mode settings
- Configure source address, destination address, and transfer size
- Interrupt settings
- End

Set source transfer size.
Set destination transfer size.
Source address to be fixed/incremented.
Destination address to be fixed/incremented.
Set channel status to register mode.
Set channel status register set to 0.
Set channel status register sweep buffer enable to 0.
Setting interrupt Mask to 0.
Set enabled register set enable to 0.
Set register select switch to 0.
Set LVL, HIEN, LOWN, REQD to that of RSPI4 TX/RX register.

Figure 5-9 DMA Configuration
5.3.3 RSPI Configuration

Figure 5-10 shows the RSPI4 configuration in slave mode. RSPI4 configuration occurs when either SW2 or SW3 is pressed after the user is prompted to choose an SPI mode.

```
R_SPI4_Init()

Enable slave mode

Configure GPIO ports

Enable RX and TX empty interrupts

End
```

0 byte in TX buffer triggers TX empty and 1 byte in RX buffer trigger RX empty interrupts

CPHA = 1

Transfer data length set to 8-bits

Slave select polarity set to 0-active

Disable interrupts, transmission and reception

Figure 5-10 Slave Mode SPI Configuration
Figure 5-11 shows RSPI4 configuration in master mode.

- **R_SPI4_Init()**
- Disable interrupts, transmission and reception
- Set baud rate to 6.67Mbits/s
- Transfer data length set to 8-bits
- Sequence length set to 1
- Slave select polarity set to 0-active
- Slave select negation and RSPCK clock delays set to 1 RSPCK.
- Next access delay set to 1 RSPCK + 2 peripheral 1 clock cycles
- CPHA = 1
- Enable master mode
- 0 byte in TX buffer triggers TX empty and 1 byte in RX buffer trigger RX empty interrupts
- Configure GPIO ports
- Enable RX and TX empty interrupts
- End

**Figure 5-11 Master Mode SPI Configuration**
5.3.4 Main Processing

Figure 5-12 shows the flow of the sample program.

![Diagram of Main Processing]

Figure 5-12 Main Processing
6. Two Board reception and transmission

If one PC is to be used for transmission across two RSK+RZA1Hs, it will be necessary to bootload the sample code into the NOR of one or both RSKs. The PC can be used to run one of the RSKs via the debugger and the other RSK can run from NOR. Alternatively, both RSKs can run from NOR.

For stand-alone operation of both RSKs, load the same sample code on both boards as outlined in section 6.1. Once the sample code is successfully loaded onto both boards, follow the instructions on PMOD to carry out data transmission.

6.1 Bootloading in NOR

This section is used for reference to program sample code into NOR flash to allow stand-alone operation. This requires SEGGER J-Link programmer/debugger.

Supplied with this sample is a batch file ‘LoadUserApplicationToNor.bat’

The instructions follows as;

- Build the ‘RZ_A1H_HSSS_DMA’ sample in either/both ‘HardwareDebug’ and/or ‘Release’ mode.
- Setting the correct path to JLink.exe might be necessary. To do this, open ‘LoadUserApplicationToNor.bat’ using any text editing program and set the correct path to where JLink.exe is located on the PC being used. Only lines 48, 53, 59 and 64 of the .bat file need to be modified depending on whether PC being used is 32-bit or 64-bit.
- Ensure that SW6 is configured as outlined in Table 6-1.

<table>
<thead>
<tr>
<th>SW6</th>
<th>SW6.1</th>
<th>SW6.2</th>
<th>SW6.3</th>
<th>SW6.4</th>
<th>SW6.5</th>
<th>SW6.6</th>
</tr>
</thead>
<tbody>
<tr>
<td>STATE</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
<td>ON</td>
</tr>
</tbody>
</table>

Table 6-1 SW6 Setting

- Double click on ‘LoadUserApplicationToNor.bat’ and follow the on-screen instructions.

7. Sample Code

The sample code is available on the Renesas Electronics Website.
Website and Support

Renesas Electronics Website
http://www.renesas.com/

Inquiries
http://www.renesas.com/contact/
## Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>Jan 11, 2016</td>
<td>All</td>
<td>Created.</td>
</tr>
</tbody>
</table>
General Precautions in the Handling of MPU/MCU Products

The following usage notes are applicable to all MPU/MCU products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   - The characteristics of an MPU or MCU in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.