Introduction

This application note describes how the timer array unit (TAU) measures time intervals between pulses. This unit measures the time elapsed between pulses which arrive at the timer input pin (TI00). Then, it stores the measured value in the on-chip RAM.

Target Device

RL78/G13

When applying the sample program covered in this application note to another microcomputer, modify the program according to the specifications for the target microcomputer and conduct an extensive evaluation of the modified program.
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1. Specifications

This application note describes the measurement of time intervals between input pulses on channel 0 of the timer array unit (TAU). Each time a valid edge is detected on the timer input pin (TI00), the count value of the timer is captured to measure the pulse interval. The measurement result is stored in the on-chip RAM.

Table 1.1 shows the required peripheral functions and their uses. Figure 1.1 presents an overview of the pulse interval measurement.

Table 1.1 Required Peripheral Functions and Their Uses

<table>
<thead>
<tr>
<th>Peripheral function</th>
<th>Use</th>
</tr>
</thead>
<tbody>
<tr>
<td>Timer array unit channel 0</td>
<td>Measurement of the time interval between input pulses on the timer input pin (TI00)</td>
</tr>
<tr>
<td>TI00</td>
<td>Input pin for pulse signals</td>
</tr>
</tbody>
</table>

Each time a pulse interval is measured, the measurement result is stored in the on-chip RAM.
2. Operation Check Conditions
The sample code described in this application note has been checked under the conditions listed in the table below.

<table>
<thead>
<tr>
<th>Item</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>Microcontroller used</td>
<td>RL78/G13 (R5F100LEA)</td>
</tr>
<tr>
<td>Operating frequency</td>
<td>• High-speed on-chip oscillator (HOCO) clock: 32 MHz</td>
</tr>
<tr>
<td></td>
<td>• CPU/peripheral hardware clock: 32 MHz</td>
</tr>
<tr>
<td>Operating voltage</td>
<td>5.0 V (Operation is possible over a voltage range of 2.9 V to 5.5 V.)</td>
</tr>
<tr>
<td></td>
<td>LVD operation (VLVI): Reset mode which uses 2.81 V (2.76 V to 2.87 V)</td>
</tr>
<tr>
<td>Integrated development environment (CubeSuite+)</td>
<td>CubeSuite+ V1.00.01 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>C compiler (CubeSuite+)</td>
<td>CA78K0R V1.20 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development environment (e2studio)</td>
<td>e2studio V2.0.1.3 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>C compiler (e2studio)</td>
<td>KPIT GNU R78-ELF Toolchain V13.02 from Renesas Electronics Corp.</td>
</tr>
<tr>
<td>Integrated development environment (IAR)</td>
<td>IAR Embedded Workbench for Renesas RL78 V1.30.2</td>
</tr>
<tr>
<td>C compiler (IAR)</td>
<td>IAR C/C++ Compiler for Renesas RL78 V1.30.2</td>
</tr>
</tbody>
</table>

3. Related Application Note
The application note that is related to this application note is listed below for reference.

- RL78/G13 Initialization (R01AN0451EJ0100) Application Note
4. Description of the Hardware

4.1 Hardware Configuration Example

Figure 4.1 shows an example of the hardware configuration used for this application note.

![Figure 4.1 Hardware Configuration](image)

Notes:
1. The purpose of this circuit is only to provide the connection outline and the circuit is simplified accordingly. When designing and implementing an actual circuit, provide proper pin treatment and make sure that the hardware's electrical specifications are met (connect the input-only ports separately to VDD or VSS via a resistor).
2. Connect any pins whose name begins with EVSS to VSS and any pins whose name begins with EVDD to VDD, respectively.
3. VDD must be held at not lower than the reset release voltage (VLVI) that is specified as LVD.

4.2 Pin to be Used

Table 4.1 shows the pin to be used and its function.

<table>
<thead>
<tr>
<th>Pin Name</th>
<th>I/O</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>P00/TI00</td>
<td>Input</td>
<td>Inputs pulse signals to the 16-bit timer 00.</td>
</tr>
</tbody>
</table>
5. Description of the Software

5.1 Operation Outline

Each time a rising edge (valid edge) is detected on the timer input pin (TI00), the sample code described in this application note captures the count value of the timer and measures the time interval between pulses which arrive at the timer input pin (TI00). When a timer interrupt (INTTM00) occurs upon completion of the capture, the sample code calculates the pulse interval and stores the calculation result in the on-chip RAM.

1. Initialize the TAU.

<Conditions for setting>
- Use the P00/TI00 pin to receive pulses.
- The operation clock for TAU channel 0 should be $f_{CLK}$.
- Set TAU channel 0 to the capture mode.
- Selects “rising edge detection” as the input edge on the TI00 pin.
- Selects the TI00 pin input valid edge to trigger the capture.

2. Set the TS00 bit of the timer channel start register 0 (TS0) to 1 to enable count operation. This clears the timer count register (TCR00) to 0000H and starts counting.

3. When a valid edge is detected, the value of the timer count register (TCR00) is captured and put into the timer data register (TDR00). A timer interrupt (INTTM00) occurs upon completion of the capture. The timer count register (TCR00) is cleared to 0000H and the TAU waits for the next valid edge input. An invalid value is captured when a timer interrupt (INTTM00) occurs upon completion of the first capture. This data is not used.

4. In the processing of a timer interrupt (INTTM00) which occurs upon completion of the second capture, the timer data register (TDR00)’s value (pulse width) is stored in the on-chip RAM.

5. The operation described in (4) above is repeated eight times. Then, the TAU transitions to the HALT state.
5.2 List of Option Byte Settings
Table 5.1 summarizes the settings of the option bytes.

Table 5.1 Option Byte Settings

<table>
<thead>
<tr>
<th>Address</th>
<th>Value</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>000C0H/010C0H</td>
<td>01101110B</td>
<td>Disables the watchdog timer. (Stops counting after the release from the reset state.)</td>
</tr>
<tr>
<td>000C1H/010C1H</td>
<td>01111111B</td>
<td>LVD reset mode 2.81 V (2.76 V to 2.87 V)</td>
</tr>
<tr>
<td>000C2H/010C2H</td>
<td>11101000B</td>
<td>HS mode HOCO: 32 MHz</td>
</tr>
<tr>
<td>000C3H/010C3H</td>
<td>1000100B</td>
<td>Enables the on-chip debugger.</td>
</tr>
</tbody>
</table>

5.3 List of Constants
Table 5.2 lists the constant that is used in this sample program.

Table 5.2 Constant for the Sample Program

<table>
<thead>
<tr>
<th>Constant</th>
<th>Setting</th>
<th>Description</th>
</tr>
</thead>
<tbody>
<tr>
<td>_0001_TAU_OVERFLOW_OCCURS</td>
<td>0x0001U</td>
<td>Detects an overflow.</td>
</tr>
</tbody>
</table>

5.4 List of Variables
Table 5.3 lists the global variables.

Table 5.3 Global Variables

<table>
<thead>
<tr>
<th>Type</th>
<th>Variable Name</th>
<th>Contents</th>
<th>Function Used</th>
</tr>
</thead>
<tbody>
<tr>
<td>uint8_t</td>
<td>g_Times</td>
<td>Holds the number of times a pulse interval measurement is to be made.</td>
<td>main()</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>R_TAU0_Channel0_Interrupt()</td>
</tr>
<tr>
<td>sreg uint32_t</td>
<td>g_PulseWidth[8]</td>
<td>Holds the measured pulse interval.</td>
<td>main()</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>R_TAU0_Channel0_Interrupt()</td>
</tr>
<tr>
<td>volatile uint32_t</td>
<td>g_Tau0Ch0Width</td>
<td>Temporary buffer which holds the measured pulse interval</td>
<td>R_TAU0_Channel0_Interrupt()</td>
</tr>
</tbody>
</table>
5.5 List of Functions

Table 5.4 lists the functions that are used in this sample program.

<table>
<thead>
<tr>
<th>Function Name</th>
<th>Outline</th>
</tr>
</thead>
<tbody>
<tr>
<td>R_TAU0_Channel0_Start</td>
<td>TAU0 channel 0 start processing</td>
</tr>
<tr>
<td>R_TAU0_Channel0_Interrupt</td>
<td>INTTM00 interrupt processing</td>
</tr>
</tbody>
</table>

5.6 Function Specifications

This section describes the specifications for the functions that are used in this sample program.

**[Function Name] R_TAU0_Channel0_Start**

**Synopsis**
TAU0 channel 0 start processing

**Header**
```
#include "r_cg_macrodriver.h"
#include "r_cg_timer.h"
#include "r_cg_userdefine.h"
```

**Declaration**
```
void R_TAU0_Channel0_Start(void)
```

**Explanation**
This function unmasks TAU0 channel 0 interrupts and starts count operation.

**Arguments**
None

**Return value**
None

**Remarks**
None

**[Function Name] R_TAU0_Channel0_Interrupt**

**Synopsis**
INTTM00 interrupt processing

**Header**
```
#include "r_cg_macrodriver.h"
#include "r_cg_timer.h"
#include "r_cg_userdefine.h"
```

**Declaration**
```
__interrupt void R_TAU0_Channel0_Interrupt(void)
```

**Explanation**
This function stores the measured value of the pulse time interval into g_PulseWidth[].

**Arguments**
None

**Return value**
None

**Remarks**
None
5.7 Flowcharts

Figure 5.1 shows the overall flow of the sample program described in this application note.

![Overall Flow Diagram](attachment:image)

Figure 5.1 Overall Flow

5.7.1 Initialization Function

Figure 5.2 shows the flowchart for the initialization function.

![Initialization Function Diagram](attachment:image)

Figure 5.2 Initialization Function

Note: The __low_level_init function initializes the system in the IAR Workbench IDE-Oriented sample code.
5.7.2 System Function

Figure 5.3 shows the flowchart for the system function.

```plaintext
R_Systeminit()

Disuse peripheral I/O redirection function
PIOR register ← 00000000B

Set up I/O ports
R_PORT_Create()

Set up CPU clock
R_CGC_Create()

Set up timer array unit
R_TAU0_Create();

return
```

Figure 5.3 System Function
5.7.3 I/O Port Setup

Figure 5.4 shows the flowchart for setting up the I/O ports.

```
R_PORT_Create()

Set up pulse waveform input
Set P00 to input mode

P0 register ← 00H
PM0 register ← 01H

return
```

**Note:** Refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100) for the configuration of the unused ports.

**Caution:** Provide proper treatment for unused pins so that their electrical specifications are observed. Connect each of any unused input-only ports to V_DD or V_SS via a separate resistor.
5.7.4 CPU Clock Setup

Figure 5.5 shows the flowchart for setting up the CPU clock.

Caution: For details on the procedure for setting up the CPU clock (R_CGC_Create()), refer to the section entitled "Flowcharts" in RL78/G13 Initialization Application Note (R01AN0451EJ0100).
5.7.5 Timer Array Unit Setup

Figure 5.6 shows the flowchart for setting up the timer array unit.

Figure 5.6   Timer Array Unit Setup

- Supply clock signals to timer array unit
- Set up TAU0 operation
  - TAU0 operation clock settings (high-speed on-chip oscillator clock: 32 MHz)
  - Operation clock 0 (CK00): 8 MHz
  - Operation clock 1 (CK01): 32 MHz
  - Operation clock 2 (CK02): 16 MHz
  - Operation clock 3 (CK03): 125 kHz
- Deactivate timer array unit 0
- Disable TAU interrupts
- Clear TAU interrupt request flag
- Set TAU interrupt priority level to 3
- Initialize TAU channel 0
  - Operation clock: CK00
  - Operation mode: Capture mode
  - Valid edge: Rising edge
  - Functional feature: Independent channel operation function
  - Trigger: Valid edge
  - Timer output: Disabled
- TAU0EN bit ← 1
- TPS0 register ← 0002H
- TT0 register ← 00H
- TMMK00 bit ← 1
- TMMIF bit ← 0
- TMPR100 bit ← 1
- TMPR000 bit ← 1
- TMR00 register ← 0144H
- TO0 register ← 00H
- TOE0 register ← 00H
- return
Starting clock signal supply to the timer array unit

- Peripheral enable register 0 (PER0)
  Supply clock signals to the timer array unit.

Symbol: PER0

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>RTCEN</td>
<td>IICA1EN</td>
<td>ADCEN</td>
<td>IICA0EN</td>
<td>SAU1EN</td>
<td>SAU0EN</td>
<td>TAU1EN</td>
<td>TAU0EN</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>TAU0EN</th>
<th>Control of timer array unit 0 input clock supply</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Stops input clock supply.</td>
</tr>
<tr>
<td>1</td>
<td>Enables input clock supply.</td>
</tr>
</tbody>
</table>

Configuring the clock frequency

- Timer clock select register 0 (TPS0)
  Select the CK00 operation clock.

Symbol: TPS0

<table>
<thead>
<tr>
<th>Symbol: TT0</th>
<th>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1 0</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Operation clock (CK00) selection</th>
</tr>
</thead>
<tbody>
<tr>
<td>( f_{\text{CLK}} = 2 \text{ MHz} )</td>
</tr>
<tr>
<td>250 kHz</td>
</tr>
<tr>
<td>250 kHz</td>
</tr>
<tr>
<td>7.81 kHz</td>
</tr>
<tr>
<td>7.81 kHz</td>
</tr>
<tr>
<td>3.91 kHz</td>
</tr>
<tr>
<td>3.91 kHz</td>
</tr>
<tr>
<td>1.95 kHz</td>
</tr>
<tr>
<td>1.95 kHz</td>
</tr>
<tr>
<td>1.22 kHz</td>
</tr>
<tr>
<td>1.22 kHz</td>
</tr>
<tr>
<td>61 Hz</td>
</tr>
<tr>
<td>61 Hz</td>
</tr>
<tr>
<td>15.62 kHz</td>
</tr>
<tr>
<td>15.62 kHz</td>
</tr>
<tr>
<td>7.81 kHz</td>
</tr>
<tr>
<td>7.81 kHz</td>
</tr>
<tr>
<td>3.91 kHz</td>
</tr>
<tr>
<td>3.91 kHz</td>
</tr>
</tbody>
</table>


Controlling the channel trigger operation

- Timer channel stop register 0 (TT0)
  Select the TAU0 stop trigger.

Symbol: TT0

<table>
<thead>
<tr>
<th>Symbol: TT0</th>
<th>15 14 13 12 11 10 9 8 7 6 5 4 3 2 1 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 0</td>
</tr>
</tbody>
</table>

<table>
<thead>
<tr>
<th>Bit 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TT00</td>
</tr>
<tr>
<td>0</td>
</tr>
<tr>
<td>1</td>
</tr>
</tbody>
</table>

Setting up the channel 0 operation mode

- Timer mode register 00 (TMR00)
 Specify the operation mode, edge, trigger, channel and clocks.

Symbol: TMR00

<table>
<thead>
<tr>
<th>CKS 001</th>
<th>CKS 000</th>
<th>0</th>
<th>CCS 00</th>
<th>MAST ER00</th>
<th>STS 002</th>
<th>STS 001</th>
<th>STS 000</th>
<th>CIS 001</th>
<th>CIS 000</th>
<th>0</th>
<th>0</th>
<th>MD 003</th>
<th>MD 002</th>
<th>MD 001</th>
<th>MD 000</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
</tr>
</tbody>
</table>

Bits 3 to 0

<table>
<thead>
<tr>
<th>MD 003</th>
<th>MD 002</th>
<th>MD 001</th>
<th>MD 000</th>
<th>Channel 0 operation mode setup</th>
</tr>
</thead>
</table>
| 0      | 0      | 0      | 0      | Interval timer mode.  
Does not generate a timer interrupt at the start of count operation. |
| 1      | 0      | 0      | 0      | Interval timer mode.  
Generates a timer interrupt at the start of count operation. |
| 0      | 1      | 0      | 0      | Capture mode  
Does not generate a timer interrupt at the start of count operation. |
| 1      | 1      | 0      | 0      | Capture & one-count mode  
Does not generate a timer interrupt at the start of count operation.  
Disables the start trigger during count operation. |
| 0      | 0      | 1      | 1      | Event counter mode  
Does not generate a timer interrupt at the start of count operation. |
| 1      | 0      | 0      | 0      | One-count mode  
Disables the start trigger during count operation. |
| 1      | 1      | 0      | 0      | One-count mode  
Enables the start trigger during count operation. |

Bits 7 and 6

<table>
<thead>
<tr>
<th>CIS 001</th>
<th>CIS 000</th>
<th>Selection of TI00 pin input valid edge</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Falling edge</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>Rising edge</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Both edges (when low-level width is measured)</td>
</tr>
<tr>
<td>1</td>
<td>1</td>
<td>Both edges (when high-level width is measured)</td>
</tr>
</tbody>
</table>

Symbol: TMR00

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>CKS001</td>
<td>CKS000</td>
<td>0</td>
<td>CCS00</td>
<td>MAST00</td>
<td>STS002</td>
<td>STS001</td>
<td>STS000</td>
<td>CIS001</td>
<td>CIS000</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
<td>0</td>
<td>0</td>
<td></td>
</tr>
</tbody>
</table>

Bits 10 to 8

<table>
<thead>
<tr>
<th>STS002</th>
<th>STS001</th>
<th>STS000</th>
<th>Setting of start trigger or capture trigger of channel 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>Only software trigger start is valid (other trigger sources are unselected).</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>1</td>
<td>Valid edge of the TI00 pin input is used as both the start trigger and capture trigger.</td>
</tr>
<tr>
<td>0</td>
<td>1</td>
<td>0</td>
<td>Both the edges of the TI00 pin input are used as a start trigger and capture trigger.</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>0</td>
<td>Interrupt signal of the master channel is used (when the channel is used as a slave channel with the simultaneous channel operation function).</td>
</tr>
</tbody>
</table>

Bit 11

<table>
<thead>
<tr>
<th>MASTER00</th>
<th>Selection between using channel 0 independently or simultaneously with another channel (as a slave or master)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Operates in independent channel operation function or as slave channel in simultaneous channel operation function.</td>
</tr>
<tr>
<td>1</td>
<td>Operates as master channel in simultaneous channel operation function.</td>
</tr>
</tbody>
</table>

Bit 12

<table>
<thead>
<tr>
<th>CCS00</th>
<th>Selection of count clock ( f_{\text{CLK}} ) of channel 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Operation clock ( f_{\text{MCK}} ) specified with the CKS000 and CKS001 bits</td>
</tr>
<tr>
<td>1</td>
<td>Valid edge of the input signal from the TI00 pin</td>
</tr>
</tbody>
</table>

Bits 15 and 14

<table>
<thead>
<tr>
<th>CKS001</th>
<th>CKS000</th>
<th>Selection of operation clock ( f_{MCK} ) of channel 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>Operation clock CK00 set by timer clock select register 0 (TPS0)</td>
</tr>
<tr>
<td>1</td>
<td>0</td>
<td>Operation clock CK01 set by timer clock select register 0 (TPS0)</td>
</tr>
</tbody>
</table>

5.7.6 Main Processing

Figure 5.7 shows the flowchart for main processing.

Figure 5.7   Main Processing

```
main()

Disable interrupts

Start operation of timer array unit
R_TAU0_Channel0_Start()

Make transition to HALT mode

Detect first rising edge

TMIF00 bit ← 0: Clears INTTM00 interrupt request flag.

Set valid-edge measurement count (8)

g_ucTimes ← 08H
g_ucTimes: Variable in RAM

Enable interrupts

IE ← 1

Make transition to HALT mode

Detect second and subsequent rising edges

Has measurement count reached 8?

No

Yes

Make transition to HALT mode
```
5.7.7 Timer Array Unit Startup

Figure 5.8 shows the flowchart for starting the operation of the timer array unit.

```
R_TAU0_Channel0_Start()

Start operation of TAU channel 0
```

- TMIF00 bit ← 0: Clears interrupt request flag.
- TMMK00 bit ← 0: Enables TAU interrupt processing.
- TS0 register ← 01h

**Figure 5.8 Timer Array Unit Startup**

Configuring the interrupt request flag

- Clear the timer interrupt request flag.

Symbol: IF1L

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMIF03</td>
<td>TMIF02</td>
<td>TMIF01</td>
<td>TMIF00</td>
<td>IICAIF0</td>
<td>SREIF1</td>
<td>TMIF03H</td>
<td>SRIF1</td>
</tr>
<tr>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
<td>0</td>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
</tr>
<tr>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
<td>0</td>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
</tr>
</tbody>
</table>

**Bit 4**

<table>
<thead>
<tr>
<th>TMIF00</th>
<th>Interrupt request flag</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No interrupt request signal is generated</td>
</tr>
<tr>
<td>1</td>
<td>Interrupt request is generated, interrupt request status</td>
</tr>
</tbody>
</table>

Configuring the interrupt mask

- Unmask timer interrupts.

Symbol: MK1L

<table>
<thead>
<tr>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>TMMK03</td>
<td>TMMK02</td>
<td>TMMK01</td>
<td>TMMK00</td>
<td>IICAMK0</td>
<td>SREM1K</td>
<td>SRMK1</td>
<td>STMK1</td>
</tr>
<tr>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
<td>0</td>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
<td>0/1</td>
</tr>
</tbody>
</table>

Bit 4

<table>
<thead>
<tr>
<th>TMMK00</th>
<th>Interrupt processing control</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>Enables interrupt processing.</td>
</tr>
<tr>
<td>1</td>
<td>Disables interrupt processing.</td>
</tr>
</tbody>
</table>


Configuring the timer channel startup

- Enable timer count operation.

Symbol: TS0

<table>
<thead>
<tr>
<th>15</th>
<th>14</th>
<th>13</th>
<th>12</th>
<th>11</th>
<th>10</th>
<th>9</th>
<th>8</th>
<th>7</th>
<th>6</th>
<th>5</th>
<th>4</th>
<th>3</th>
<th>2</th>
<th>1</th>
<th>0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>TS</td>
<td>H03</td>
<td>0</td>
<td>TS</td>
<td>H01</td>
<td>0</td>
<td>TS</td>
<td>07</td>
<td>TS</td>
<td>06</td>
<td>TS</td>
<td>05</td>
</tr>
<tr>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>0</td>
<td>1</td>
</tr>
</tbody>
</table>

Bit 0

<table>
<thead>
<tr>
<th>TS00</th>
<th>Operation enable (start) trigger of channel 0</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>No trigger operation</td>
</tr>
<tr>
<td>1</td>
<td>The TE00 bit is set to 1 and the count operation becomes enabled.</td>
</tr>
</tbody>
</table>

6. Sample Code
The sample code is available on the Renesas Electronics Website.

7. Documents for Reference
User’s Manual:
- RL78/G13 User's Manual: Hardware (R01UH0146EJ)
  The latest version can be downloaded from the Renesas Electronics website.

Technical Updates/Technical News
The latest information can be downloaded from the Renesas Electronics website.

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<table>
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<th>Page</th>
<th>Description</th>
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<td>1.00</td>
<td>Sep. 30, 2011</td>
<td>—</td>
<td>First edition issued</td>
</tr>
<tr>
<td>2.00</td>
<td>Dec. 27, 2013</td>
<td>4</td>
<td>Table 2.1: Added e2studio and IAR information</td>
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<td></td>
<td>9</td>
<td>Added note</td>
</tr>
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<td></td>
<td></td>
<td></td>
<td>Figure 5.2: Fixed typo in function name</td>
</tr>
<tr>
<td></td>
<td></td>
<td>10</td>
<td>Figure 5.3: Fixed typo in function name</td>
</tr>
<tr>
<td></td>
<td></td>
<td>11</td>
<td>Figure 5.4: Fixed typo in function name</td>
</tr>
</tbody>
</table>

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General Precautions in the Handling of MPU/MCU Products

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1. Handling of Unused Pins
   Handle unused pins in accord with the directions given under Handling of Unused Pins in the manual.
   — The input pins of CMOS products are generally in the high-impedance state. In operation with unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable.
   When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to one with a different part number, confirm that the change will not lead to problems.
   — The characteristics of MPU/MCU in the same group but having different a different part number may differ in terms of the internal memory capacity and layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to products with a different part number, implement a system-evaluation test for the given product.
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Renesas Electronics America Inc.
2850 Scott Boulevard Santa Clara, CA 95055-2554, U.S.A.
Tel: +1-408-588-6000, Fax: +1-408-588-6133

Renesas Electronics Canada Limited
1101 Nicholson Road, Newmarket, Ontario L3Y 9C3, Canada
Tel: +1-905-898-5441, Fax: +1-905-898-3220

Renesas Electronics Europe Limited
Dukes Meadow, Milton Road, Bourne End, Buckinghamshire, SL8 5FH, U.K.
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadianstrasse 10 40472 Düsseldorf, Germany
Tel: +49-211-65030, Fax: +49-211-6503-1327

Renesas Electronics (Shanghai) Co., Ltd.
Unit 204, 205, AZIA Center, No.1233 Lujiazui Ring Rd., Pudong District, Shanghai 200120, China
Tel: +86-21-5877-1818, Fax: +86-21-6887-7888 / -7898

Renesas Electronics Hong Kong Limited
Unit 1501-1513, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2886-9318, Fax: +852 2886-9022/9044

Renesas Electronics Taiwan Co., Ltd.
1F., No. 315, Section 3, Zhonghua North Road, Taipei, Taiwan
Tel: +886-2-6175-9600, Fax: +886-2-6175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bedok North Road, Unit 505-02 Hyflux Innovation Centre Singapore 339948
Tel: +65-6213-0200, Fax: +65-6213-0100

Renesas Electronics Malaysia Sdn.Bhd.
Unit 35G, Block B, Menara Ritzco, Artylo Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics Korea Co., Ltd.
1F., South Korea Trade Tower 272-2, Yeoksam-Dong, Kangnam-Ku, Seoul 135-080, Korea
Tel: +82-2-588-3177, Fax: +82-2-588-5141

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