RNA51957A, B
Voltage Detecting, System Resetting IC Series

Description
RNA51957A,B are semiconductor integrated circuits for resetting of all types of logic circuits such as CPUs, and has the feature of setting the detection voltage by adding external resistance. They include a built-in delay circuit to provide the desired retardation time simply by adding an external capacitor. They find extensive applications, including battery checking circuit, level detecting circuit and waveform shaping circuit.

Features
- Few external parts
- Large delay time with a capacitor of small capacitance (td ≈ 100 ms, at 0.33 μF)
- Low threshold operating voltage (Supply voltage to keep low-state at low supply voltage): 0.6 V (Typ) at RL = 22 kΩ
- Wide supply voltage range: 2 V to 17 V
- Wide application range
- Ordering Information

<table>
<thead>
<tr>
<th>Part Name</th>
<th>Package Type</th>
<th>Package Code</th>
<th>Package Abbreviation</th>
<th>Taping Abbreviation (Quantity)</th>
<th>Surface Treatment</th>
</tr>
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<tbody>
<tr>
<td>RNA51957AFPH0</td>
<td>SOP-8 pin</td>
<td>PRSP0008DE-C</td>
<td>FP</td>
<td>H (2,500 pcs / Reel)</td>
<td>0 (Ni/Pd/Au)</td>
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<tr>
<td>RNA51957APT0</td>
<td>DIP-8 pin</td>
<td>PRDP0008AF-B</td>
<td>P</td>
<td>T (1,000 pcs / Box)</td>
<td>0 (Ni/Pd/Au)</td>
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<tr>
<td>RNA51957BFPH0</td>
<td>SOP-8 pin</td>
<td>PRSP0008DE-C</td>
<td>FP</td>
<td>H (2,500 pcs / Reel)</td>
<td>0 (Ni/Pd/Au)</td>
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<td>RNA51957BPT0</td>
<td>DIP-8 pin</td>
<td>PRDP0008AF-B</td>
<td>P</td>
<td>T (1,000 pcs / Box)</td>
<td>0 (Ni/Pd/Au)</td>
</tr>
</tbody>
</table>

Application
- Reset circuit of Pch, Nch, CMOS, microcomputer, CPU and MCU, Reset of logic circuit, Battery check circuit, switching circuit back-up voltage, level detecting circuit, waveform shaping circuit, delay waveform generating circuit, DC/DC converter, over voltage protection circuit

Recommended Operating Condition
- Supply voltage range: 2 V to 17 V
Outline and Article Indication

- RNA51957A, B

Pin Arrangement

RNA51957A, B

- NC: No Connection

Outline: PRSP0008DE-C (SOP-8)
PRDP0008AF-B (DIP-8)
**Block Diagram**

![Block Diagram of RNA51957A, B](image)

**Operating Waveform**

![Operating Waveform of RNA51957A, B](image)

1.25 V

Input voltage

Output state

H

L

\[ \text{td} \approx 0.34 \times C_d \times \mu s \]
### Absolute Maximum Ratings

(Ta = 25°C, unless otherwise noted)

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Ratings</th>
<th>Unit</th>
<th>Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Supply voltage</td>
<td>VCC</td>
<td>18</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Output sink current</td>
<td>Isink</td>
<td>6</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Output voltage</td>
<td>VO</td>
<td>VCC</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>18</td>
<td></td>
<td>Type A (output with constant current load)</td>
</tr>
<tr>
<td></td>
<td></td>
<td>570</td>
<td>mW</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>8.3</td>
<td></td>
<td>Type B (open collector output)</td>
</tr>
<tr>
<td>Power dissipation</td>
<td>Pd</td>
<td>400</td>
<td>mW</td>
<td>8-pin SO...</td>
</tr>
<tr>
<td></td>
<td></td>
<td>4.4</td>
<td></td>
<td>8-pin SOP (PRSP0008DE-C)</td>
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<tr>
<td></td>
<td></td>
<td>8.3</td>
<td></td>
<td>8-pin DIP (PRDP0008AF-B)</td>
</tr>
<tr>
<td>Thermal derating</td>
<td>Kt</td>
<td>1.4</td>
<td>mW/°C</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.4</td>
<td></td>
<td>Refer to the thermal derating curve.</td>
</tr>
<tr>
<td>Operating temperature</td>
<td>Topr</td>
<td>–40 to +85</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Storage temperature</td>
<td>Tstg</td>
<td>–55 to +125</td>
<td>°C</td>
<td></td>
</tr>
<tr>
<td>Input voltage range</td>
<td>VIN</td>
<td>–0.3 to VCC</td>
<td>V</td>
<td>VCC ≤ 7 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–0.3 to +7</td>
<td></td>
<td>VCC &gt; 7 V</td>
</tr>
</tbody>
</table>

### Electrical Characteristics

(Ta = 25°C, unless otherwise noted)

- “L” reset type

<table>
<thead>
<tr>
<th>Item</th>
<th>Symbol</th>
<th>Min</th>
<th>Typ</th>
<th>Max</th>
<th>Unit</th>
<th>Test Conditions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Detecting voltage</td>
<td>VS</td>
<td>1.20</td>
<td>1.25</td>
<td>1.30</td>
<td>V</td>
<td>VCC ≤ 7 V</td>
</tr>
<tr>
<td>Hysteresis voltage</td>
<td>ΔVS</td>
<td>9</td>
<td>15</td>
<td>23</td>
<td>mV</td>
<td>VCC = 5V</td>
</tr>
<tr>
<td>Detecting voltage</td>
<td>VS/ΔT</td>
<td></td>
<td>0.01</td>
<td></td>
<td>%/°C</td>
<td>Type A, VCC = 5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td>Type B, VCC = 5V</td>
</tr>
<tr>
<td>Supply voltage range</td>
<td>VCC</td>
<td>2</td>
<td>17</td>
<td></td>
<td>V</td>
<td>VCC = 5V</td>
</tr>
<tr>
<td>Input voltage range</td>
<td>VIN</td>
<td>–0.3</td>
<td></td>
<td>VCC</td>
<td>V</td>
<td>VCC &gt; 7 V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>–0.3</td>
<td></td>
<td>7.0</td>
<td>V</td>
<td>VCC = 5V</td>
</tr>
<tr>
<td>Input current</td>
<td>IIN</td>
<td></td>
<td>100</td>
<td>500</td>
<td>nA</td>
<td>VIN = 1.25V</td>
</tr>
<tr>
<td>Circuit current</td>
<td>ICC</td>
<td></td>
<td>390</td>
<td>590</td>
<td>μA</td>
<td>Type A, VCC = 5V</td>
</tr>
<tr>
<td></td>
<td></td>
<td></td>
<td>360</td>
<td>540</td>
<td></td>
<td>Type B, VCC = 5V</td>
</tr>
<tr>
<td>Delay time</td>
<td>tpd</td>
<td>1.6</td>
<td>3.4</td>
<td>7.0</td>
<td>ms</td>
<td>Cd = 0.01μF *</td>
</tr>
<tr>
<td>Constant current</td>
<td>Ipq</td>
<td>–8</td>
<td>–5</td>
<td>–3</td>
<td>μA</td>
<td>VCC = 5V</td>
</tr>
<tr>
<td>Output saturation voltage</td>
<td>Vsat</td>
<td></td>
<td>0.2</td>
<td>0.4</td>
<td>V</td>
<td>L reset type, VCC = 5V, VIN &lt; 1.2V, Isink = 4mA</td>
</tr>
<tr>
<td>Threshold operating voltage</td>
<td>VOLT</td>
<td>0.57</td>
<td>0.7</td>
<td></td>
<td>V</td>
<td>Rl = 2.2kΩ, Vsat ≤ 0.4V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>0.55</td>
<td>0.7</td>
<td></td>
<td></td>
<td>Rl = 100kΩ, Vsat ≤ 0.4V</td>
</tr>
<tr>
<td>Output leakage current</td>
<td>IOL</td>
<td></td>
<td>30</td>
<td></td>
<td>nA</td>
<td>Type B</td>
</tr>
<tr>
<td>Output load current</td>
<td>VOL</td>
<td>40</td>
<td>25</td>
<td>17</td>
<td>μA</td>
<td>Type A, VCC = 5V, VO = 1/2 x VCC</td>
</tr>
<tr>
<td>Output high voltage</td>
<td>VOL</td>
<td>VCC–0.2</td>
<td>VCC–0.06</td>
<td></td>
<td>V</td>
<td>Type A</td>
</tr>
</tbody>
</table>

Note: Please set the desired delay time by attaching capacitor of the range between 4700 pF and 10 μF.
Typical Characteristics

**Thermal Derating**

- Power Dissipation $P_d$ (mW)
- Ambient Temperature $T_a$ ($^\circ$C)

**Detection Voltage vs. Ambient Temperature**

- Detection Voltage $V_S$ (V)
- Ambient Temperature $T_a$ ($^\circ$C)

**Detection Voltage vs. Supply Voltage**

- Detection Voltage $V_S$ (V)
- Supply Voltage $V_{CC}$ (V)

**Input Current vs. Supply Voltage**

- Input Current $I_{IN}$ (nA)
- Supply Voltage $V_{CC}$ (V)

**Delay Capacitance vs. Delay Time**

- Delay Capacitance $C_d$ ($\mu$F)
- Delay Time $t_{pd}$ (ms)

**Delay Time vs. Ambient Temperature**

- Delay Time $t_{pd}$ (ms)
- Ambient Temperature $T_a$ ($^\circ$C)

---

**Ambient Temperature $T_a$ ($^\circ$C)**

**Power Dissipation $P_d$ (mW)**

**Detection Voltage $V_S$ (V)**

**Input Current $I_{IN}$ (nA)**

**Delay Capacitance $C_d$ ($\mu$F)**

**Delay Time $t_{pd}$ (ms)**
Supply Voltage $V_{CC}$ (V)

Threshold Operating Voltage

Output Saturation Voltage $V_{sat}$ (V)

Output Load Current vs. Output Voltage

Output Sink Current $I_{sink}$ (mA)

Circuit Current vs. Supply Voltage

Constant Current at Cd pin vs. Ambient Temperature

Output Saturation Voltage vs. Output Sink Current

Supply voltage detecting "L" reset type
- $V_{CC} = 4$ V
- Except above mentioned: $V_{CC} = 5$ V

Constant Current at Cd pin

Ambient Temperature $T_a$ (°C)

Circuit Current $I_{CC}$ (μA)

Canstant Current at Cd pin

Output Voltage $V_{OUT}$ (V)

Output Load Current $I_{CC}$ (μA)

Canstant Current at Cd pin (RNA51957B)

Circuit Current (RNA51957B)

Ambient Temperature $T_a$ (°C)

Canstant Current at Cd pin (RNA51957B)

Circuit Current $I_{CC}$ (μA)

Supply voltage detecting "L" reset type
- $V_{CC} = 4$ V
- Except above mentioned: $V_{CC} = 5$ V

Supply voltage detecting "L" reset type
- $V_{CC} = 4$ V
- Except above mentioned: $V_{CC} = 5$ V

Supply voltage detecting "L" reset type
- $V_{CC} = 4$ V
- Except above mentioned: $V_{CC} = 5$ V

Output Saturation Voltage $V_{sat}$ (V)

Supply Voltage $V_{CC}$ (V)

Threshold Operating Voltage

Output Saturation Voltage $V_{sat}$ (V)

Output Load Current vs. Output Voltage

Output Sink Current $I_{sink}$ (mA)

Circuit Current vs. Supply Voltage

Constant Current at Cd pin vs. Ambient Temperature
Example of Application Circuit

Reset Circuit of RNA51957

![Diagram of Reset Circuit of RNA51957](image)

**Figure 1  Reset Circuit of RNA51957**

Notes:
1. The detecting supply voltage is \( V_s \times \frac{R_1 + R_2}{R_2} \) (V) approximately. \( V_s = 1.25 \) V (Typ)
2. The delay time is about \( 0.34 \times C_d \) (pF) \( \mu s \).
3. If the RNA51957 and the logic circuit share a common power source, type A (built-in load type) can be used whether a pull-up resistor is included in the logic circuit or not.
4. The logic circuit preferably should not have a pull-down resistor, but if one is present, add load resistor \( R_L \) to overcome the pull-down resistor.
5. When a negative supply voltage is used, the supply voltage side of RNA51957 and the GND side are connected to negative supply voltage respectively.

Case of Using Reset Signal except Supply Voltage in the RNA51957

![Diagram of Case of Using Reset Signal except Supply Voltage in the RNA51957](image)

**Figure 2  Case of Using Reset Signal except Supply Voltage in the RNA51957**
Delay Waveform Generating Circuit

When RNA51957 are used, a waveform with a large delay time can generate only by adding a small capacitor.

![Delay Waveform Generating Circuit](image)

**Figure 3** Delay Waveform Generating Circuit

Operating Waveform

![Operating Waveform](image)

\[ t_d = 0.34 \times C_d (\text{pF}) \mu s \]

**Figure 4** Operating Waveform
Notice for use

About the Power Supply Line

1. About bypass capacitor
   Because the ripple and the spike of the high frequency noise and the low frequency are superimposed to the power supply line, it is necessary to remove these. Therefore, please install C1 and C2 for the low frequency and for the high frequency between the power supply line and the GND line as shown in following figure 5.

![Figure 5 Example of Ripple Noise Measures](image)

2. The sequence of voltage impression
   Please do not impress the voltages to the input terminals earlier than the power supply terminal. Moreover, please do not open the power supply terminal with the voltage impressed to the input terminal. (The setting of the bias of an internal circuit collapses, and a parasitic element might operate.)

About the Input Terminal

1. Setting range of input voltage
   The following voltage is recommended to be input to the input terminal (pin 2).
   - about 0.8 (V) < Vin < VCC – 0.3 (V) ... at VCC ≤ 7 V
   - about 0.8 (V) < Vin < 6.7 (V) ............. at VCC > 7 V

2. About using input terminal
   Please do an enough verification to the transition characteristic etc. of the power supply when using independent power supply to input terminal (pin 2).

![Figure 6 Recommended Example](image)
3. Calculation of detecting voltage
Detecting voltage $V_S$ can be calculated by the following expression.
However, the error margin is caused in the detecting voltage because input current $I_{in}$ (standard 100 nA) exists if it sets too big resistance.
Please set the constant to disregard this error margin.

$$V_S = 1.25 \times \left( \frac{R_1 + R_2}{R_2} \right) + I_{in} \times \frac{R_1}{R_1 \text{ error margin}}$$

4. About the voltage input outside ratings
Please do not input the voltage outside ratings to the input terminal.
An internal protection diode becomes order bias, and a large current flows.
Setting of Delay Capacity

Please use capacitor Cd for the delay within the range of 10 μF or less.

When a value that is bigger than this is set, the problem such as following (1), (2), and (3) becomes remarkable.

![Figure 9 Time Chart at Momentary Voltage-Decrease](image)

(1) The difference at delay time becomes remarkable.
A long delay setting of tens of seconds is fundamentally possible. However, when set delay time is lengthened, the range of the difference relatively grows, too. When a set value is assumed to be ‘tpd’, the difference occurs in the range from 0.47 × tpd to 2.05 × tpd. For instance, 34 seconds can be calculated at 100 μF. However, it is likely to vary within the ranges of 16-70 seconds.

(2) Difficulty to react to a momentary voltage decrease.
For example, the reaction time tPHL is 10 μs when delay capacitor Cd = 0.1 μF.
The momentary voltage-decrease that is longer than such tPHL are occurs, the detection becomes possible. When the delay capacitance is enlarged, tPHL also becomes long. For instance, it becomes about 100 to 200 μs in case of circuit constant C1 = 100 μF.
(Characteristic graph 1 is used and extrapolation in case of Cd = 100 μF.)
Therefore, it doesn't react to momentary voltage-decrease that is shorter than this.

(3) Original delay time is not obtained.
When the momentary voltage-decrease time ‘t’ is equivalent to tPHL, the discharge becomes insufficient and the charge starts at that state. This phenomenon occurs at large capacitance. And, original delay time tpd is not obtained.
Please refer to characteristic graph 2. (Delay time versus input pulse width)

![Figure 10 Characteristic Graph](image)
Setting of Output Load Resistance (RNA51957B)

High level output voltage can be set without depending on the power-supply voltage because the output terminal is an open collector type. However, please guard the following notes.

1. Please set it in value (2 V to 17 V) within the range of the power-supply voltage recommendation. Moreover, please never impress the voltage of maximum ratings 18 V or more even momentarily either.
2. Please set output load resistance (pull-up resistance) $R_L$ so that the output current (output inflow current $I_L$) at L level may become 4 mA or less. Moreover, please never exceed absolute maximum rating (6 mA).

![Figure 11 Output Load Resistance $R_L$](image)

Others

1. Notes when IC is handled are published in our reliability handbook, and please refer it. The reliability handbook can be downloaded from our homepage (following URL).
   http://www.renesas.com/products/common_info/reliability/index.jsp
2. Additionally, please inquire of our company when there is an uncertain point on use.
### Package Dimensions

<table>
<thead>
<tr>
<th>JEITA Package Code</th>
<th>RENESAS Code</th>
<th>Previous Code</th>
<th>MASII(Typ.)</th>
</tr>
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<tr>
<td>P-5QP8-4.4x4.85-1.27</td>
<td>PRSP008DE-CC</td>
<td>——</td>
<td>0.1g</td>
</tr>
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</table>

**Terminal cross section (Ni/Pd/Au plating)**

<table>
<thead>
<tr>
<th>Reference Symbol</th>
<th>Dimension in Millimeters</th>
<th>Min</th>
<th>Nom</th>
<th>Max</th>
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<tr>
<td>D</td>
<td>4.65</td>
<td>4.85</td>
<td>5.05</td>
<td></td>
</tr>
<tr>
<td>E</td>
<td>4.2</td>
<td>4.4</td>
<td>4.6</td>
<td></td>
</tr>
<tr>
<td>A1</td>
<td>1.8</td>
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<td></td>
<td></td>
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<tr>
<td>A2</td>
<td>0.00</td>
<td>0.1</td>
<td>0.20</td>
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</tr>
<tr>
<td>A</td>
<td>2.03</td>
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<td></td>
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</tr>
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<td>B1</td>
<td>0.34</td>
<td>0.44</td>
<td>0.64</td>
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<tr>
<td>B2</td>
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<td>0.20</td>
<td>0.25</td>
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<tr>
<td>C1</td>
<td>0.00</td>
<td>0.1</td>
<td>0.20</td>
<td></td>
</tr>
<tr>
<td>C2</td>
<td>0.45</td>
<td>0.65</td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

**Note:**

1. DIMENSIONS**1** (Nom.) and **2** DO NOT INCLUDE MOLD FLASH.
2. DIMENSION**3** DOES NOT INCLUDE TRIM OFFSET.
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