Renesas Synergy™, RL78/G1D

In-Transit Medication Management (ITMM) Kit User Guide

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1. Introduction

Renesas has developed a reference solution for in-transit medication management (ITMM) which enables data logger manufactures to achieve quick time to market. This solution can be thought of as an advanced data logger which enables the supply chain to be compatible to Drug Supply Chain Security Act (DSCSA). This ITMM solution is backward compatible to traditional hand-held scanning systems.

The Renesas ITMM solution has multiple sensors, to track: temperature, humidity, GPS location, tamper, shock and pressure. These parameters are displayed on the onboard display in human readable, and barcode format. A primary cell battery powers the ITMM module, and Bluetooth® low energy technology is used to communicate to a mobile phone. USB port is provided for data transfer or firmware upgrade. Push buttons and LEDs provide HMI functionality to the solution.

This user manual describes the key aspects of the reference design so that OEM/ODM entity can jump start their product development using the reference system

2. Target Device

RL78/G1D and R7FS3A77C3A01CFB

3. Contents

Folder Name	Description
Firmware	
\Packs	Custom BSP pack for ITMM board
\RL78G1D_HexFiles	VUART Profile Modem configuration hex file that needs to be loaded on RL78/G1D BLE Module
\RL78G1D_VUART_Profile	Source code for generating VUART Profile hex files. Also contains Bluetooth Developer Studio project
\ROMA_Custom_BSP	Synergy Project used for generating custom BSP
\Synergy_Project	Synergy Project for ITMM \src \COM: BLE interfacing and Communication protocol source files \Common: Common includes used across project \DeviceDrivers: Device driver code for BMC150 Accelerometer EPD Module ENS210 Temperature and Humidity sensor LEDs User Buttons MAX17055 Fuel Gauge MS5637 Atmospheric Pressure Sensor N25Q - 16MB NOR Flash memory

	PA6H - GPS Module \MEM: Non-volatile memory functionality related files \SYS: System time update and read functionality configuration.xml: Synergy configuration file ROMA_TargetBoard.pincfg: Pin configuration file for ITMM board Thread entry source files for the following threads Communication Thread Impact Monitoring Thread Periodic Monitoring Thread Monitor and Log Thread VUART Thread rBEL Serial Communication Thread
\Bin	cratus_roma_fw_synergy.hex: Hex file for programming Synergy microcontroller rBLE_Mdm_VUART.hex: Hex file for programming RL78/G1D microcontroller roma_program_synergy.jlink: JLink script for programming Synergy microcontroller roma_program_synergy.bat: Batch file for programming Synergy microcontroller \ROMA_BLE_Flash_Program ROMA_BLE_Flash_Program.rpj: RL78/G1D Flash programming project file
Hardware	
\Fab-Assembly Files	Fabrication and assembly files sent out to get the boards done
\ROMA Design Files	Altium design files
ROMA Schematics.pdf	PDF version of schematics and PCB Layout
Smartphone_Application	
\ROMA	\ROMA : Xamarin Forms source files \ROMA.Android: Resources needed for Android platform \ROMA.iOS: Resources needed for iOS platform
ROMA.sln	Visual Studio Solution file for the project

4. System Requirements

4.1 Hardware Requirements

The following equipment is needed to program and demonstrate operation of the ITMM device

- 1x PC running Microsoft Windows 7 or Windows 10
- 1x Android 7.0+ device

- 1x ITMM hardware
- 1x E1 Debugger (for RL78/G1D only)

4.2 Software requirements

The following software should be installed on to personal and mobile computing platforms as instructed by the respective installation manuals:

- e2 studio (5.4.0.018 or higher)
- Synergy Software Package (v1.3.3) i.e. SSP
- GNU Tools for ARM Embedded Processors 4.9.3 20150529 (release)
- Segger J-Link Debugger Tools (Installed to default location C: Files (x86))
- ITMM Project Sources for Synergy Project
- RL78/G1D BLE Stack (v 1.21) and Flash Libraries
- Bluetooth Developer Studio and RL78/G1D plugins
- Renesas ITMM Mobile application APK installed on to a mobile platform

5. Out-of-Box Experience

The ITMM reference design should be programmed upon receipt. However, you may follow the instructions below to re-program the devices. The reference design has two parts (R7FS3A77C Synergy microcontroller and RL78/G1D BLE microcontroller) that need to be programmed and both have different procedures. Following subsections outline the procedure.

5.1 Reprogramming the S3A7 Microcontroller

1. Connection setup
    a. Establish connection between J-Link LITE programmer and the SWD program/debug port K2/K3 on the reference design
2. Open roma_program_synergy.bat located in Bin folder
    a. Edit path to JLink.exe tool. By default it is assumed as "C:\Program Files\SEGGER\JLink_V614b\JLink.exe"
3. Execute roma_program_synergy.bat. It should program the device. Output after successful programming is given here for reference

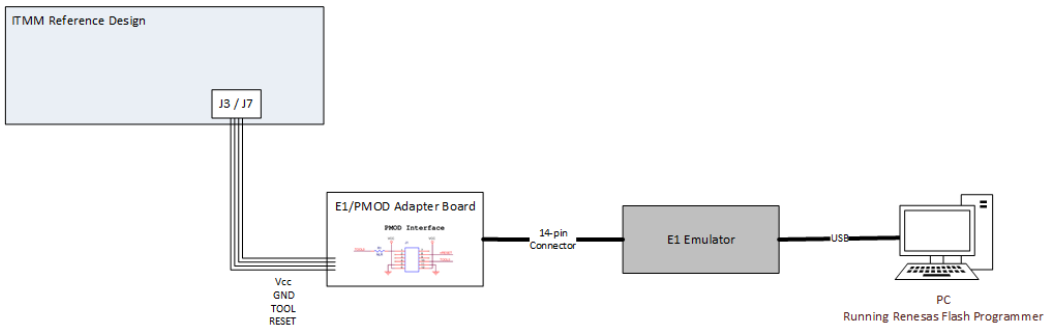
```
---------------------------------------------------------------------------
SEGGER J-Link Commander V6.14b (Compiled Mar  9 2017 08:46:23)
DLL version V6.14b, compiled Mar  9 2017 08:46:04


Script file read successfully.
Processing script file...

J-Link connection not established yet but required for command.
Connecting to J-Link via USB...O.K.
Firmware: J-Link Lite-Cortex-M V8 compiled Sep 15 2016 12:05:01
Hardware version: V8.00
S/N: 518112829
License(s): GDB
VTref = 3.313V

Selecting SWD as current target interface.
```

```
Selecting 3000 kHz as target interface speed


Target connection not established yet but required for command.
Device "R7FS3A77C" selected.


Found SWD-DP with ID 0x5BA02477
Found SWD-DP with ID 0x5BA02477
AP-IDR: 0x24770011, Type: AHB-AP
AHB-AP ROM: 0xE00FF000 (Base addr. of first ROM table)
Found Cortex-M4 r0p1, Little endian.
FPUnit: 6 code (BP) slots and 2 literal slots
CoreSight components:
ROMTbl 0 @ E00FF000
ROMTbl 0 [0]: FFF0F000, CID: B105E00D, PID: 000BB00C SCS
ROMTbl 0 [1]: FFF02000, CID: B105E00D, PID: 003BB002 DWT
ROMTbl 0 [2]: FFF03000, CID: B105E00D, PID: 002BB003 FPB
ROMTbl 0 [3]: FFF01000, CID: B105E00D, PID: 003BB001 ITM
ROMTbl 0 [4]: FFF41000, CID: B105900D, PID: 000BB9A1 TPIU
ROMTbl 0 [5]: FFF42000, CID: B105900D, PID: 000BB925 ETM
ROMTbl 0 [6]: FFF43000, CID: B105900D, PID: 002BB908 CSTF
ROMTbl 0 [7]: FFF44000, CID: B105900D, PID: 001BB961 TMC
ROMTbl 0 [8]: FFF45000, CID: B105F00D, PID: 001BB101 TSG
Cortex-M4 identified.
Reset delay: 200 ms
Reset type NORMAL: Resets core & peripherals via SYSRESETREQ & VECTRESET bit.

PC = FFFFFFFE, CycleCnt = 00000000
R0 = 2000093C, R1 = 40044200, R2 = 00000000, R3 = 00000000
R4 = 2000093C, R5 = 2000095C, R6 = 2000095C, R7 = 200132D8
R8 = 00000003, R9 = 00000000, R10= 20015790, R11= 00000000
R12= 20015AD8
SP(R13)= FFFFFFFC, MSP= FFFFFFFC, PSP= 20015AD8, R14(LR) = FFFFFFFF
XPSR = 01000000: APSR = nzcvq, EPSR = 01000000, IPSR = 000 (NoException)
CFBP = 00000000, CONTROL = 00, FAULTMASK = 00, BASEPRI = 00, PRIMASK = 00
FPU regs: FPU not enabled / not implemented on connected CPU.

Downloading file [cratus_roma_fw_synergy.hex]...

**************************
WARNING: CPU is running at low speed (8000 kHz).
**************************

J-Link: Flash download: Flash programming performed for 2 ranges (86016 bytes)
J-Link: Flash download: Total time needed: 1.580s (Prepare: 0.158s, Compare:
0.045s, Erase: 0.024s, Program: 1.312s, Verify: 0.020s, Restore: 0.018s)
O.K.
--------------------------------------------------------------------------------
```

5.2 Reprogramming the RL78/G1D Microcontroller

1. Connection setup

    a. Hardware setup for programming the RL78/G1D microcontroller is as shown in the diagram below



2. Open Renesas Flash Programmer V3.0.3 and open the flash programming project file ROMA_BLE_Flash_Program.rpj located in Bin folder

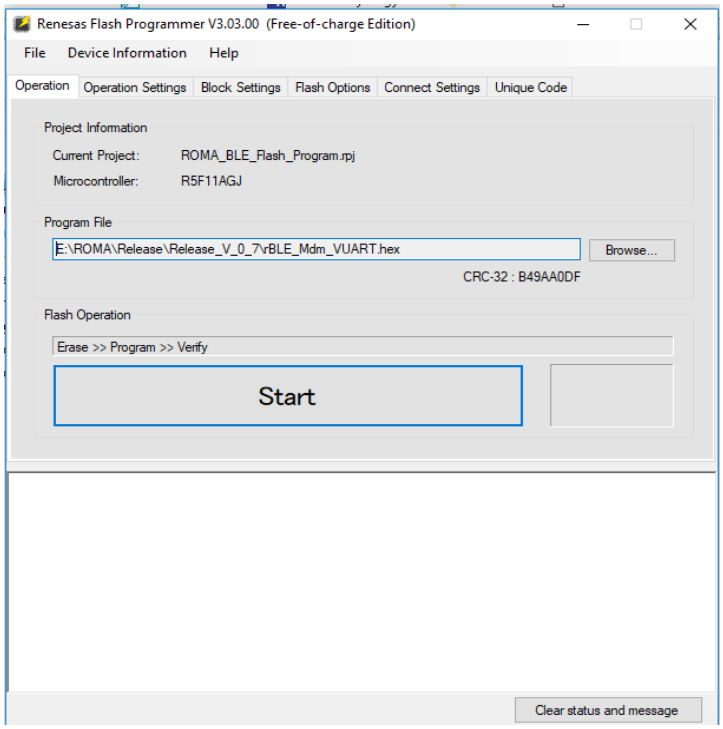


Figure 1 Renesas Flash Programmer Screen

3. Choose rBLE_Mdm_VUART.hex file located in Bin folder for programming
4. Start Programming by clicking on the START button. Below screen shots show the progress and successful completion of the programming operation

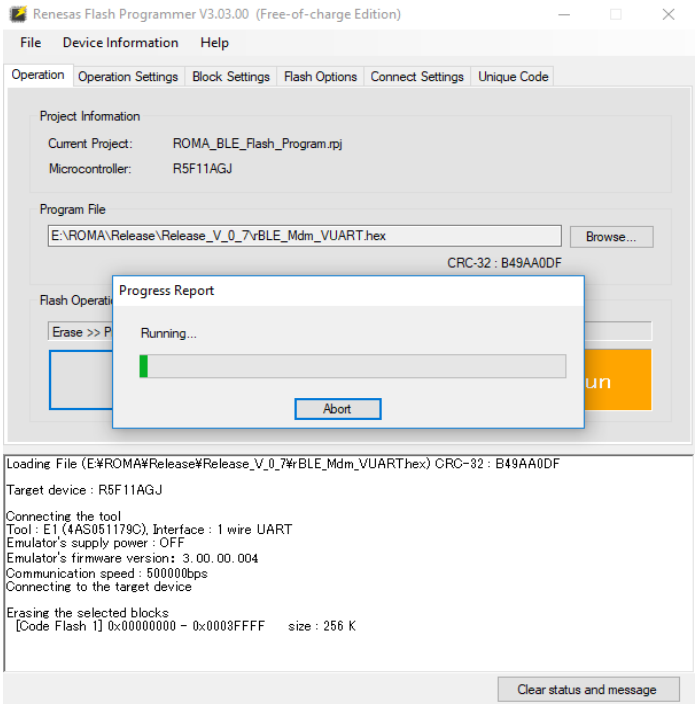


Figure 2 Flash program operation in progress

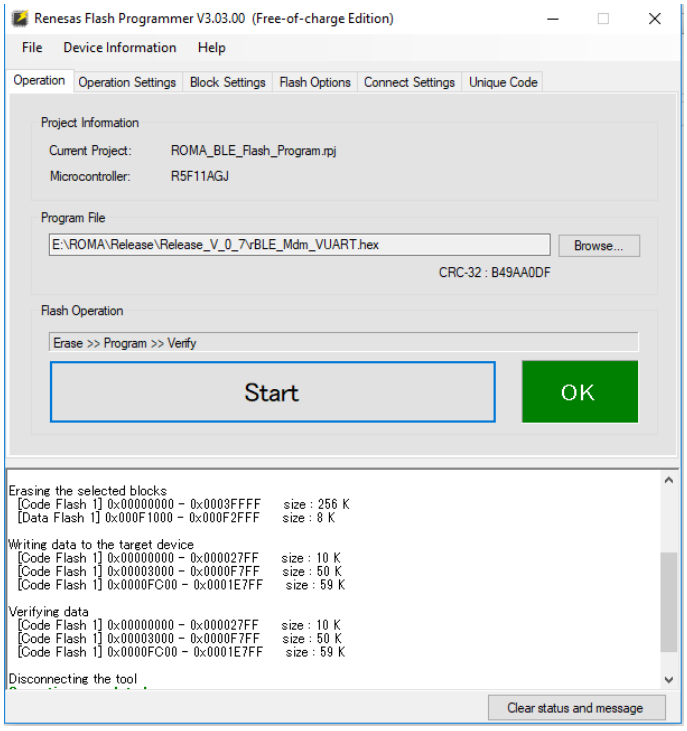


Figure 3 RL78/G1D Successfully programmed

5.3 Mobile Application Installation

Mobile Applications are available for installation on iOS and Android devices at the following locations:

- https://itunes.apple.com/us/app/roma-app/id1357462314?mt=8
- https://play.google.com/store/apps/details?id=com.cratustech.ROMA&hl=en

6. ITMM Reference Application Flow

This section outlines the design methodology used for the firmware on board and provides UML State Machine Diagrams for each of the threads

Design Methodology

Programming of concurrent systems poses several challenges. In order to avoid perils of blocking, following practices have been adopted in the design

1. Don't block inside your code
    a. Communicate and synchronize threads asynchronously via event objects
2. Don't share data or resources among threads
3. Keep data isolated and bound to threads (strict encapsulation)
    a. Structure your threads as "message pumps"

Following the above-mentioned principle of design, ALL the threads of the firmware synchronize through events mechanism. Each of the threads have a finite state machine or 'Spaghetti Code Reducers' of their own. Interaction between these threads take place through EVENT mechanism. Following subsections outline the finite state machines for each of the threads using UML State Machine Diagrams

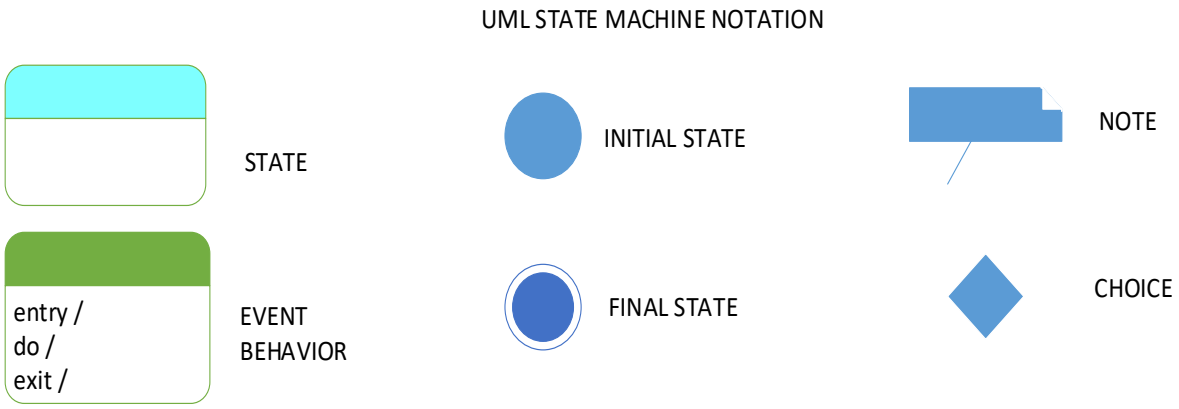


Figure 4 UML STATE MACHINE NOTATION

ITMM Firmware has following threads:

- Communication Thread
- HMI Thread
- Impact Monitoring Thread
- Monitor and Log Thread
- Periodic Monitoring Thread
- Virtual UART (VUART) Thread
- rBLE Serial Communication Thread

6.1 Communication Thread

This thread is responsible for interfacing between BLE Communication and rest of the system. It is responsible for processing data received over BLE and framing the appropriate response back to the App. Communication stack function called from within this thread handles processing of all the commands received over BLE.

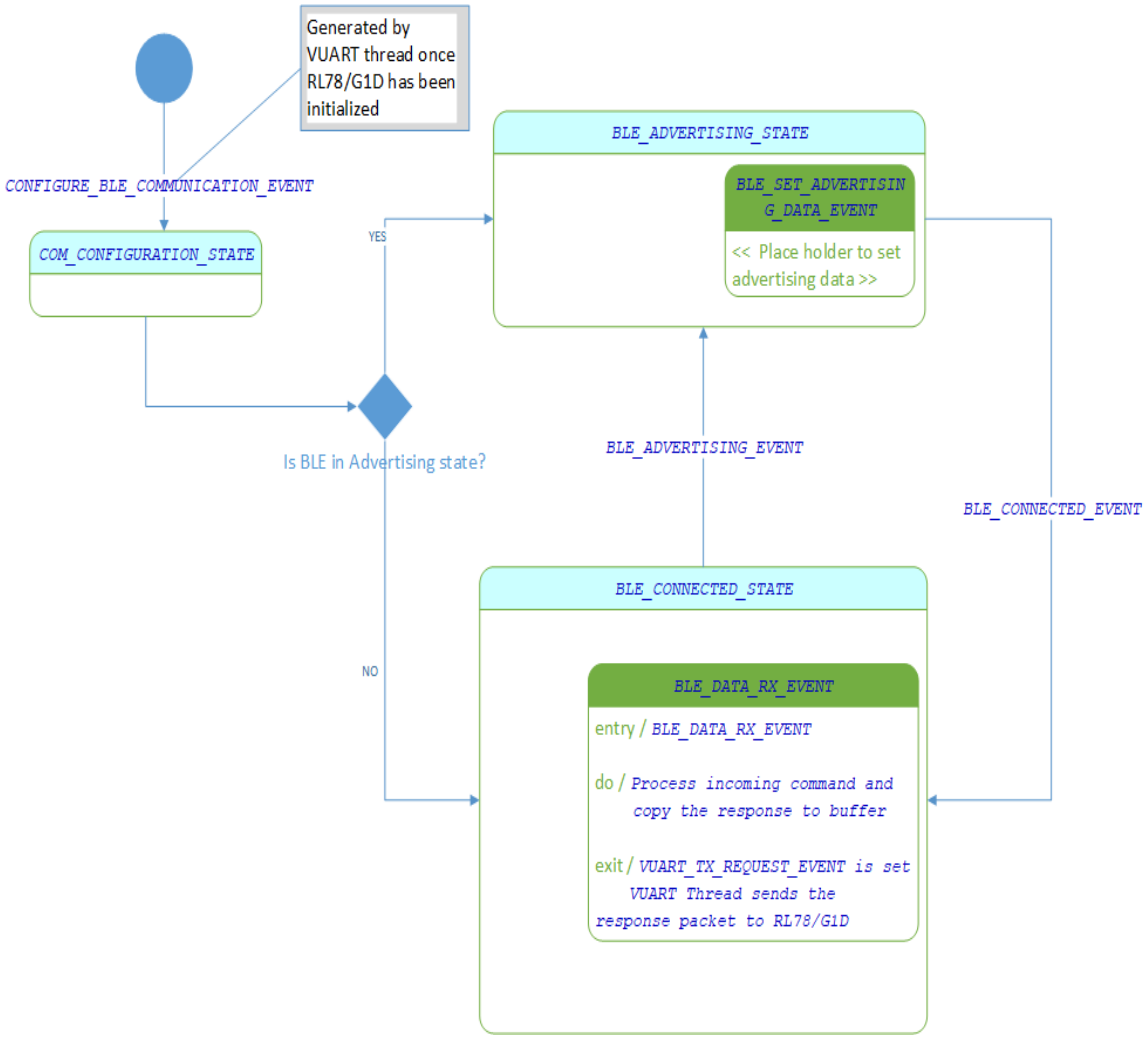


Figure 5 COMMUNICATION THREAD STATE MACHINE

6.2 HMI Thread

This thread is responsible for responding to the actions on user button. It turns on the system on POWER_ON_BUTTON event. While it is in SYSTEM_POWER_ON_STATE handles User's request for

- Toggling the display between Alpha-numeric and barcode display
- Start / Stop data logging operations

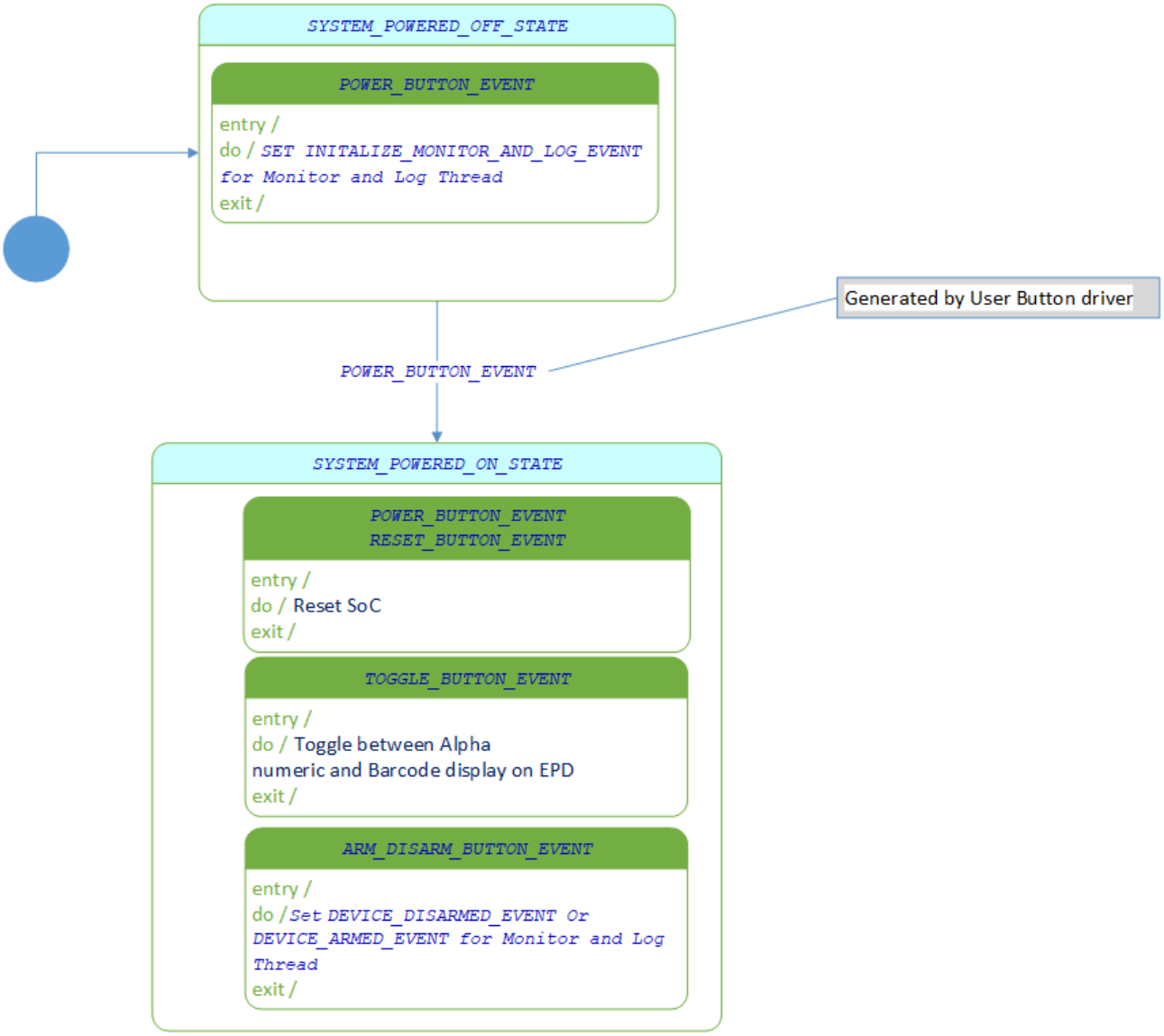


Figure 6 HMI THREAD STATE MACHINE

6.3 Impact Monitoring Thread

This thread is responsible for initializing and configuring the sensor (Accelerometer) to detect shock events. Upon detection of shock event, directs the Monitor and Log Thread to store the event in non-volatile memory.

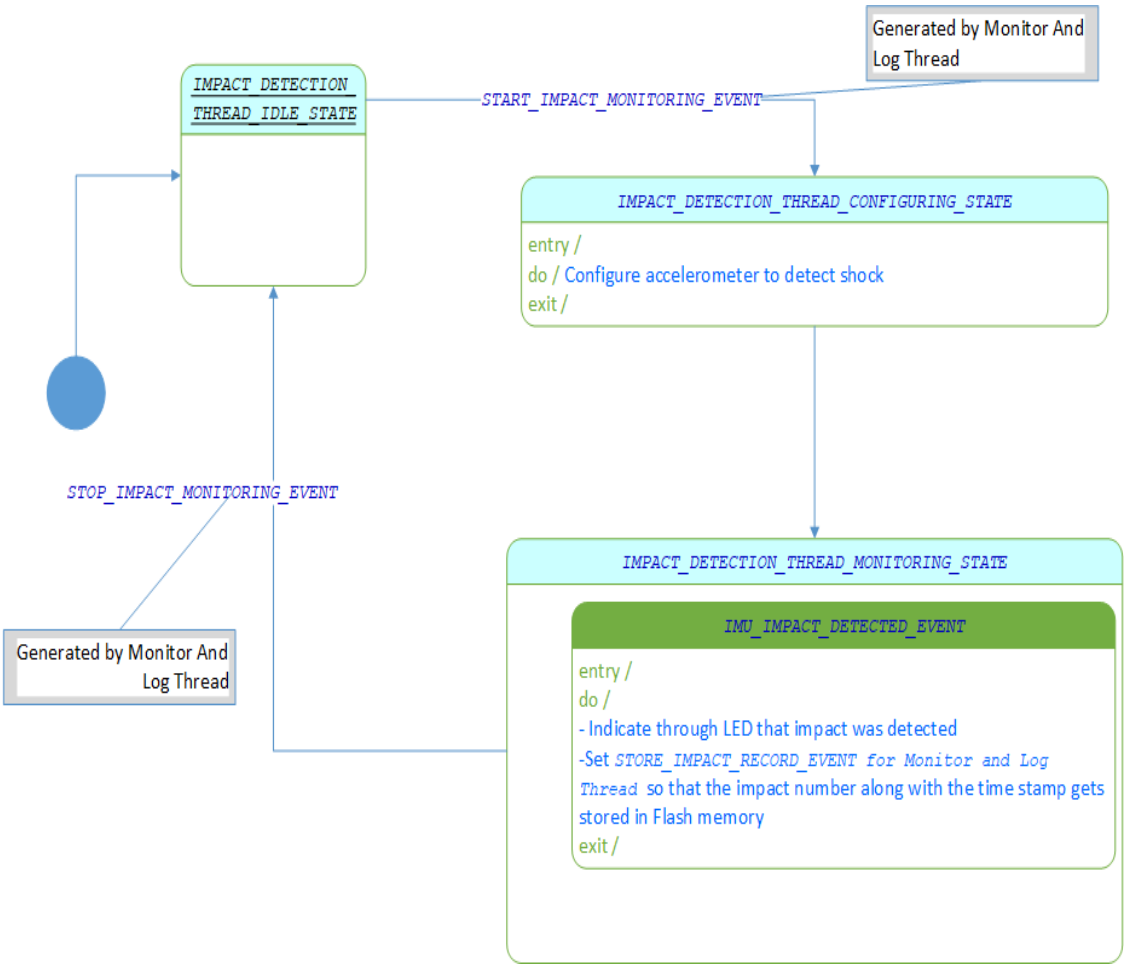


Figure 7 IMPACT MONITORING THREAD STATE MACHINE

6.4 Monitor & Log Thread

This thread is responsible for initiating and stopping logging of data from sensors on board. Upon receipt of command to start logging (either through HMI thread or the BLE) it activates Impact Monitoring Thread and Periodic Monitoring Thread to start reading data from sensors. When data from sensor is available, it stores the data read into non-volatile memory. Upon receipt of command to stop logging, it deactivates Impact Monitoring Thread and Periodic Monitoring Thread.

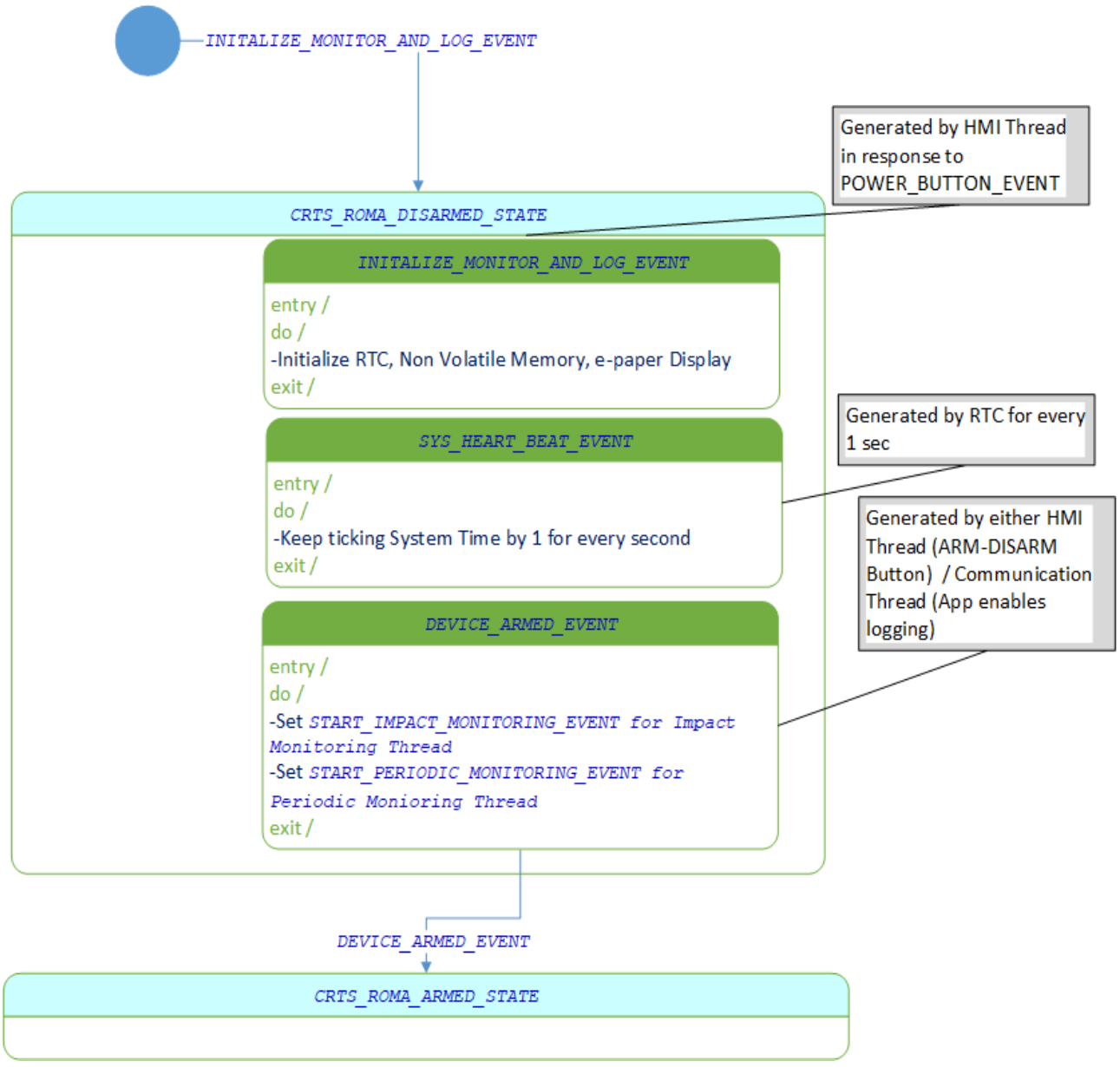


Figure 8 MONITOR AND LOG THREAD STATE MACHINE – DISARMED STATE

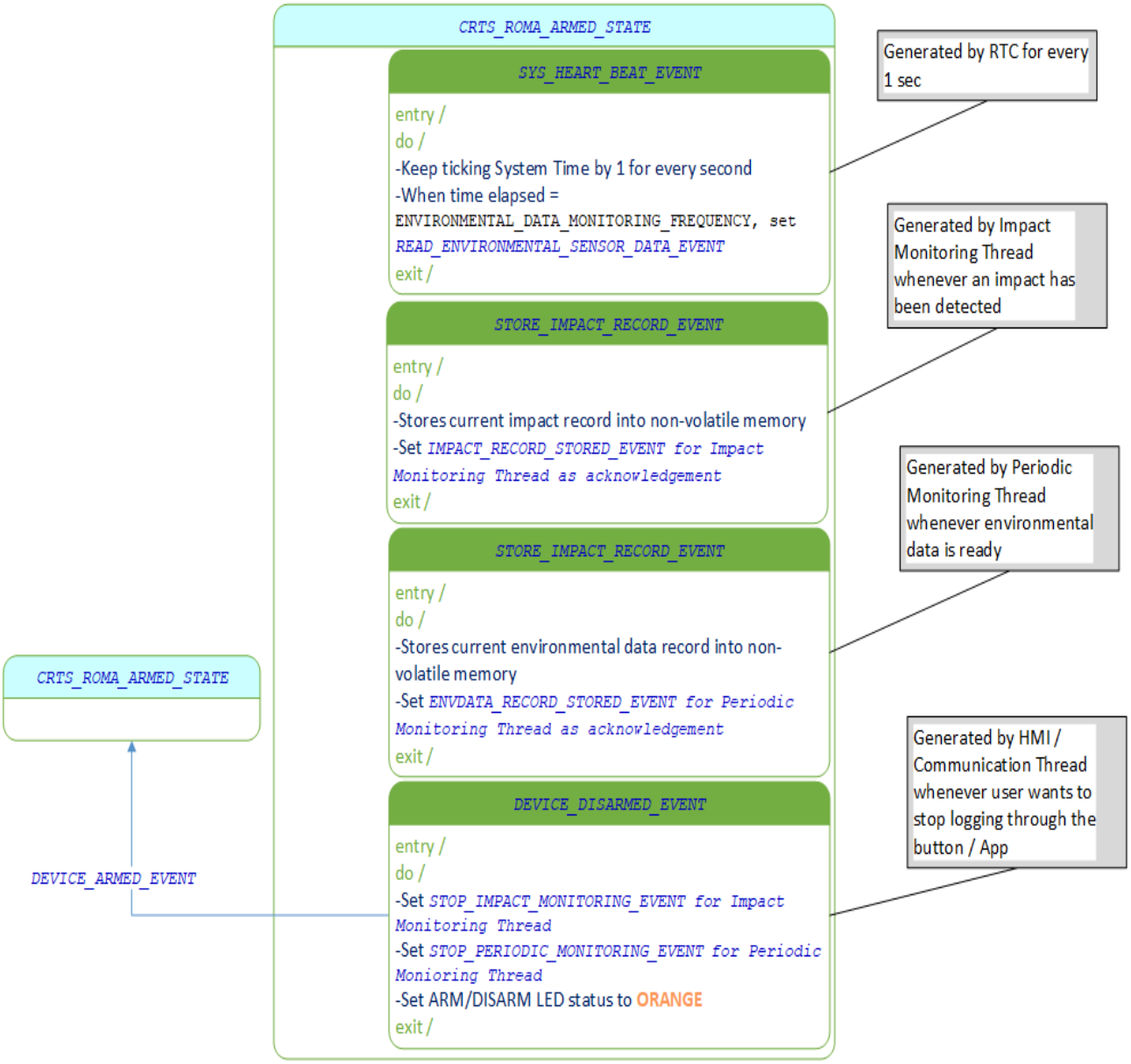


Figure 9 MONITOR AND LOG THREAD STATE MACHINE - ARMED STATE

6.5 Periodic Monitoring Thread

This thread is responsible for reading data from sensors periodically. It is activated / deactivated through Monitor and Log Thread. Temperature and Humidity Sensor, Atmospheric Pressure Sensor, GPS Coordinates, and the fuel gauge value are read periodically when this thread is activated.

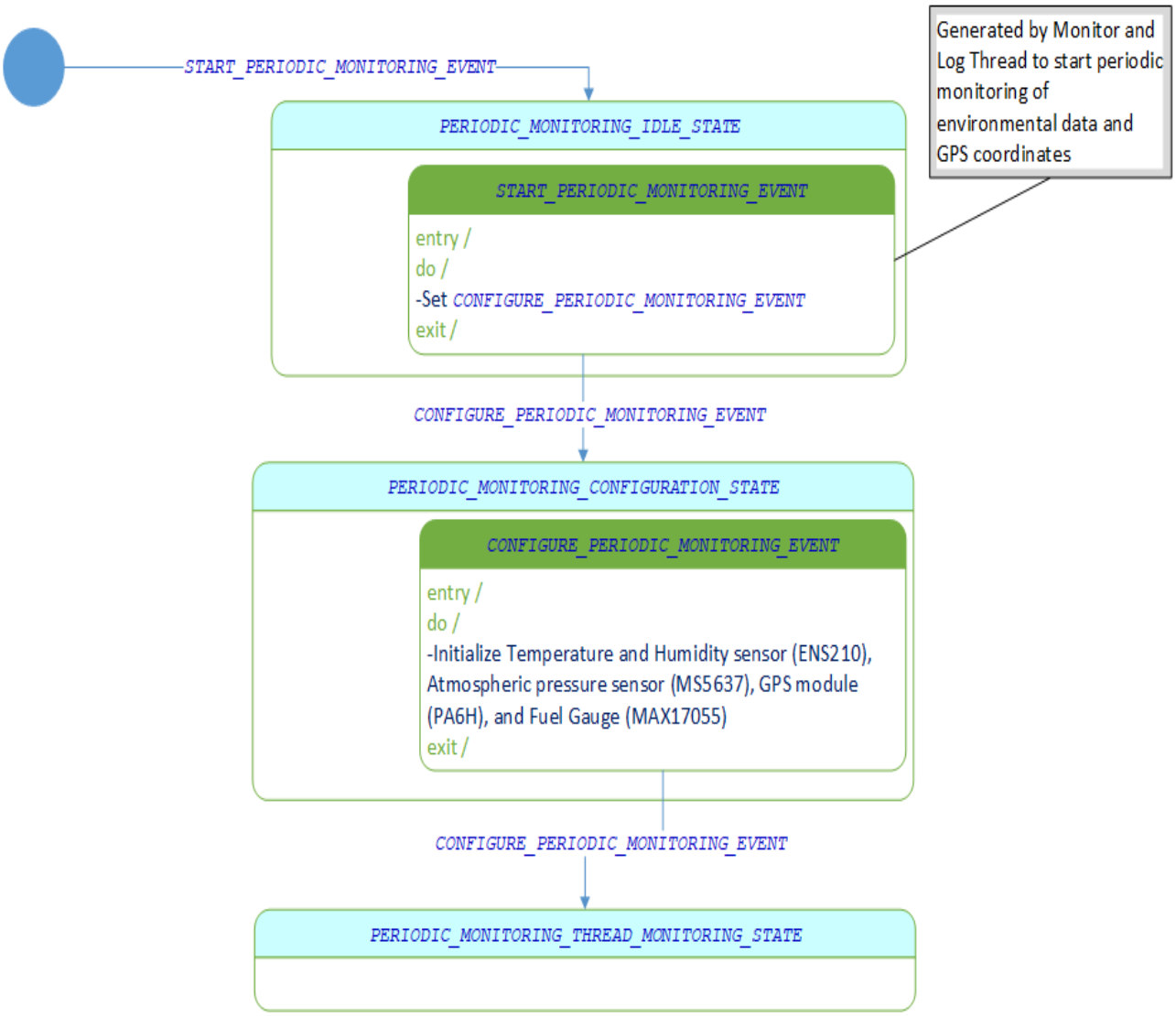


Figure 10 PERIODIC MONITORING THREAD STATE MACHINE – IDLE / CONFIGURE STATE

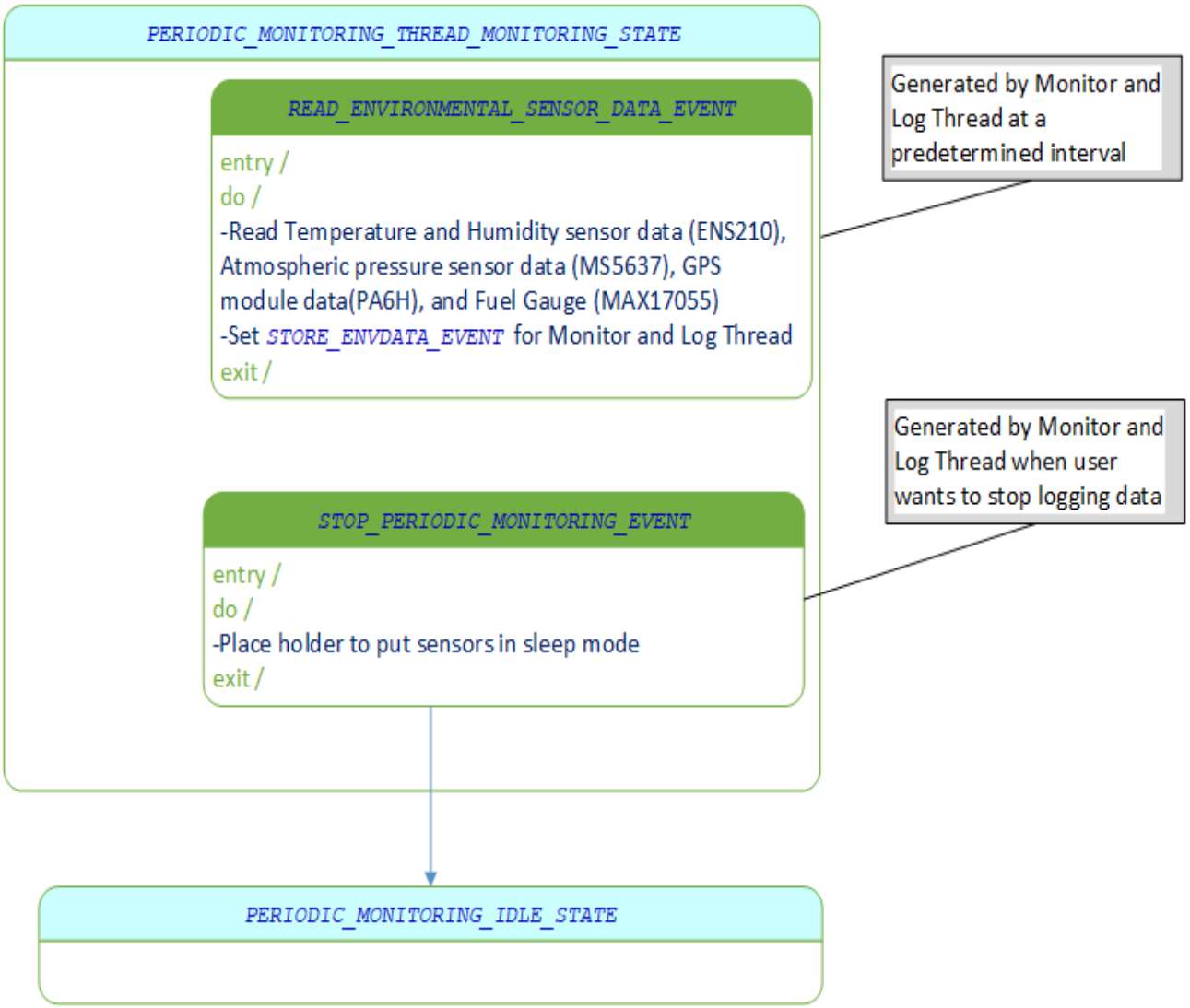


Figure 10 PERIODIC MONITORING THREAD STATE MACHINE-PERIODIC MONITORING STATE

6.6 VUART Thread

This thread is responsible for handling all the events covering Virtual UART Profile. This thread indicates to Communication Thread when a data packet has been received over BLE. It dispatches a framed packet to RL78/G1D when Communication Thread has data to send. It interfaces with rBLE Serial Communication Thread to handle the transactions over UART between Synergy microcontroller and RL78/G1D BLE module.

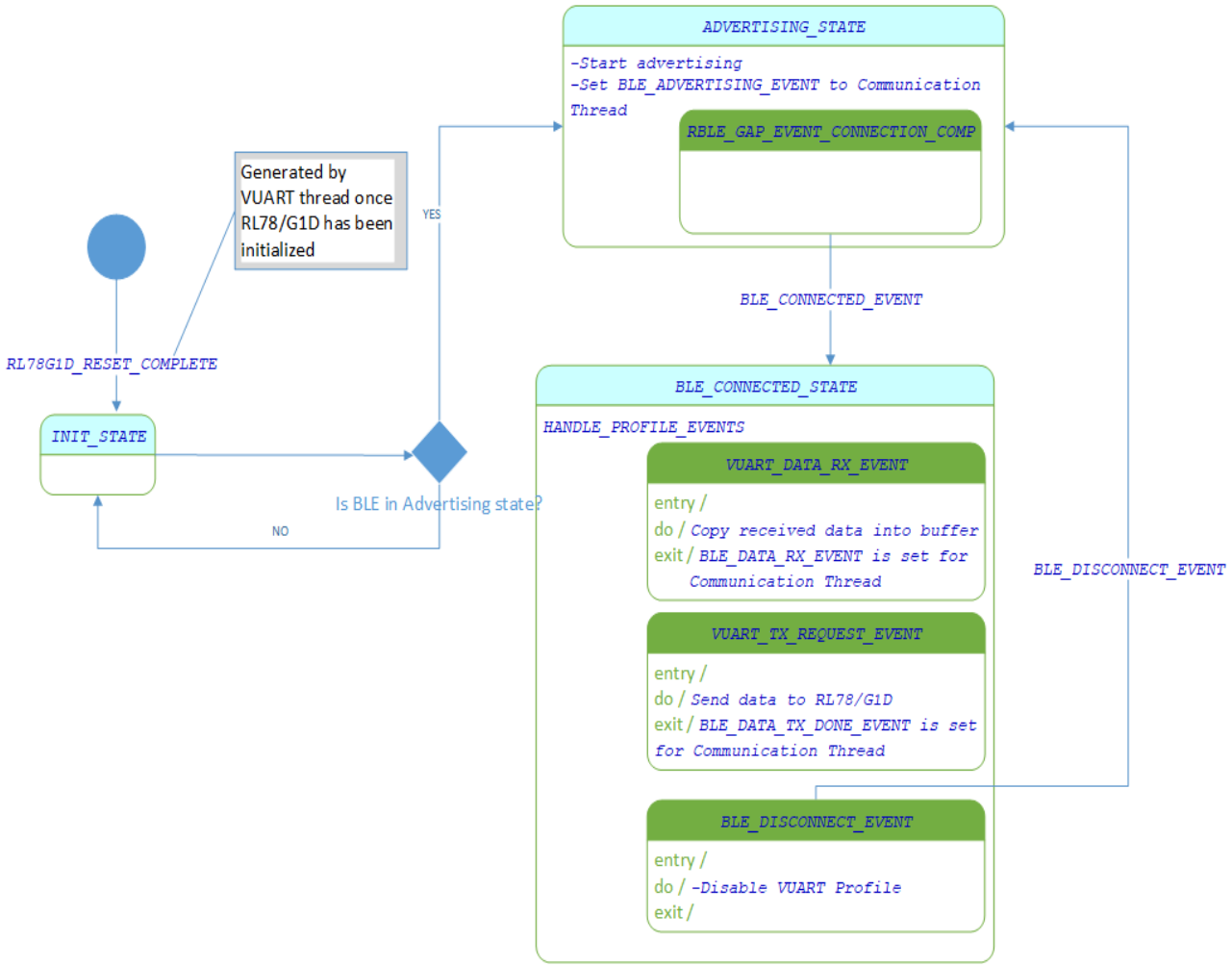


Figure 11 Virtual UART THREAD STATE MACHINE

6.7 rBLE Serial Communication Thread

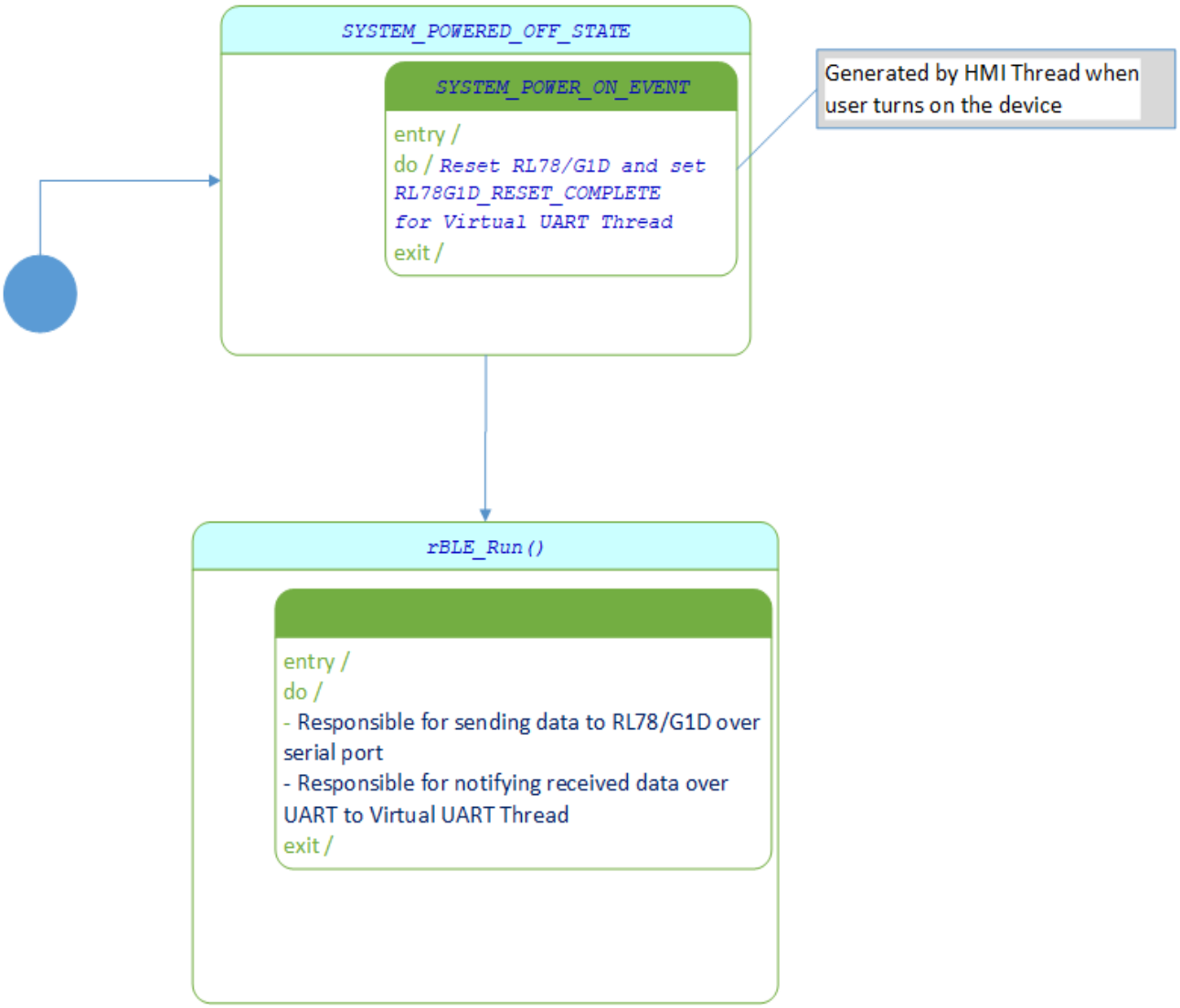


Figure 12 rBLE Serial Communication Thread State Machine

7. Next Steps

With an understanding of the Reference Application flow, it is possible to import, build, and modify the application to match actual product needs.

7.1 Importing the Synergy Project

Import the ITMM Solutions project using the procedure specified in the document R11AN0023 available via the Renesas website.

7.2 Building the Synergy Project

ITMM Project makes use of Custom BSP package. Same can be found in 'Packs' directory of the archive. CRATUS.ROMA_Rev2_BSP.1.3.0.pack needs to be copied to C:\Renesas\e2_studio\internal\projectgen\arm\Packs directory, assuming that e2_studio was installed in C:\

Sample Output from the build is a given below:

```
------------------------------------------------------------------------------

'Building target: cratus_roma_fw_v3.elf'
'Invoking: Cross ARM C Linker'
arm-none-eabi-gcc @"cratus_roma_fw_v3.elf.in"
'Finished building target: cratus_roma_fw_v3.elf'
' '
'Invoking: Cross ARM GNU Create Flash Image'
arm-none-eabi-objcopy -O srec "cratus_roma_fw_v3.elf"  "cratus_roma_fw_v3.srec"
'Invoking: Cross ARM GNU Print Size'
arm-none-eabi-size --format=berkeley "cratus_roma_fw_v3.elf"
   text        data         bss         dec         hex     filename
  87440         603       93488      181531       2c51b
      cratus_roma_fw_v3.elf
'Finished building: cratus_roma_fw_v3.srec'
'Finished building: cratus_roma_fw_v3.siz'
' '
' '

15:50:42 Build Finished. 0 errors, 2 warnings. (took 30s.67ms)
------------------------------------------------------------------------------
```

8. Appendix

8.1 Identified Hardware Issues

- Do not connect/disconnect Electrophoretic Display (EPD) module while the device is powered on. Connect or disconnect EPD display only when the system is NOT powered through battery or USB.

8.2 Sample Programming output

```
---------------------------------------------------------------------------
SEGGER J-Link Commander V6.14b (Compiled Mar  9 2017 08:46:23)
DLL version V6.14b, compiled Mar  9 2017 08:46:04


Script file read successfully.
Processing script file...

J-Link connection not established yet but required for command.
Connecting to J-Link via USB...O.K.
Firmware: J-Link Lite-Cortex-M V8 compiled Sep 15 2016 12:05:01
Hardware version: V8.00
S/N: 518112829
License(s): GDB
VTref = 3.313V

Selecting SWD as current target interface.

Selecting 3000 kHz as target interface speed


Target connection not established yet but required for command.
Device "R7FS3A77C" selected.


Found SWD-DP with ID 0x5BA02477
Found SWD-DP with ID 0x5BA02477
AP-IDR: 0x24770011, Type: AHB-AP
AHB-AP ROM: 0xE00FF000 (Base addr. of first ROM table)
Found Cortex-M4 r0p1, Little endian.
FPUnit: 6 code (BP) slots and 2 literal slots
CoreSight components:
ROMTbl 0 @ E00FF000
ROMTbl 0 [0]: FFF0F000, CID: B105E00D, PID: 000BB00C SCS
ROMTbl 0 [1]: FFF02000, CID: B105E00D, PID: 003BB002 DWT
ROMTbl 0 [2]: FFF03000, CID: B105E00D, PID: 002BB003 FPB
ROMTbl 0 [3]: FFF01000, CID: B105E00D, PID: 003BB001 ITM
ROMTbl 0 [4]: FFF41000, CID: B105900D, PID: 000BB9A1 TPIU
ROMTbl 0 [5]: FFF42000, CID: B105900D, PID: 000BB925 ETM
ROMTbl 0 [6]: FFF43000, CID: B105900D, PID: 002BB908 CSTF
ROMTbl 0 [7]: FFF44000, CID: B105900D, PID: 001BB961 TMC
ROMTbl 0 [8]: FFF45000, CID: B105F00D, PID: 001BB101 TSG
Cortex-M4 identified.
Reset delay: 200 ms
Reset type NORMAL: Resets core & peripherals via SYSRESETREQ & VECTRESET bit.

PC = FFFFFFFE, CycleCnt = 00000000
R0 = 2000093C, R1 = 40044200, R2 = 00000000, R3 = 00000000
R4 = 2000093C, R5 = 2000095C, R6 = 2000095C, R7 = 200132D8
R8 = 00000003, R9 = 00000000, R10= 20015790, R11= 00000000
R12= 20015AD8
```

```
SP(R13)= FFFFFFFC, MSP= FFFFFFFC, PSP= 20015AD8, R14(LR) = FFFFFFFF
XPSR = 01000000: APSR = nzcvq, EPSR = 01000000, IPSR = 000 (NoException)
CFBP = 00000000, CONTROL = 00, FAULTMASK = 00, BASEPRI = 00, PRIMASK = 00
FPU regs: FPU not enabled / not implemented on connected CPU.

Downloading file [cratus_roma_fw_synergy.hex]...

*************************
WARNING: CPU is running at low speed (8000 kHz).
*************************

J-Link: Flash download: Flash programming performed for 2 ranges (86016 bytes)
J-Link: Flash download: Total time needed: 1.580s (Prepare: 0.158s, Compare:
0.045s, Erase: 0.024s, Program: 1.312s, Verify: 0.020s, Restore: 0.018s)
O.K.
--------------------------------------------------------------------------------
```

8.3 Acknowledgments

We acknowledge the use of **nRFConnect** Mobile application which has been instrumental in the design and development of the non-commercial Renesas Personal Medical Adherence reference design.

Website and Support

Renesas Electronics Website
http://www.renesas.com/

Renesas Electronics In-Transit Medication Management Website

https://www.renesas.com/us/en/solutions/healthcare/itmmsolution.html

Renesas Electronics Healthcare Applications Website
https://www.renesas.com/us/en/solutions/healthcare.html

Inquiries
http://www.renesas.com/contact/

Revision History

		Description	
Rev.	**Date**	**Page**	**Summary**
1.00	September11,2018		Release

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins

   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.

   — The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on

   The state of the product is undefined at the moment when power is supplied.

   — The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses

   Access to reserved addresses is prohibited.

   — The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals

   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.

   — When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products

   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.

   — The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
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5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
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