ISL6731AEVAL2Z and ISL6731BEVAL2Z: High Performance Boost CCM PFC Front End for Server Power Applications

Introduction
This application note describes the design and implementation of a 390V, 750W, Continuous Conduction Mode (CCM) Boost PFC converter using either ISL6731A or ISL6731B. The converter exhibits high power factor, low THD and high conversion efficiency. The ISL6731A, ISL6731B are voltage mode power factor correction (PFC) controllers designed to drive cost-effective high performance converters to meet the tight input line harmonic requirements. The IC can be ISL6731A (124kHz) or ISL6731B (64kHz).

Application
PFC front end for server, data center, telecom, industrial and infrastructure power applications.

Key Features
• Universal input: 90V~265VAC
• Adaptive control to achieve extremely low THD and high PF without DSP.
• Compact implementation

References
• “ISL6731A, ISL6731B” datasheet

Design Specifications
• Input Voltage, Vin: 90V - 265VAC
• Output Voltage, V0: 390VDC
• Output Current, I0: 1.92A (750W)
• Switching Frequency: ISL6731A (124kHz) or ISL6731B (64kHz)
• Efficiency: Full Load, 93% @ 115V; 97% @ 230V
• PF: Full Load, 0.99
• THD: Full Load, 2%
• Board Dimension: 121×96×38 mm³(L×W×H)

Test Setup
• See the test set-up in Figure 9 on page 7
• A 12V DC FAN is needed to cool the heat-sink during the test, especially at full load with low line 90~140VAC input!

Ordering Information

<table>
<thead>
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<th>PART NUMBER</th>
<th>DESCRIPTION</th>
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<tr>
<td>ISL6731AEVAL2Z</td>
<td>750W Boost CCM PFC, 124KHz</td>
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<tr>
<td>ISL6731BEVAL2Z</td>
<td>750W Boost CCM PFC, 64KHz</td>
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FIGURE 1. SIMPLIFIED SCHEMATIC
Component Selection Guidelines

A 750W, universal input, PFC converter design is provided for demonstration. The design method is for a continuous current mode power factor correction boost converter with the ISL6731B. The switching frequency is 64kHz.

Table 1 shows the design parameters.

### Table 1. Converter Design Parameters

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<tr>
<th>PARAMETER</th>
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<th>TYP</th>
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<td>Efficiency</td>
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<td>92</td>
<td>%</td>
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#### BOOST INDUCTOR SELECTION

First, calculate the maximum input RMS current, I\text{INMAX}.

\[
I_{\text{INMAX}} = \frac{P_{\text{OMAX}}}{\eta \cdot V_{\text{RMSmin}}} \quad (\text{EQ. 1})
\]

Where \( \eta \) is the converter efficiency at \( V_{\text{RMSmin}} \). PF is the power factor at \( V_{\text{RMSmin}} \).

Assuming the current is sinusoidal and the peak-to-peak ripple at line is 40%.

The boost inductor, \( L_{\text{BST}} \), is given by the following equation:

\[
L_{\text{BST}} \geq \frac{\sqrt{2} \cdot V_{\text{RMSmin}}}{0.4 \cdot F_{\text{sw}} \cdot \sqrt{2} \cdot I_{\text{INMAX}} \cdot \left(1 - \frac{\sqrt{2} \cdot V_{\text{RMSmin}}}{V_{\text{OUT}}}\right)} \quad (\text{EQ. 3})
\]

An 850µH inductor was selected. The peak current of the inductor is the sum of the average peak inductor current and half of the peak-to-peak ripple current. Select and design the boost inductor as given by Equation 3. The ISL6731A and ISL6731B provide a peak current limit function that can prevent the boost inductor saturation. Assuming 25% margin is given to the OCP threshold, select and design the boost inductor with saturation current given by Equation 5 with 25% margin.

\[
I_{\text{LPeak}} = \sqrt{2} \cdot I_{\text{INMAX}} + \frac{1}{2} \cdot \Delta \eta
\]

\[
I_{\text{LPeak}} = \sqrt{2} \cdot 9.06A + (3.152A) = 14.4A
\]

#### INPUT RECTIFIER

The maximum average input current is calculated:

\[
I_{\text{INAVE(max)}} = \frac{2 \cdot \sqrt{2} \cdot I_{\text{INMAX}}}{\pi} \quad (\text{EQ. 7})
\]

Select the bridge diode using Equation 9 and sufficient reverse breakdown voltage. Assuming the forward voltage, \( V_{\text{F,BR}} \), is 1.1V across each rectifier diode. The power loss of the rectifier bridge can be calculated:

\[
P_{\text{BR}} = 2 \cdot V_{\text{F,BR}} \cdot I_{\text{INAVE(max)}} \quad (\text{EQ. 9})
\]

\[
P_{\text{BR}} = 2 \cdot 1.1V \cdot 8.2A = 17.9W
\]

#### INPUT CAPACITOR SELECTION

Refer to the “Recommended Filtering Capacitor” table, in the ISL6731A, ISL6731B datasheet for the recommended input filter capacitor value.

\[
C_{\text{F1}} = 750W \cdot 0.22 \cdot 100 = 1.65\mu F
\]

The definition of \( C_{\text{F1}} \) is on the block diagram in the ISL6731A, ISL6731B datasheet.

This is the recommended capacitor used after the diode bridge. For better power factor, less capacitance can be used. To lower the input filter inductor size, more capacitance can be used.

One 0.68µF capacitor is used for \( C_{\text{F1}} \).

#### BOOST DIODE SELECTION

The boost diode loss is determined by the diode forward voltage drop, \( V_{\text{F}} \) and the output average current. The maximum output current is:

\[
I_{\text{OUT(max)}} = \frac{P_{\text{OMAX}}}{V_{\text{OUT}}} \quad (\text{EQ. 12})
\]

\[
I_{\text{OUT(max)}} = \frac{750W}{390V} = 1.923A
\]

The forward power loss on the diode is:

\[
P_{\text{FD}} = I_{\text{OUT(max)}} \cdot V_{\text{F}} \quad (\text{EQ. 14})
\]

\[
P_{\text{FD}} = 1.923A \cdot 1.3V = 2.5W
\]

The reverse recovery loss on the diode can be calculated. The \( Q_{\text{RR}} \) is found from the diode datasheet. \( Q_{\text{RR}} = 12nC \).

\[
P_{\text{RRD}} = \frac{1}{4} \cdot Q_{\text{RR}} \cdot V_{\text{OUT}} \cdot F_{\text{sw}} \quad (\text{EQ. 16})
\]

\[
P_{\text{RRD}} = \frac{1}{4} \cdot 12nC \cdot 390V \cdot 64kHz = 0.075W
\]

The total power loss on the diode is:

\[
P_{\text{D}} = P_{\text{FD}} + P_{\text{RRD}} = (2.5 + 0.075)W = 2.575W
\]

#### MOSFET POWER DISSIPATION

The power dissipation on the MOSFET is from two different types of losses; the conduction loss and the switching loss.
For the MOSFET, the worst case is at minimum line input voltage.

First, the drain to source RMS current is calculated:

\[
I_{DS(max)} = \frac{I_{INMAX}}{\sqrt{1 - \frac{8}{3}\frac{V_{\text{RMSmin}}}{\sqrt{V_{\text{OUT}}}}} (\text{EQ. 19})
\]

\[
I_{DS(max)} = \frac{9.06A}{\sqrt{1 - \frac{8}{3}\frac{90V}{390V}}} = 7.7A (\text{EQ. 20})
\]

The MOSFET, SPP20N60C3 is selected.

\[
P_{\text{COND}} = \frac{1}{2}I_{DS(max)} \cdot R_{DS(on)} (\text{EQ. 21})
\]

\[
P_{\text{COND}} = 7.7A^2 \cdot 0.188 \Omega = 11.12W (\text{EQ. 22})
\]

The switching loss of the MOSFET consists of three parts: the turn-on loss, the turn-off loss and the C\text{OSS} loss.

From the MOSFET datasheet, the typical switching losses curves are provided.

\[E_{ON} = 0.022mJ, E_{OFF} = 0.029mJ.\]

The switching loss due to transition is calculated:

\[
P_{SW} = (E_{ON} + E_{OFF}) \cdot F_{sw} (\text{EQ. 23})
\]

\[
P_{SW} = (0.022mJ + 0.029mJ) \cdot 64kHz = 3.26W (\text{EQ. 24})
\]

The loss caused by C\text{OSS} can be estimated as:

\[
P_{\text{OSS}} = \frac{2}{3}C_{\text{OSS}} \cdot V_{\text{OUT}}^2 \cdot F_{sw} (\text{EQ. 25})
\]

From the datasheet, the C\text{OSS} is 61pF at 390V.

\[
P_{\text{OSS}} = \frac{2}{3}61pF \cdot 390V^2 \cdot 64kHz = 0.394W (\text{EQ. 26})
\]

**THE TOTAL LOSS ON THE MOSFET**

\[
P_{\text{COND}} + P_{SW} + P_{\text{OSS}} = 11.12W + 3.26W + 0.394W = 14.78W (\text{EQ. 27})
\]

**OUTPUT CAPACITOR SELECTION**

The output capacitor, C\text{O}, is required to hold the output above 300V during one line cycle. For capacitors with 10% tolerance, the tolerance should be taken into consideration. Thus, the output capacitance should be greater than:

\[
C_{O} \geq \frac{2 \cdot T_{\text{HOLD}} \cdot P_{\text{OMAX}}}{V_{\text{OUT}}^2 - V_{\text{HOLD}}^2} \cdot \frac{1}{1 - 0.1} (\text{EQ. 28})
\]

\[
C_{O} \geq \frac{2 \cdot 20ms \cdot 750W}{(390V)^2 - (300V)^2} \cdot 1.25 = 537\mu F (\text{EQ. 29})
\]

Calculate the ripple RMS current through the capacitor:

\[
I_{\text{CORMS}(\text{max})} = I_{\text{OUT}(\text{max})} \sqrt{1 - \frac{8}{3}\frac{V_{\text{RMSmin}}}{\sqrt{V_{\text{OUT}}}}} (\text{EQ. 30})
\]

\[
I_{\text{CORMS}(\text{max})} = \frac{1.923A}{\sqrt{1 - \frac{8}{3}\frac{390V}{90V}}} = 3.942A (\text{EQ. 31})
\]

Select the proper capacitor according to the hold time and ripple RMS current requirement. The actual capacitance is 2x270\mu F.

It is important to make sure the output peak-to-peak ripple is less than the minimum OVP threshold. The ESR of the capacitor at 2 times the line frequency is found in the capacitor datasheet. The ESR is 367m\Omega.

\[
V_{\text{OPP}} = I_{\text{OUT}(\text{max})} \cdot \frac{\sqrt{(4\pi \cdot \text{line} \cdot C_{\text{O}} \cdot \text{ESR})^2 + 1}}{(4\pi \cdot \text{line} \cdot C_{\text{O}} \cdot 0.8)} (\text{EQ. 32})
\]

\[
V_{\text{OPP}} = 1.923A \cdot \frac{\sqrt{(4\pi \cdot 60Hz \cdot 540\mu F \cdot 0.367\Omega)^2 + 1}}{(4\pi \cdot 60Hz \cdot 540\mu F \cdot 0.8)} = 5.97V (\text{EQ. 33})
\]

The minimum OVP threshold is 103% of the nominal output value. The maximum output peak-to-peak ripple should be less than 6% of the nominal value, which is 23.4V_P_P.

**CURRENT SENSING RESISTORS**

Please refer to Equation 34 for calculation of the current sensing resistor R\text{CS}.

\[
R_{\text{CS}} \geq \frac{120mV \cdot 265V \cdot 0.92}{\sqrt{2 \cdot 750W}} = 0.028\Omega (\text{EQ. 34})
\]

While a large R\text{CS} renders better current sensing accuracy, larger R\text{CS} also incurs higher power dissipation. Select R\text{CS} from available standard value resistors to determine the sense resistor.

\[
R_{\text{CS}} = 0.044\Omega (\text{EQ. 35})
\]

The maximum power dissipation on the R\text{CS} occurs at low line and full load condition. The maximum power dissipation is calculated:

\[
P_{\text{RCSMAX}} = I_{\text{INMAX}}^2 \cdot R_{\text{CS}} (\text{EQ. 36})
\]

\[
P_{\text{RCSMAX}} = 9.06A^2 \cdot 0.044\Omega = 3.61W (\text{EQ. 37})
\]

The resistor R\text{SEN} sets the overcurrent protection limit.

\[
R_{\text{SEN}} \geq \frac{R_{\text{CS}} \cdot I_{\text{Peak}} \cdot (1 + 0.25)}{2 \cdot 0.5I_{\text{OC}}} (\text{EQ. 38})
\]

Where |x| stands for the ABS (x) function. I_{\text{OC}} is overcurrent threshold (in datasheet).

\[
R_{\text{SEN}} \geq \frac{0.044\Omega \cdot 14.4A \cdot 1.25}{159\mu A} = 5.0k\Omega (\text{EQ. 39})
\]

The selected R\text{SEN} is 5.2k\Omega.

**CURRENT LOOP COMPENSATION**

The input current shaping is achieved by comparing the sensed current signal to the sensed input voltage signal. The current error amplifier (Gmi), together with the current compensation network, adjusts the duty cycle so that the inductor current traces the sensed rectified voltage. Thus, unity power factor is achieved.

The compensation network consists of the Trans-Conductance error amplifier (Gmi) and the impedance network (Z\text{ICOMP}). The goal of the compensation network is to provide a closed loop transfer function with the sufficient 0dB crossing frequency.
Using the following guidelines for locating the poles and zeros of the compensation network.

Near crossover frequency, the transfer function from duty cycle to inductor current is well approximated Equation 42:

$$G_{id}(s) = \frac{V_{OUT}}{I_{BST} \cdot s}$$  \hspace{1cm} (EQ. 42)

The compensation gain uses external impedance networks as shown in Figure 2, $G_{ci}(s)$ is given by:

$$G_{ci}(s) = \frac{1}{(C_{ic} + C_{ip})} \cdot \frac{s}{2 \cdot \pi \cdot F_Z + 1}$$  \hspace{1cm} (EQ. 43)

The current gain and modulation gain $G_{sm}$ is:

$$G_{sm} = \frac{R_{cs} \cdot R_{sen}}{R_{is}^2} \cdot \frac{1}{2 \cdot V_m}$$  \hspace{1cm} (EQ. 44)

where $V_m$ is the amplitude of the PWM carrier. The open loop gain of the current loop is

$$G_{ILoop}(s) = G_{id}(s) \cdot G_{sm} \cdot G_{ci}(s)$$  \hspace{1cm} (EQ. 45)

It is recommended to set the crossover frequency from $1/10$ to $1/6$ of the switching frequency with phase margin of about $60^\circ$. A high frequency pole is set at $1/2$ or less of the switching frequency for ripple filtering. In this example, we set the crossover, $F_C$ at $1/9$ of the switching frequency.

$$F_Z = \frac{F_C}{\tan \left( \frac{F_C}{F_p} + \Phi_M \right)}$$  \hspace{1cm} (EQ. 46)

Where $F_C = F_{sw}/9 = 7.1kHz$, $\Phi_M$ is the phase margin, which is $50^\circ$. $F_P = F_{sw}/4 = 16kHz$.

Thus, the current loop compensation zero is:

$$F_Z = \frac{(64kHz)/9}{\tan \left( \frac{4}{9} + 50\text{deg} \right)} = 2.04kHz$$  \hspace{1cm} (EQ. 47)

The total compensation capacitance is calculated:

$$C_{ip} + C_{ic} = \left( \frac{V_{OUT}}{L_{BST} \cdot (2\pi f_c)^2 \cdot \frac{A_{IDC}}{V_m} \cdot \frac{R_{cs}}{R_{sen}}} \cdot \frac{1 + (f_c/f_p)^2}{1 + (f_c/f_p)^2} \right)^{1/2}$$  \hspace{1cm} (EQ. 48)

$$C_{ip} + C_{ic} = 8.148nF$$  \hspace{1cm} (EQ. 49)

$$C_{ip} = \left( \frac{C_{ip} + C_{ic}}{f_p} \right)^{1/2}$$  \hspace{1cm} (EQ. 50)

The value of the noise filtering capacitor is:

$$C_{ip} = 8.148nF \cdot \frac{2.04kHz}{16kHz} = 1.041nF$$  \hspace{1cm} (EQ. 51)

The value of $C_{ic}$ is:

$$C_{ic} = 8.148nF - 1.041nF = 7.1nF$$  \hspace{1cm} (EQ. 52)
The value of $R_{ic}$ is:

$$R_{ic} = \frac{1}{2\pi \cdot 2.04\,\text{kHz} \cdot 7.1\,\text{nF}} = 10.96\,\text{k}\Omega \quad \text{(EQ. 53)}$$

Select the RC value from the standard value, we have:

$$R_{ic} = 10\,\text{k}\Omega, \quad C_{ic} = 6.8\,\text{nF}, \quad C_{ip} = 1\,\text{nF}.$$ Figure 4 shows the bode plot of current loop gain, where $f_s = F_{sw}$.

**INPUT VOLTAGE SETTING**

First, set the BO resistor divider gain, $K_{BO}$ according to Equation 54.

Assuming the converter starts at $V_{LINE} = 80\,\text{V}_{\text{RMS}}$, then the BO resistor divider gain, $K_{BO}$ should be:

$$K_{BO} = \frac{0.5\,\text{V}}{80\,\text{V}_{\text{RMS}} - 2\,\text{V}} = 0.00641 \quad \text{(EQ. 54)}$$

In this design, two 200kΩ resistors in series are used for $R_{IN2}$. So, $R_{IN1}$ is calculated:

$$R_{IN1} = \frac{0.00641}{1 - 0.00641} \cdot (440\,\text{k}\Omega) = 2.581\,\text{k}\Omega \quad \text{(EQ. 55)}$$

Using resistor from the standard value, $R_{IN1} = 2.49\,\text{k}\Omega$, the actual $K_{BO}$ is calculated:

$$K_{BO} = \frac{R_{IN1}}{R_{IN1} + R_{IN2}} = 0.00619 \quad \text{(EQ. 56)}$$

**NEGATIVE INPUT CAPACITOR GENERATION**

The ISL6731A and ISL6731B generate an equivalent negative capacitance at the input to cancel the input filter capacitance. Thus, more input capacitors can be used without reducing the power factor.

The input equivalent negative capacitance is a function of the current sensing gain, BO resistor divider gain and the compensation components.

$$C_{NEG} = \left( K_{BO} \cdot 0.8 \cdot \frac{V_m}{V_{OUT}} \right) \cdot \frac{R_{SEN}}{R_{CS} A_{IDC}} (C_{ic} + C_{ip}) \quad \text{(EQ. 57)}$$

$$C_{NEG} = \left( 0.00619 \cdot 0.8 - 1.5 \right) \cdot \frac{5.2k}{390} \cdot \frac{0.044 \cdot 1.9}{(6.8nF + 1nF)} = 0.54\,\mu\text{F} \quad \text{(EQ. 58)}$$

This equivalent negative capacitor cancels the input filter capacitor required for EMI filtering. Therefore, the displacement power factor significantly improves.

For example, refer to the block diagram on page 4 in the ISL6731A, ISL6731B datasheet $C_{F2} + C_{F3} = 2\,\mu\text{F}, \quad C_{F1} = 0.68\,\mu\text{F}$, when $V_{LINE} = 230\,\text{V}_{\text{AC}}, \quad f_{LINE} = 50\,\text{Hz}, \quad P_O = 750\,\text{W}$.

Assuming 95% efficiency under the above test condition, the resistive component of the line current, which is in phase to voltage:

$$I_a = \frac{P_o}{V_{LINE} \cdot 0.95} = 3.432\,\text{A} \quad \text{(EQ. 59)}$$

The reactive current through the input capacitors:

$$I_c = V_{LINE} \cdot (2\pi \cdot f_{LINE}) \cdot (C_{F1} + C_{F2} + C_{F3}) = 0.232\,\text{A} \quad \text{(EQ. 60)}$$

Thus, the displacement power factor is:

$$PF_{DIS} = \frac{I_a}{\sqrt{(I_a)^2 + (I_c - I_{neg})^2}} = 0.9977 \quad \text{(EQ. 61)}$$

The reactive current generated by the equivalent negative capacitor is:

$$I_{neg} = V_{LINE} \cdot (2\pi \cdot f_{LINE}) \cdot C_{NEG} = 0.046\,\text{A} \quad \text{(EQ. 62)}$$

With the equivalent negative capacitor, the total reactive current reduces to:

$$I_c - I_{neg} = 0.186\,\text{A} \quad \text{(EQ. 63)}$$

The displacement power factor increases to:

$$PF_{DIS} = \frac{I_a}{\sqrt{(I_a)^2 + (I_c - I_{neg})^2}} = 0.9985 \quad \text{(EQ. 64)}$$

**VOLTAGE LOOP COMPENSATION**

The average boost diode forward current can be approximated by:

$$I_{D(ave)} = \frac{P_{in}}{V_{OUT}} \quad \text{(EQ. 65)}$$

Assuming the input current traces the input voltage perfectly. The input power is in proportion to $(V_{COMP} - 1\,\text{V})$.

$$I_{D(ave)} = \frac{R_{SEN}}{R_{CS} \cdot 0.5 \cdot R_{IS}} \cdot \frac{1}{V_{OUT}} \cdot \left( \frac{0.25}{((2\sqrt{2}/\pi)^2 \cdot K_{BO}) \cdot \Delta_{COMP}} \right) \quad \text{(EQ. 66)}$$

Where $\Delta_{COMP}$ is the $V_{COMP} - 1\,\text{V}$. 1V is the offset voltage.

$R_{IS}$ is the internal current scaling resistor. $R_{IS} = 14.2\,\text{k}\Omega$.

$$I_{D(ave)} = (2.13) \frac{A}{V} \cdot \Delta_{COMP} \quad \text{(EQ. 67)}$$
Thus, the transfer function from $V_{\text{COMP}}$ to $V_{\text{OUT}}$ is:

$$G_{\text{PS}}(s) = \frac{V_{\text{OUT}}(s)}{\Delta_{\text{COMP}}} = \frac{1}{C_{\text{O}} \cdot s} \frac{I_{\text{D}(\text{ave})}}{\Delta_{\text{COMP}}}$$  \hspace{1cm} (EQ. 68)

$$G_{\text{PS}}(s) = \left( \frac{I_{\text{D}(\text{ave})}}{C_{\text{O}} \cdot s} \frac{1}{\Delta_{\text{COMP}}} \right) = 2.13 \frac{1}{C_{\text{O}} \cdot s}$$  \hspace{1cm} (EQ. 69)

As shown in Figure 5, the voltage loop gain is:

$$G_{\text{VLOOP}}(s) = G_{\text{PS}}(s) \cdot G_{\text{DIV}} \cdot G_{\text{mv}} \cdot Z_{\text{COMP}}(s)$$  \hspace{1cm} (EQ. 70)

The output feedback resistor divider gain, $G_{\text{DIV}}$ is:

$$G_{\text{DIV}} = \frac{V_{\text{REF}}}{V_{\text{OUT}}}$$  \hspace{1cm} (EQ. 71)

The compensation gain uses external impedance networks as shown in Figure 5, $Z_{\text{COMP}}(s)$ is given by:

$$Z_{\text{COMP}}(s) = \frac{1}{(C_{\text{vc}} + C_{\text{vp}}) \cdot s + \frac{R_{\text{vc}} \cdot C_{\text{vc}} \cdot s + 1}{C_{\text{vc}} \cdot C_{\text{vp}}}}$$  \hspace{1cm} (EQ. 72)

The targeted crossover frequency, $F_{\text{CV}}$ is 10Hz. The high frequency pole, $F_{\text{PV}}$ is required in order to reject the 2 time line frequency component. $F_{\text{PV}} = 20Hz$. The targeted phase margin is 50°.

The zero, $F_{Z\text{v}}$ is calculated:

$$F_{Z\text{v}} = \frac{F_{\text{CV}}}{\tan(\Phi_{\text{m}} + \tan(F_{\text{CV}}/(F_{\text{PV}})))}$$  \hspace{1cm} (EQ. 73)

$$F_{Z\text{v}} = \frac{10\text{Hz}}{\tan(50\text{deg} + \tan((10\text{Hz})/(20\text{Hz})))} = 2.389\text{Hz}$$  \hspace{1cm} (EQ. 74)

Then the total capacitance used for compensation is calculated:

$$C_{\text{vc}} + C_{\text{vp}} = \left| \frac{G_{\text{PS}}(s) \cdot (2\pi F_{\text{CV}})}{2\pi F_{\text{CV}}} \right| \cdot \frac{G_{\text{DIV}} \cdot G_{\text{mv}}}{\sqrt{(F_{\text{CV}}/F_{Z\text{v}})^2 + 1}}$$  \hspace{1cm} (EQ. 75)

Thus, the total compensation capacitance is:

$$C_{\text{vc}} + C_{\text{vp}} = 1233\text{nF}$$  \hspace{1cm} (EQ. 76)

$$C_{\text{vp}} = 1233\text{nF} \cdot \frac{F_{Z\text{v}}}{F_{\text{PV}}} = 147\text{nF}$$  \hspace{1cm} (EQ. 77)

$$C_{\text{vc}} = 1233\text{nF} - 147\text{nF} = 1086\text{nF}$$  \hspace{1cm} (EQ. 78)

$$R_{\text{vc}} = \frac{1}{2 \cdot \pi \cdot F_{Z\text{v}} \cdot C_{\text{VC}}} = 61.3k\Omega$$  \hspace{1cm} (EQ. 79)

Choose components from the standard values. We have $C_{\text{vp}} = 150\text{nF}$, $C_{\text{VC}} = 1\mu\text{F}$, $R_{\text{VC}} = 62k\Omega$. The actual bode plot is shown in Figure 7.

**ADAPTIVE CONTROL**

ISL6730 and ISL6731 family have excellent power factor correction capability to achieve low THD and high PF with the above circuit optimization. To further improve THD at light and high line condition, Q3, Q4, Q5 and Q6 and two comparators are added to dynamically change current loop and current sense gain (refer to Figure 1). This simple analog implementation can achieve same level of THD and PF performance as DSP control.

The signal Sp controls Q6 (inverted) and Q4. Sp is controlled by load power level via the voltage level on COMP pin. Sp goes high at heavy load and low at light load.
At light load condition, COMP voltage is low. Sp goes low. Q4 turns off to increase Ric resistance to increase current loop gain and Q6 turns on to increase current sense gain. The increase of current loop and sense gain will push crossover frequency higher to improve THD.

The signal Sv controls Q3 and Q5. Sv is controlled by line voltage via the voltage level on BO pin. Sv goes high at low line and low at high line.

At high line condition, BO voltage is low. Sv goes low. Q5 turns off to increase Ric resistance to increase current loop gain and Q3 turns off to increase current sense gain. The increase of current loop and sense gain will push crossover frequency higher to improve THD.

At light load or high line condition, the boost inductor current is relatively small. The converter runs in discontinuous conduction mode. In this condition the CCM frequency domain model cannot be used for analysis. In DCM condition, the current loop will be inherently stable and thus can be pushed to run in a higher gain and crossover frequency configuration.
# Bill of Materials

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## Bill of Materials (Continued)

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PCB Layout

FIGURE 10. TOP LAYER

FIGURE 11. BOTTOM LAYER
Assembly Drawing

FIGURE 12. ASSEMBLY ON TOP
Performance Curves and Typical Waveforms

FIGURE 13. EFFICIENCY vs LOAD, ISL6731AEVAL2Z

FIGURE 14. EFFICIENCY vs LOAD, ISL6731BEVAL2Z

FIGURE 15. POWER FACTOR vs LOAD, ISL6731AEVAL2Z

FIGURE 16. POWER FACTOR vs LOAD, ISL6731BEVAL2Z

FIGURE 17. THD vs LOAD, ISL6731AEVAL2Z

FIGURE 18. THD vs LOAD, ISL6731BEVAL2Z
Performance Curves and Typical Waveforms (Continued)

FIGURE 19. WAVEFORMS OF LINE CURRENT AND VOLTAGE (115V/FULL LOAD)

FIGURE 20. WAVEFORMS OF LINE CURRENT AND VOLTAGE (230V/FULL LOAD)

FIGURE 21. SWITCHING WAVEFORMS