ISL70001ASEHEV1Z

Evaluation Board

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The ISL70001ASEHEV1Z evaluation board is designed to demonstrate the features of the ISL70001ASEH, a TID and SEE hardened 6A synchronous buck regulator IC with integrated MOSFETs intended for Space applications. For more detailed information about the ISL70001ASEH, please refer to the ISL70001ASEH datasheet.

The ISL70001ASEHEV1Z evaluation board accepts a nominal 3V to 5.5V input voltage and provides a regulated output voltage ranging from 0.8V to 85% of the input voltage at output currents ranging from 0A to 6A. The output can be quickly set to any of six commonly used preset voltages (0.8V, 1.0V, 1.2V, 1.8V, 2.5V, 3.3V) or adjusted to an alternate voltage using the onboard potentiometer. A PGOOD (Power-Good) signal goes high and lights a red LED to indicate that the output voltage is within a ±11% typical regulation window. A toggle switch is provided to conveniently enable or disable the output voltage.

The ISL70001ASEHEV1Z evaluation board can be set to run from the nominal 1MHz internal oscillator of the ISL70001ASEH or synchronized to a 1MHz ±20% external clock. Two or more ISL70001ASEHEV1Z evaluation boards can be synchronized to each other in a Master/Slave configuration, with all Slave units switching 180° out-of-phase with respect to the Master unit.

Schematic and BOM

A schematic and BOM of the ISL70001ASEHEV1Z evaluation board are shown in Figure 1 and Table 1, respectively. The schematic indicates numerous test points, which allow virtually all nodes of the evaluation circuit to be monitored directly. The BOM shows components that are representative of the types needed for a design, but these components are not space-qualified. Equivalent space-qualified components would be required for flight applications.

Recommended Test Equipment

- A 0V to 6V power supply with at least 10A source current capability.
- An electronic load capable of sinking current up to 6A.
- Two digital multimeters (DMMs).
- A 500MHz dual-trace oscilloscope.

Quick Start

1. Short J1, J2 (pins 2-3), J4 (pins 1-2), J5 and J15.
2. Open J3, J7 and J9-J13.
3. Toggle S2 to the down (OFF) position.
4. Turn on the power supply. Set the output voltage to 3.3V and set the output current limit to 10A. Turn off the power supply.
5. Connect the positive lead of the power supply to TP1 and the negative lead of the power supply to TP2.
6. Turn on the electronic load and set the output current to 3A.
7. Connect the positive lead of the electronic load to TP44 and connect the negative lead of the electronic load to TP45.
8. Configure one DMM to monitor the input voltage from TP22 to TP25.
9. Configure another DMM to monitor the output voltage from TP38 to TP39.
10. Connect Channel 1 of the oscilloscope to J6 (or from TP33 to TP28) to monitor the rectangular waveform on the LXx pins.
11. Connect Channel 2 of the oscilloscope to J14 (or from TP36 to TP37) to monitor the output voltage.
12. Toggle S2 to the up (ON) position.
13. Verify the output voltage is 0.8V ±3% and the frequency of the LXx waveform is 1MHz ±10%.

Configuration Options

The ISL70001ASEHEV1Z evaluation board can be easily configured for a number of different applications. Table 2 provides the available settings for the jumpers and toggle switch and explains their respective functions.

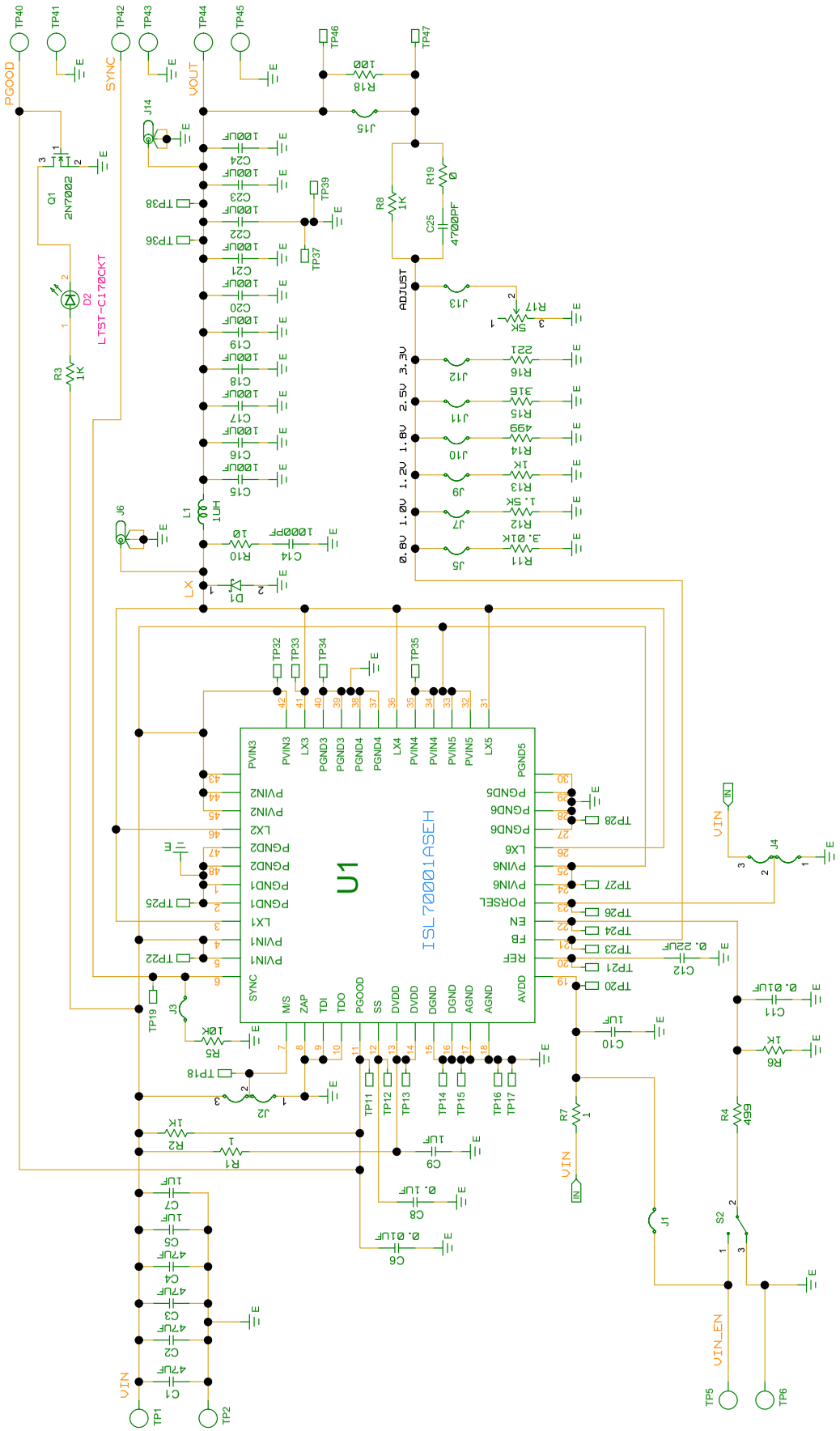

FIGURE 1. ISL70001ASEHEV1Z SCHEMATIC

TABLE 1. ISL70001ASEHEV1Z BOM

REF DES	QTY	PART NUMBER	VALUE	DESCRIPTION	MANUFACTURER
C1-C4	4		47µF	Capacitor, Ceramic, 10%, 10V, X7R, 1210	Various
C5, C7, C9, C10	4		1µF	Capacitor, Ceramic, 10%, 10V, X7R, 0603	Various
C6, C11	2		0.01µF	Capacitor, Ceramic, 10%, 16V X7R, 0603	Various
C8	1		0.1µF	Capacitor, Ceramic, 10%, 16V, X7R, 0603	Various
C12	1		0.22µF	Capacitor Ceramic, 10%, 16V, X7R, 0603	Various
C14	1		1000pF	Capacitor Ceramic, 10%, 16V, X7R, 0603	Various
C15-C24	10		100µF	Capacitor Ceramic, 20%, 6.3V, X5R, 1210	Various
C25	1		4700pF	Capacitor, Ceramic, 10%, 50V, X7R, 0603	Various
D1	1	MBRS320T3G-T		Diode, Schottky, 20V, 3A, SMC	On Semiconductor
D2	1	LTST-C170CKT		Diode, LED, Green	Vishay
J1, J3, J5, J7, J9-J13	9	69190-202HLF		Connector, Header, 1x2, Thru-hole	BERG/FCI
J2, J4	2	68000-236HLF-1X3		Connector, Header, 1x3, Thru-hole	BERG/FCI
J1-J5, J7, J9-J13, J15	12	SPC02SYAN		Connector, Jumper, 2-pin	Sullins
J6, J14	2	131-4353-00		Jack, Scope Probe, Thru-hole	Tektronics
L1	1	CDRH127/LDNP-1R0NC	1µH	Inductor, 30%, 14A, SMD	Sumida
Q1	1	2N7002-7-F-T		Transistor, MOSFET, N-channel, SOT-23	Diodes, Inc.
R1, R7	2		1Ω	Resistor, Film, 1%, 1/10W, 0603	Various
R2, R3, R6, R8, R13	5		1kΩ	Resistor, Film, 1%, 1/10W, 0603	Various
R4, R14	2		499Ω	Resistor, Film, 1%, 1/10W, 0603	Various
R5	1		10kΩ	Resistor, Film, 1%, 1/10W, 0603	Various
R10	1		10Ω	Resistor, Film, 1%, 1/4W, 1206	Various
R11	1		3.01kΩ	Resistor, Film, 1%, 1/10W, 0603	Various
R12	1		1.5kΩ	Resistor, Film, 1%, 1/10W, 0603	Various
R15	1		316Ω	Resistor, Film, 1%, 1/10W, 0603	Various
R16	1		221Ω	Resistor, Film, 1%, 1/10W, 0603	Various
R17	1	3296W-1-502LF	5kΩ	Resistor, Potentiometer, Trim, 10%, 1/2W, Thru-hole	Bourns
R18	1		100Ω	Resistor, Film, 1%, 1/10W, 0603	Various
R19	1		0Ω	Resistor, Film, 1%, 1/10W, 0603	Various
S2	1	GT11MSCBE-T		Switch, Toggle, SPDT, SMD	ITT/C&K
TP1, TP2, TP5, TP6, TP40-45	10	1514-2		Terminal, Turret, Thru-hole	Keystone
TP11-TP28, TP32-TP39	26	5002		Connector, Test Point, Thru-hole	Various
U1	1	ISL70001ASEHFE/PROTO		IC, Regulator, Switching, 6A, CQFP-48 w/ heatsink	Intersil
	1	SP2000-0.020-AC-1212-NA		Thermal Interface Material, Sil-Pad, 12inx12inx0.020in, with adhesive, cut to 0.4in x 0.4in and place under U1	Bergquist

TABLE 2. CONFIGURATION OPTIONS

REF. DESIGNATOR	SETTING	FUNCTION
J1	Short	Selects AVDD to be monitored by the EN pin through a resistive divider (R4 and R6) if S2 is toggled to the down position.
	Open	Allows an external voltage connected to TP5 to be monitored by the EN pin through a resistive divider (R4 and R6) if S2 is toggled to the down position.
J2	Short 2-3	Selects Master mode, which forces the chip to run from the internal 1MHz oscillator. In Master mode, the SYNC pin is an output that provides a nominal 1MHz clock signal.
	Short 1-2	Selects Slave mode, which allows the chip to be synchronized to another ISL70001ASEH or to an external clock. In Slave mode, the SYNC pin is an input that accepts a 1MHz synchronizing signal from the SYNC pin of another ISL70001ASEH configured as a Master or from an external clock.
J3	Short	Loads the SYNC pin with R5, which is a 10kΩ resistor. If synchronization to an external clock over long distances is required, it may be necessary to use a controlled impedance trace to avoid excessive ringing on the SYNC line. If this is the case, the SYNC trace should be terminated into 50Ω at the Slave units. This can be accomplished by replacing R5 on the Slave units with a 50Ω resistor. Please note that the SYNC pin of an ISL70001ASEH is not designed to drive a 50Ω load.
	Open	Disconnects the SYNC pin from R5.
J4	Short 2-3	Selects the 5V input UVLO threshold. Use this setting when the nominal input voltage is 5V.
	Short 1-2	Selects the 3.3V input UVLO threshold. Use this setting when the nominal input voltage is 3.3V. Also use this setting for nominal input voltages between 5V and 3.3V.
J5	Short	Selects the 0.8V preset output voltage option as long as J7 and J9-J13 are open.
	Open	Allows output voltages other than 0.8V to be selected.
J7	Short	Selects the 1.0V preset output voltage option as long as J5 and J9-J13 are open.
	Open	Allows output voltages other than 1.0V to be selected.
J9	Short	Selects the 1.2V preset output voltage option as long as J5, J7 and J10-J13 are open.
	Open	Allows output voltages other than 1.2V to be selected.
J10	Short	Selects the 1.8V preset output voltage option as long as J5, J7, J9 and J11-J13 are open.
	Open	Allows output voltages other than 1.8V to be selected.
J11	Short	Selects the 2.5V preset output voltage option as long as J5, J7, J9-J10 and J12-J13 are open.
	Open	Allows output voltages other than 2.5V to be selected.
J12	Short	Selects the 3.3V preset output voltage option as long as J5, J7, J9-J11 and J13 are open.
	Open	Allows output voltages other than 3.3V to be selected.
J13	Short	Selects the adjustable output voltage option as long as J5, J7 and J9-J12 are open. Potentiometer, R17, can be used to adjust the output voltage.
	Open	Allows the preset output voltage options to be selected.
J15	Short	Shorts out R18, allowing normal operation of the evaluation board.
	Open	Facilitates control loop stability measurements by allowing a signal to be injected across R18.
S2	Short 2-3	S1 in the up position shorts contacts 2-3. This pulls the EN pin low to disable the output voltage.
	Short 1-2	S1 in the down position shorts contacts 1-2. This enables the output voltage as long as the voltage on the EN pin exceeds 0.6V.

Layout Guidelines

1. Use a four layer PCB with 2 ounce copper.
2. Layer 2 should be a dedicated ground plane and layer 3 should be a dedicated power plane split between VIN and VOUT.
3. Layers 1 and 4 should be used primarily for signals, but can also be used to increase the VIN, VOUT and ground planes as required.
4. Connect all AGND, DGND and PGNDx pins directly to the ground plane. Connect all PVINx pins directly to the VIN portion of the power plane.
5. Locate ceramic bypass capacitors as close as possible to U1. Prioritize the placement of the bypass capacitors on the pins of U1 in the order shown: REF, SS, AVDD, DVDD, PVINx (C5, C7), EN, PGOOD, PVINx (C1-C4).
6. Locate the output voltage resistive divider as close as possible to the FB pin of the IC. The top leg of the divider should connect directly to the POL (Point Of Load) and the bottom leg of the resistive divider should connect directly to AGND. The junction of the resistive divider should connect directly to the FB pin.
7. Locate the Schottky diode, D1, as close as possible to the LXx and PGNDx pins of the IC. A smaller Schottky diode may be used as long as derating requirements are satisfied.
8. Use a small island of copper to connect the LXx pins of U1 to the inductor, L1, on layers 1 and 4. Void the copper on layers 2 and 3 adjacent to the island to minimize capacitive coupling. Place most of the island on layer 4 to minimize the amount of copper that must be voided from the ground layer (layer 2).
9. Keep all signal traces as short as possible.
10. A small series snubber (R10 and C14) connected from the LXx pins to the PGNDx pins may be used to damp ringing on the LXx pins if desired.
11. For optimum thermal performance, place a pattern of vias on the top layer of the PCB directly underneath U1. Connect the vias to the ground plane (layer 2), which serves as a heatsink. Thermal interface material such as a Sil-Pad should be used to fill the gap between the vias and the bottom of U1 to insure good thermal contact. Using a Sil-Pad has the added benefit of raising the bottom of U1 from the PCB surface so that a slight bend can be added to the leads for strain relief.
12. Refer to Figures 2 through 7 for an example layout.

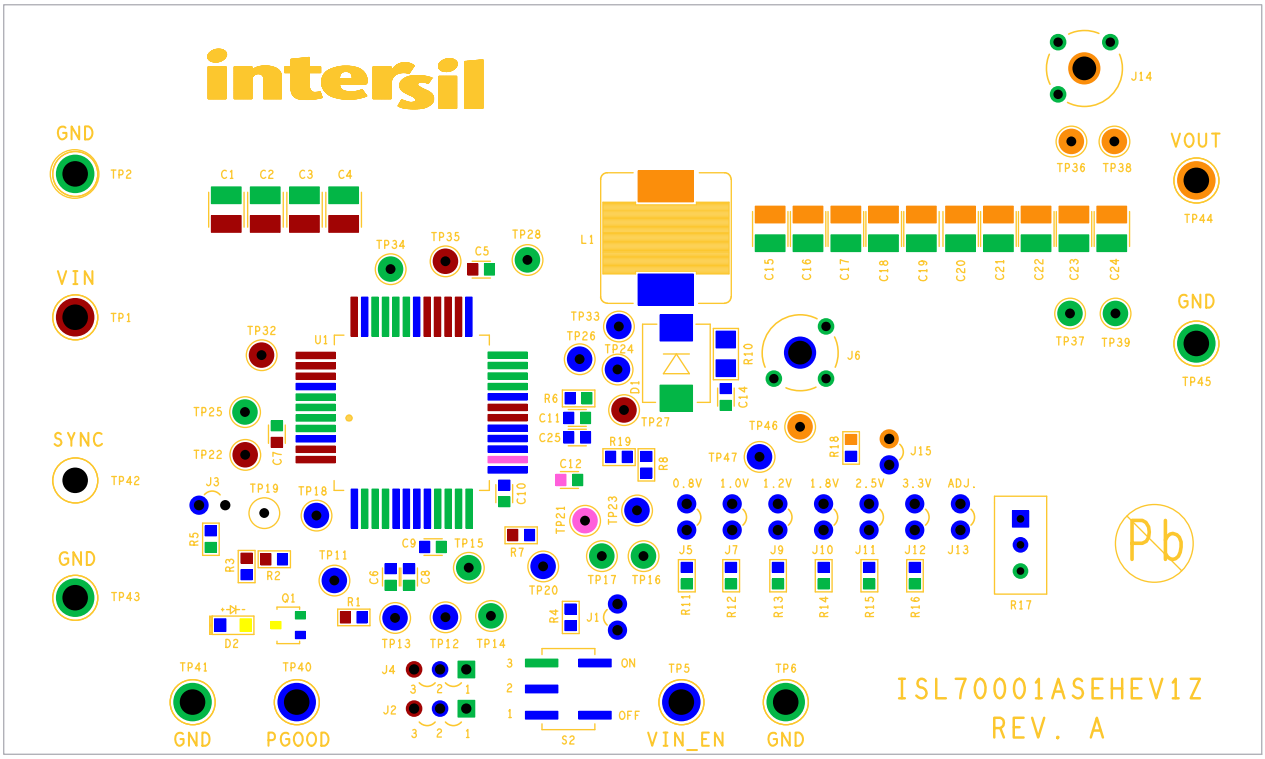

FIGURE 2. SILK SCREEN TOP

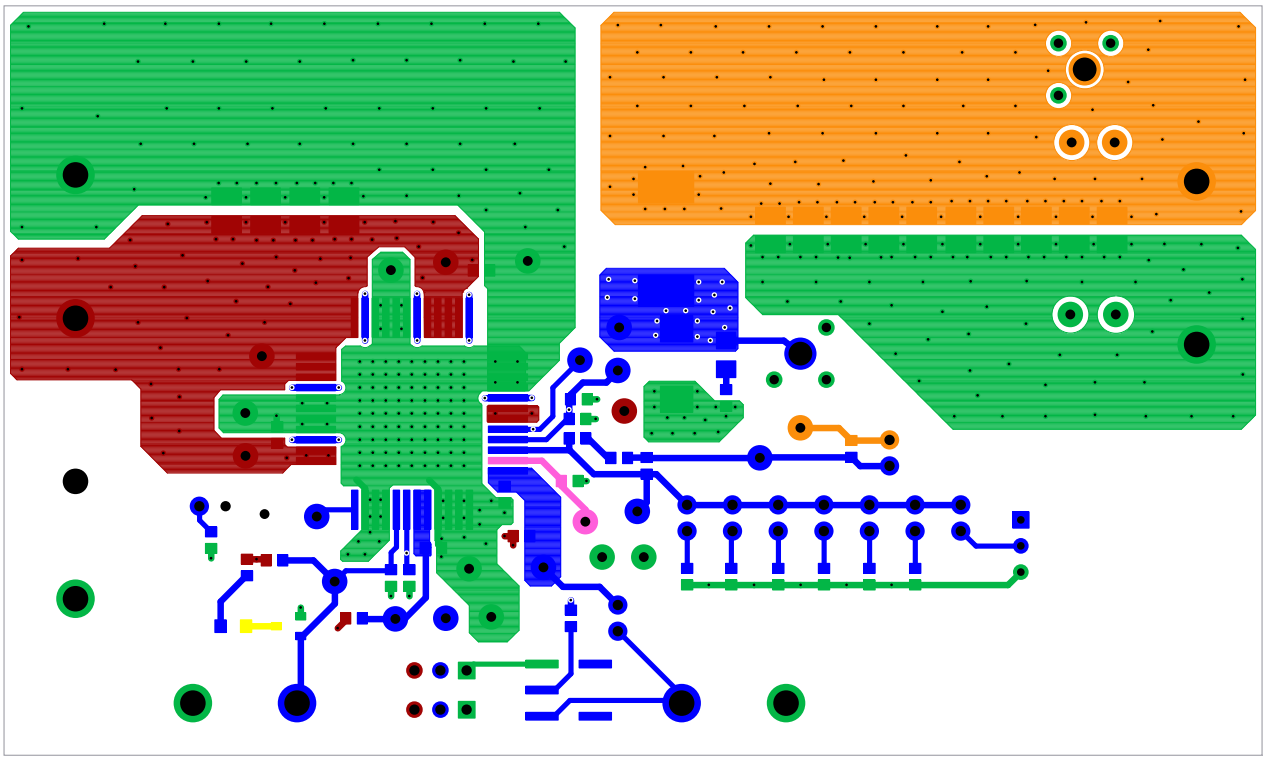

FIGURE 3. FIRST LAYER ETCH

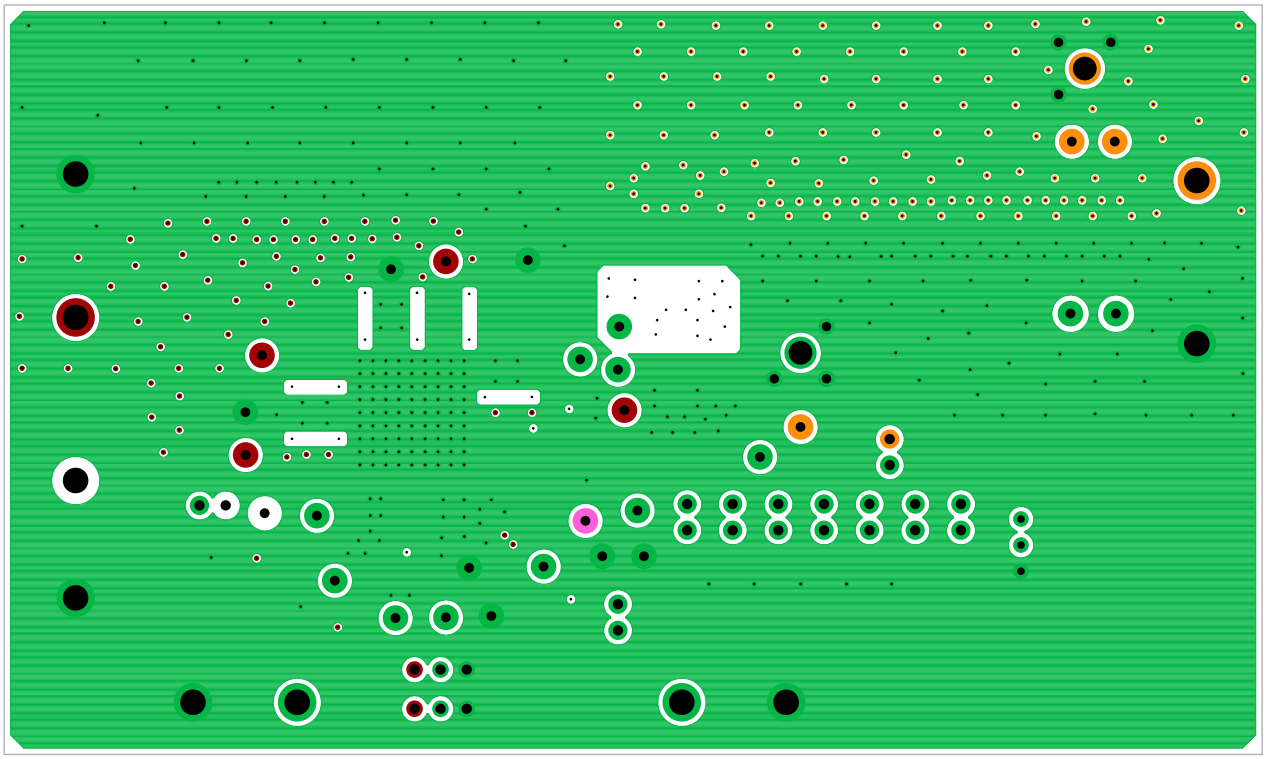

FIGURE 4. SECOND LAYER ETCH

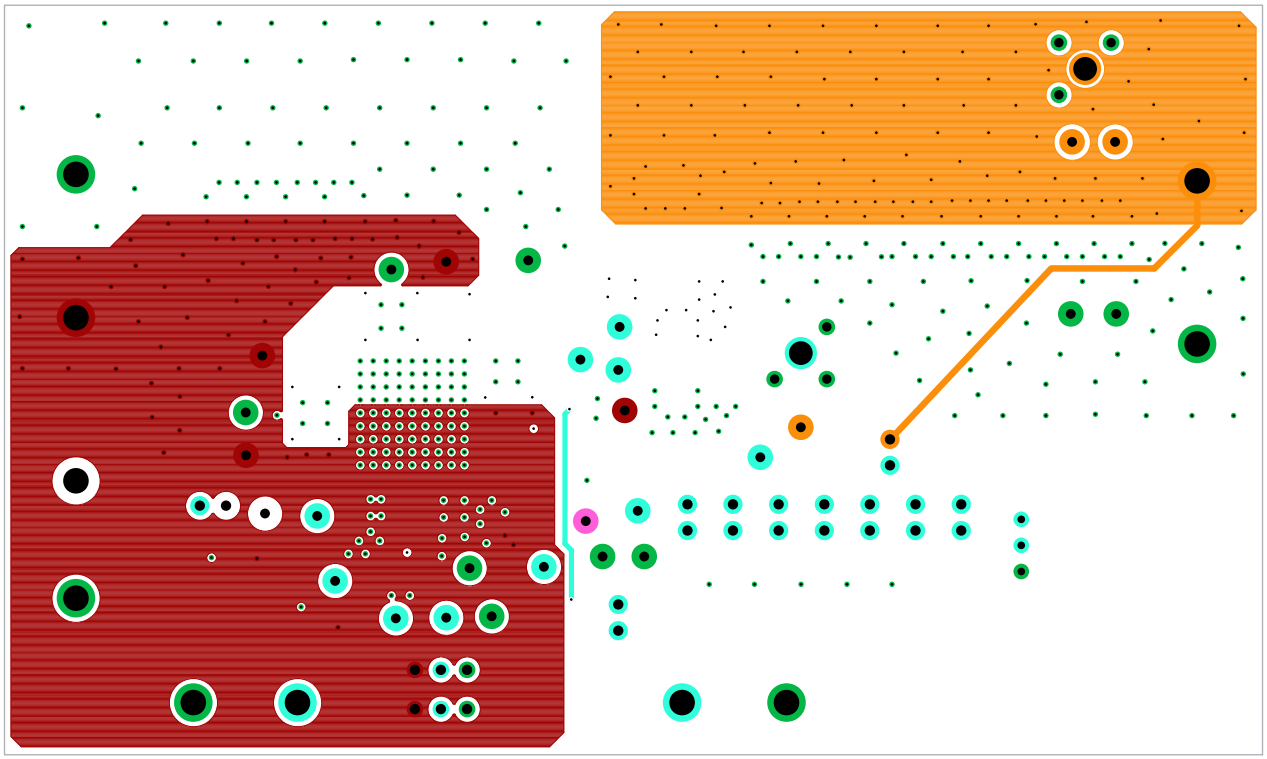

FIGURE 5. THIRD LAYER ETCH

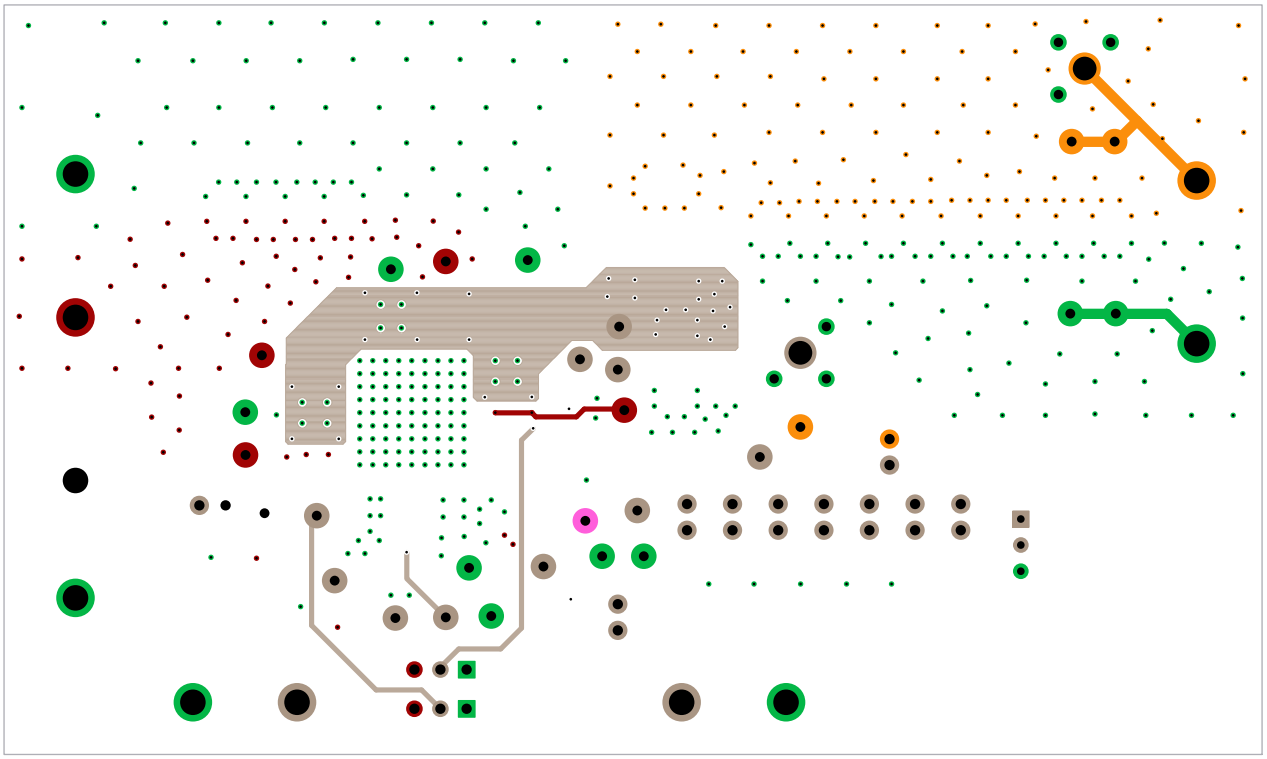

FIGURE 6. FOURTH LAYER ETCH

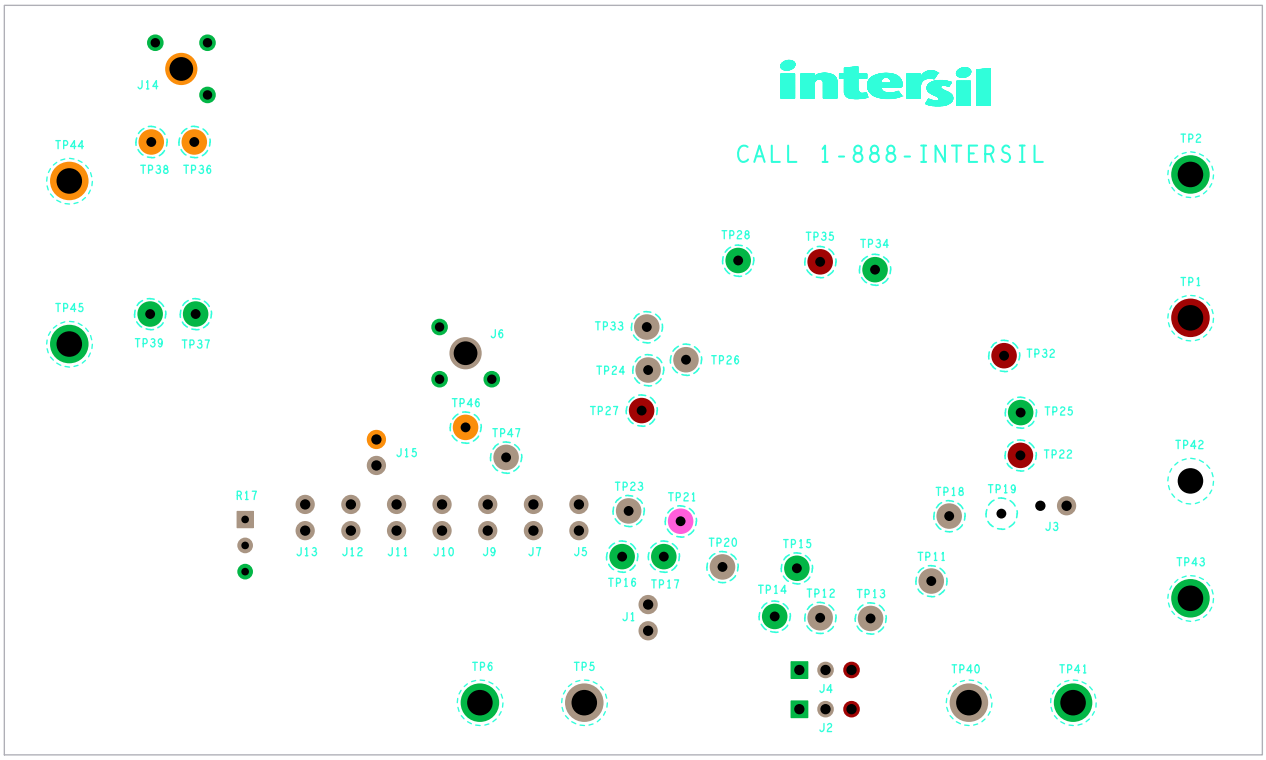

FIGURE 7. SILK SCREEN BOTTOM

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