The **ISL8026, ISL8026A** are highly efficient, monolithic, synchronous step-down DC/DC converters that can deliver 6A of continuous output current from a 2.5V to 5.5V input supply. The devices use current mode control architecture to deliver a very low duty cycle operation at high frequency with fast transient response and excellent loop stability.

The ISL8026, ISL8026A integrate a very low ON-resistance P-channel (36mΩ) high-side FET and N-channel (13mΩ) low-side FET to maximize efficiency and minimize external component count. The 100% duty-cycle operation allows less than 180mV dropout voltage at 6A output current. The operation frequency of the Pulse-width Modulator (PWM) is adjustable from 500kHz to 4MHz. The default switching frequency, which is set by connecting the FS pin high, is 1MHz for the ISL8026 and 2MHz for the ISL8026A.

The ISL8026, ISL8026A can be configured for discontinuous or forced continuous operation at light load. Forced continuous operation reduces noise and RF interference, while discontinuous mode provides higher efficiency by reducing switching losses at light loads.

Fault protection is provided by internal hiccup mode current limiting during short-circuit and overcurrent conditions. Other protection, such as overvoltage and over-temperature, are also integrated into the device. A power-good output voltage monitor indicates when the output is in regulation.

The ISL8026, ISL8026A offer a 1ms Power-Good (PG) timer at power-up. When in shutdown, the ISL8026, ISL8026A discharge the output capacitor through an internal soft-stop switch. Other features include internal fixed or adjustable soft-start and internal/external compensation.

The ISL8026, ISL8026A are offered in a space saving 16 Ld 3x3 Pb-free TQFN package with an exposed pad for improved thermal performance and 0.8mm maximum height. The complete converter occupies less than 142mm².

**Features**

- 2.5V to 5.5V input voltage range
- Very low ON-resistance FETs - P-channel 36mΩ and N-channel 13mΩ typical values
- High efficiency synchronous buck regulator with up to 95% efficiency
- 1.0% reference accuracy over load/line/temperature (-40°C to +85°C)
- 1.5% reference accuracy over load/line/temperature (-40°C to +125°C)
- Internal soft-start: 1ms or adjustable
- Soft-stop output discharge during disable
- Adjustable frequency from 500kHz to 4MHz - default at 1MHz (ISL8026) or 2MHz (ISL8026A)
- External synchronization up to 4MHz
- Over-temperature, overcurrent, overvoltage and negative overcurrent protection

**Applications**

- DC/DC POL modules
- µC/µP, FPGA and DSP power
- Video processor/SOC power
- Li-ion battery powered devices
- Routers and switchers
- Portable instruments
- Test and measurement systems
- Industrial PCs

**Related Literature**

- UG033, “ISL8026xEVAL3Z Evaluation Board User Guide”
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### Pin Descriptions

<table>
<thead>
<tr>
<th>PIN NUMBER</th>
<th>SYMBOL</th>
<th>DESCRIPTION</th>
</tr>
</thead>
<tbody>
<tr>
<td>1, 2, 16</td>
<td>VIN</td>
<td>Input supply voltage. Place a minimum of two 22μF ceramic capacitors from VIN to PGND as close as possible to the IC for decoupling.</td>
</tr>
<tr>
<td>3</td>
<td>PG</td>
<td>Power-good is an open-drain output. Use a 10kΩ to 100kΩ pull-up resistor connected between VIN and PG. At power-up or EN HI, PG rising edge is delayed by 1ms once the output voltage reaches regulation.</td>
</tr>
<tr>
<td>4</td>
<td>SYNC</td>
<td>Mode Selection pin. Connect to logic high or input voltage VIN for PWM mode. Connect to logic low or ground for PFM mode. Connect to an external function generator for synchronization with the positive edge trigger. There is an internal 1MΩ pull-down resistor to prevent an undefined logic state in case the SYNC pin is floating.</td>
</tr>
<tr>
<td>5</td>
<td>EN</td>
<td>Regulator enable pin. Enable the output when driven high. Shut down the chip and discharge output capacitor when driven low.</td>
</tr>
<tr>
<td>6</td>
<td>FS</td>
<td>This pin sets the oscillator switching frequency using a resistor, RFS, from the FS pin to GND. The frequency of operation may be programmed between 500kHz to 4MHz. The default frequency is 1MHz (ISL8026), 2MHz (ISL8026A) if FS is connected to VIN.</td>
</tr>
<tr>
<td>7</td>
<td>SS</td>
<td>SS is used to adjust the soft-start time. Connect to SGND for internal 1ms rise time. Connect a capacitor from SS to SGND to adjust the soft-start time. Do not use more than 33nF per IC.</td>
</tr>
<tr>
<td>8, 9</td>
<td>COMP, FB</td>
<td>The feedback network of the regulator, FB, is the negative input to the transconductance error amplifier. The output voltage is set by an external resistor divider connected to FB. With a properly selected divider, the output voltage can be set to any voltage between the power rail (reduced by converter losses) and the 0.6V reference. COMP is the output of the amplifier if COMP is not tied to VIN. Otherwise, COMP is disconnected through a MOSFET for internal compensation. Must connect COMP to VIN in internal compensation mode to meet a typical application. Additional external networks across COMP and SGND might be required to improve the loop compensation of the amplifier operation. In addition, the regulator power-good and undervoltage protection circuitry use FB to monitor the regulator output voltage.</td>
</tr>
<tr>
<td>10</td>
<td>PGND/SGND</td>
<td>Power/signal ground</td>
</tr>
<tr>
<td>11, 12</td>
<td>PGND</td>
<td>Power ground</td>
</tr>
<tr>
<td>13, 14, 15</td>
<td>PHASE</td>
<td>Switching node connections. Connect to one terminal of the inductor. This pin is discharged by a 100Ω resistor when the device is disabled. See &quot;Block Diagram&quot; on page 5 for more detail.</td>
</tr>
</tbody>
</table>

**Exposed Pad**

- The exposed pad must be connected to the SGND pin for proper electrical performance. Place as many vias as possible under the pad connecting to the SGND plane for optimal thermal performance.
Ordering Information

<table>
<thead>
<tr>
<th>PART NUMBER (Notes 1, 2, 3)</th>
<th>PART MARKING</th>
<th>OPERATION FREQUENCY (MHz)</th>
<th>TEMP. RANGE (°C)</th>
<th>PACKAGE (RoHS COMPLIANT)</th>
<th>PKG. DWG. #</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISL8026IRTAJZ 026A</td>
<td>1</td>
<td>-40 to +85</td>
<td>16 Ld 3x3 TQFN</td>
<td>L16.3x3D</td>
<td></td>
</tr>
<tr>
<td>ISL8026AIRTAJZ 26AA</td>
<td>2</td>
<td>-40 to +85</td>
<td>16 Ld 3x3 TQFN</td>
<td>L16.3x3D</td>
<td></td>
</tr>
<tr>
<td>ISL8026FRTAJZ 026F</td>
<td>1</td>
<td>-40 to +125</td>
<td>16 Ld 3x3 TQFN</td>
<td>L16.3x3D</td>
<td></td>
</tr>
<tr>
<td>ISL8026AFRTAJZ 026AF</td>
<td>2</td>
<td>-40 to +125</td>
<td>16 Ld 3x3 TQFN</td>
<td>L16.3x3D</td>
<td></td>
</tr>
<tr>
<td>ISL8026EVAL3Z</td>
<td>Evaluation board for ISL8026</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>ISL8026AEVAL3Z</td>
<td>Evaluation board for ISL8026A</td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

NOTES:
1. Add "-T" suffix for 6k unit or "-T7A" suffix for 250 unit Tape and Reel options. Please refer to TB347 for details on reel specifications.
2. These Intersil Pb-free plastic packaged products employ special Pb-free material sets, molding compounds/die attach materials, and 100% matte tin plate plus anneal (e3 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations). Intersil Pb-free products are MSL classified at Pb-free peak reflow temperatures that meet or exceed the Pb-free requirements of IPC/JEDEC J STD-020.
3. For Moisture Sensitivity Level (MSL), please see device information page for ISL8026, ISL8026A. For more information on MSL please see techbrief TB363.

TABLE 1. SUMMARY OF KEY DIFFERENCES

<table>
<thead>
<tr>
<th>PART NUMBER</th>
<th>IOUT (MAX) (A)</th>
<th>fSW RANGE (MHz)</th>
<th>VIN RANGE (V)</th>
<th>VOUT RANGE (V)</th>
<th>PART SIZE (mm)</th>
</tr>
</thead>
<tbody>
<tr>
<td>ISL8026</td>
<td>6</td>
<td>Programmable 0.5MHz to 4MHz</td>
<td>2.5 to 5.5</td>
<td>0.6 to 5.5</td>
<td>3x3</td>
</tr>
<tr>
<td>ISL8026A</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
</tbody>
</table>

TABLE 2. ISL8026 COMPONENT SELECTION

<table>
<thead>
<tr>
<th>VOUT</th>
<th>0.8V</th>
<th>1.2V</th>
<th>1.5V</th>
<th>1.8V</th>
<th>2.5V</th>
<th>3.3V</th>
<th>3.6V</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
</tr>
<tr>
<td>C2</td>
<td>4 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
</tr>
<tr>
<td>C3</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
</tr>
<tr>
<td>L1</td>
<td>0.47~1µH</td>
<td>0.47~1µH</td>
<td>0.47~1µH</td>
<td>0.68~1.5µH</td>
<td>0.68~1.5µH</td>
<td>1~2.2µH</td>
<td>1~2.2µH</td>
</tr>
<tr>
<td>R2</td>
<td>33kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
</tr>
<tr>
<td>R3</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
</tr>
</tbody>
</table>

TABLE 3. ISL8026A COMPONENT SELECTION

<table>
<thead>
<tr>
<th>VOUT</th>
<th>0.8V</th>
<th>1.2V</th>
<th>1.5V</th>
<th>1.8V</th>
<th>2.5V</th>
<th>3.3V</th>
<th>3.6V</th>
</tr>
</thead>
<tbody>
<tr>
<td>C1</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
</tr>
<tr>
<td>C2</td>
<td>3 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
<td>2 x 22µF</td>
</tr>
<tr>
<td>C3</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
<td>22µF</td>
</tr>
<tr>
<td>L1</td>
<td>0.22~0.47µH</td>
<td>0.22~0.47µH</td>
<td>0.22~0.47µH</td>
<td>0.33~0.68µH</td>
<td>0.33~0.68µH</td>
<td>0.47~1µH</td>
<td>0.47~1µH</td>
</tr>
<tr>
<td>R2</td>
<td>33kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
</tr>
<tr>
<td>R3</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
<td>100kΩ</td>
</tr>
</tbody>
</table>
FIGURE 3. FUNCTIONAL BLOCK DIAGRAM
Absolute Maximum Ratings  (Reference to GND)

VIN  ................................................................. -0.3V to 5.8V (DC) or 7V (20ms)
EN, FS, PG, SYNC, VFB  .............................................. -0.3V to VIN + 0.3V
PHASE  .......................................................... -1.5V (100ns)/-0.3V (DC) to 6.5V (DC) or 7V (20ms)
COMP, SS  ...................................................... -0.3V to 2.7V

ESD Ratings
- Human Body Model (Tested per JESD22-A114) ............................. 3kV
- Charged Device Model (Tested per JESD22-C101E) .................... 2kV
- Machine Model (Tested per JESD22-A115) ................................ 200V
- Latch-Up (Tested per JESD-78A; Class 2, Level A) ........................ 100mA at +85°C

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions may adversely impact product 
reliability and result in failures not covered by warranty.

NOTES:
4. \( \theta_{JA} \) is measured in free air with the component mounted on a high effective thermal conductivity test board with “direct attach” features. See Tech 
Brief TB379.
5. \( \theta_{JC} \) “case temperature” location is at the center of the exposed metal pad on the package underside.

Thermal Information

Thermal Resistance
\( \theta_{JA} \) (°C/W)  \( \theta_{JC} \) (°C/W)
16 LD TQFN Package (Notes 4, 5) .................................. 47 6.5

Junction Temperature Range ........................................... -55°C to +125°C
Storage Temperature Range ........................................... -65°C to +150°C

Recommended Operating Conditions

VIN Supply Voltage Range ........................................... 2.5V to 5.5V
Load Current Range .................................................. 0A to 6A
Ambient Temperature Range (Industrial) ...................... -40°C to +85°C
Ambient Temperature Range (Full-Range Industrial) .......................... -40°C to +125°C

Electrical Specifications

Unless otherwise noted, all parameter limits are established across the recommended operating conditions 
and are measured at the following conditions: VIN = 3.6V, EN = VIN, unless otherwise noted. Typical values are at \( T_A = +25°C \). Unless otherwise noted,
Boldface limits apply across the operating temperature range, -40°C to +125°C

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN (Note 6)</th>
<th>TYP</th>
<th>MAX (Note 6)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>INPUT SUPPLY</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>VIN Undervoltage Lockout Threshold</td>
<td>VUVLO</td>
<td>Rising, no load</td>
<td>2.3</td>
<td>2.5</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>Falling, no load</td>
<td>2.10</td>
<td>2.25</td>
<td>V</td>
<td></td>
</tr>
<tr>
<td>Quiescent Supply Current</td>
<td>IIN</td>
<td>SYNC = GND, no load at the output</td>
<td>50</td>
<td></td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYNC = GND, no load at the output and no switching</td>
<td>50</td>
<td>62</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYNC = VIN, fSW = 1MHz, no load at the output (ISL8026)</td>
<td>9</td>
<td>16</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td></td>
<td></td>
<td>SYNC = VIN, fSW = 2MHz, no load at the output (ISL8026A)</td>
<td>16</td>
<td>23</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Shutdown Supply Current</td>
<td>ISD</td>
<td>SYNC = GND, VIN = 5.5V, EN = low</td>
<td>5</td>
<td>8</td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>OUTPUT REGULATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Reference Voltage</td>
<td>VREF</td>
<td>-40°C &lt; TJ &lt; +85°C</td>
<td>0.594</td>
<td>0.600</td>
<td>0.606</td>
<td>V</td>
</tr>
<tr>
<td></td>
<td></td>
<td>-40°C &lt; TJ &lt; +125°C</td>
<td>0.591</td>
<td>0.600</td>
<td>0.606</td>
<td>V</td>
</tr>
<tr>
<td>VFB Bias Current</td>
<td>IREF</td>
<td>VFB = 0.75V</td>
<td>0.1</td>
<td></td>
<td>µA</td>
<td></td>
</tr>
<tr>
<td>Line Regulation</td>
<td>VIN</td>
<td>VIN = VD + 0.5V to 5.5V (minimal 2.5V)</td>
<td>0.2</td>
<td></td>
<td>%/V</td>
<td></td>
</tr>
<tr>
<td>Soft-Start Ramp Time Cycle</td>
<td>SS</td>
<td>SS = SGND</td>
<td>1</td>
<td></td>
<td>ms</td>
<td></td>
</tr>
<tr>
<td>Soft-Start Charging Current</td>
<td>ISS</td>
<td>VSS = 0.1V</td>
<td>1.45</td>
<td>1.85</td>
<td>2.25</td>
<td>µA</td>
</tr>
<tr>
<td>OVERCURRENT PROTECTION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Current Limit Blanking Time</td>
<td>tOCON</td>
<td></td>
<td>17</td>
<td></td>
<td>Clock pulses</td>
<td></td>
</tr>
<tr>
<td>Overcurrent and Auto Restart Period</td>
<td>tOCOFF</td>
<td></td>
<td>8</td>
<td></td>
<td>SS cycle</td>
<td></td>
</tr>
<tr>
<td>Positive Peak Current Limit</td>
<td>IPLIMIT</td>
<td>6A application</td>
<td>7.5</td>
<td>9</td>
<td>11</td>
<td>A</td>
</tr>
<tr>
<td>Peak Skip Limit</td>
<td>ISKIP</td>
<td>6A application (See &quot;Application Information&quot; on page 19 for more detail)</td>
<td>1</td>
<td>1.3</td>
<td>1.8</td>
<td>A</td>
</tr>
<tr>
<td>Zero Cross Threshold</td>
<td></td>
<td></td>
<td>-300</td>
<td>300</td>
<td>mA</td>
<td></td>
</tr>
<tr>
<td>Negative Current Limit</td>
<td>INLIMIT</td>
<td></td>
<td>-4.5</td>
<td>-3.0</td>
<td>-1.5</td>
<td>A</td>
</tr>
</tbody>
</table>
**Electrical Specifications**  Unless otherwise noted, all parameter limits are established across the recommended operating conditions and are measured at the following conditions: \( V_{IN} = 3.6\text{V} \), \( EN = V_{IN} \), unless otherwise noted. Typical values are at \( T_A = +25 \text{°C} \). Unless otherwise noted, **Boldface limits apply across the operating temperature range, -40°C to +125°C (Continued)**

<table>
<thead>
<tr>
<th>PARAMETER</th>
<th>SYMBOL</th>
<th>TEST CONDITIONS</th>
<th>MIN (Note 6)</th>
<th>TYP</th>
<th>MAX (Note 6)</th>
<th>UNIT</th>
</tr>
</thead>
<tbody>
<tr>
<td>COMPENSATION</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>Error Amplifier Transconductance</td>
<td></td>
<td>Internal compensation</td>
<td>60</td>
<td></td>
<td></td>
<td>( \mu\text{A}/\text{V} )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>External compensation</td>
<td>120</td>
<td></td>
<td></td>
<td>( \mu\text{A}/\text{V} )</td>
</tr>
<tr>
<td>Transresistance</td>
<td>( R_t )</td>
<td>6A application (test at 3.6V) [-40°\text{C} &lt; T_J &lt; +85°\text{C}]</td>
<td>0.119</td>
<td>0.140</td>
<td>0.166</td>
<td>( \Omega )</td>
</tr>
<tr>
<td></td>
<td></td>
<td>6A application (test at 3.6V) [-40°\text{C} &lt; T_J &lt; +125°\text{C}]</td>
<td>0.110</td>
<td>0.140</td>
<td>0.170</td>
<td>( \Omega )</td>
</tr>
<tr>
<td>PHASE</td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
<td></td>
</tr>
<tr>
<td>P-Channel MOSFET ON-Resistance</td>
<td>( V_{IN} = 5V ), ( I_O = 200mA )</td>
<td></td>
<td></td>
<td>36</td>
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<td>( V_{IN} = 2.7V ), ( I_O = 200mA )</td>
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<td></td>
<td>52</td>
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<td>PHASE Maximum Duty Cycle</td>
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<td>PHASE Minimum On-Time</td>
<td>( \text{SYNC} = \text{High} )</td>
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<td>Nominal Switching Frequency</td>
<td>( f_{SW} )</td>
<td>( f_{SW} = V_{IN}.\text{ISL8026A.} ; -40°\text{C} &lt; T_J &lt; +85°\text{C} )</td>
<td>1600</td>
<td>2000</td>
<td>2400</td>
<td>kHz</td>
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<td>( f_{SW} = V_{IN}.\text{ISL8026A.} ; -40°\text{C} &lt; T_J &lt; +125°\text{C} )</td>
<td>1550</td>
<td>2000</td>
<td>2450</td>
<td>kHz</td>
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<td></td>
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<td>( f_{SW} = V_{IN}.\text{ISL8026} )</td>
<td>780</td>
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<td>( f_{SW} ) with ( RS = 402\text{kΩ} )</td>
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<td>SYNC Logic LOW to HIGH Transition Range</td>
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<td>SYNC Logic Input Leakage Current</td>
<td>( V_{IN} = 3.6\text{V} )</td>
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<td>Delay Time (Rising Edge)</td>
<td>Time from ( V_{OUT} ) reached regulation</td>
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<td>UVP PG Rising Threshold</td>
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<td>UVP PG Hysteresis</td>
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<td>PGOOD Delay Time (Falling Edge)</td>
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<td>EN Logic Input Leakage Current</td>
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<td>Thermal Shutdown</td>
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**NOTE:**
6. Compliance to datasheet limits is assured by one or more methods: production test, characterization and/or design.
**Typical Operating Performance**  Unless otherwise noted, operating conditions are: $T_A = +25\,^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$.

SYNC = $V_{IN}$, $L = 1.0\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to $6A$. Resistor load is used in the test.

**FIGURE 4.** EFFICIENCY vs LOAD (1MHz $3.3V_{IN}$ PWM)

**FIGURE 5.** EFFICIENCY vs LOAD (1MHz $3.3V_{IN}$ PFM)

**FIGURE 6.** EFFICIENCY vs LOAD (1MHz $5V_{IN}$ PWM)

**FIGURE 7.** EFFICIENCY vs LOAD (1MHz $5V_{IN}$ PFM)

**FIGURE 8.** EFFICIENCY vs LOAD (2MHz $3.3V_{IN}$ PWM)

**FIGURE 9.** EFFICIENCY vs LOAD (2MHz $3.3V_{IN}$ PFM)
**Typical Operating Performance**  Unless otherwise noted, operating conditions are: $T_A = +25^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$,  
$SYNC = V_{IN}$, $L = 1.0\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to $6A$. Resistor load is used in the test. (Continued)
**Typical Operating Performance**  
Unless otherwise noted, operating conditions are: $T_A = +25^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$. $SYNC = V_{IN}$, $L = 1.0\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to $6A$. Resistor load is used in the test. (Continued)
**Typical Operating Performance**  
Unless otherwise noted, operating conditions are: $T_A = +25\, ^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$. $SYNC = V_{IN}$, $L = 1.0\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to 6A. Resistor load is used in the test. (Continued)
Typical Operating Performance

Unless otherwise noted, operating conditions are: \( T_A = +25 \, ^\circ \text{C}, \, V_{IN} = 5 \, \text{V}, \, \text{EN} = V_{IN} \).

SYNC = \( V_{IN} \), \( L = 1 \, \mu \text{H}, \, C_1 = 22 \, \mu \text{F}, \, C_2 = 2 \times 22 \, \mu \text{F}, \, I_{OUT} = 0 \, \text{A} \) to 6A. Resistor load is used in the test. (Continued)

**FIGURE 25. START-UP AT 6A LOAD (PFM)**

**FIGURE 26. SHUTDOWN AT 6A LOAD (PFM)**

**FIGURE 27. START-UP AT 3A LOAD (PWM)**

**FIGURE 28. SHUTDOWN AT 3A LOAD (PWM)**

**FIGURE 29. START-UP AT 3A LOAD (PFM)**

**FIGURE 30. SHUTDOWN AT 3A LOAD (PFM)**
Typical Operating Performance

Unless otherwise noted, operating conditions are: $T_A = +25\, ^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$, $SYNC = V_{IN}$, $L = 1\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to $6A$. Resistor load is used in the test. (Continued)
Typical Operating Performance

Unless otherwise noted, operating conditions are: $T_A = +25^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$, $SYNC = V_{IN}$, $L = 1.0\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to $6A$. Resistor load is used in the test. (Continued)
Typical Operating Performance

Unless otherwise noted, operating conditions are: $T_A = +25\, ^\circ\text{C}$, $V_{\text{IN}} = 5\, \text{V}$, $EN = V_{\text{IN}}$.

$SYNC = V_{\text{IN}}$, $L = 1.0\mu\text{H}$, $C_1 = 22\mu\text{F}$, $C_2 = 2 \times 22\mu\text{F}$, $I_{\text{OUT}} = 0\, \text{A}$ to $6\, \text{A}$. Resistor load is used in the test. (Continued)
Typical Operating Performance  Unless otherwise noted, operating conditions are: $T_A = +25^\circ C$, $V_{IN} = 5V$, $EN = V_{IN}$, $SYNC = V_{IN}$, $L = 1.0\mu H$, $C_1 = 22\mu F$, $C_2 = 2 \times 22\mu F$, $I_{OUT} = 0A$ to $6A$. Resistor load is used in the test. (Continued)

**FIGURE 49. PFM TO PWM TRANSITION**

600mA MODE TRANSITION, COMPLETELY ENTER TO PWM AT 640mA

**FIGURE 50. PWM TO PFM TRANSITION**

BACK TO PFM AT 360mA

**FIGURE 51. OVERVOLTAGE PROTECTION**

**FIGURE 52. OVER-TEMPERATURE PROTECTION**
Theory of Operation

The ISL8026, ISL8026A are step-down switching regulators optimized for battery-powered applications. The regulators operate at a 1MHz or 2MHz fixed default switching frequency for high efficiency and allow smaller form factor when FS is connected to VIN. By connecting a resistor from FS to SGND, the operational frequency adjustable range is 500kHz to 4MHz. At light load, the regulator reduces the switching frequency, unless forced to the fixed frequency, to minimize the switching loss and to maximize the battery life. The quiescent current when the output is not loaded is typically only 50µA. The supply current is typically only 5µA when the regulator is shut down.

PWM Control Scheme

Pulling the SYNC pin HI (>0.8V) forces the converter into PWM mode, regardless of output current. The ISL8026, ISL8026A employs the current-mode Pulse-width Modulation (PWM) control scheme for fast transient response and pulse-by-pulse current limiting. Figure 3 on page 5 shows the functional block diagram. The current loop consists of the oscillator, the PWM comparator, current sensing circuit and the slope compensation for the current loop stability. The slope compensation is 440mV/Ts, which changes with frequency. The gain for the current sensing circuit is typically 140mV/A. The control reference for the current loops comes from the Error Amplifier’s (EAMP) output.

The PWM operation is initialized by the clock from the oscillator. The P-Channel MOSFET is turned on at the beginning of a PWM cycle and the current in the MOSFET starts to ramp up. When the sum of the current amplifier, CSA, and the slope compensation reaches the control reference of the current loop, the PWM comparator COMP sends a signal to the PWM logic to turn off the P-FET and turn on the N-channel MOSFET. The N-FET stays on until the end of the PWM cycle. Figure 53 shows the typical operating waveforms during the PWM operation. The dotted lines illustrate the sum of the slope compensation ramp and the Current-Sense Amplifier’s (CSA) output.

The output voltage is regulated by controlling the V_{EAMP} voltage to the current loop. The bandgap circuit outputs a 0.6V reference voltage to the voltage loop. The feedback signal comes from the VFB pin. The soft-start block only affects the operation during the start-up and will be discussed separately. The error amplifier is a transconductance amplifier that converts the voltage error signal to a current output. The voltage loop is internally compensated with the 55pF and 100kΩ RC network. The maximum EAMP voltage output is precisely clamped to 1.6V.

FIGURE 53. PWM OPERATION WAVEFORMS

SKIP Mode

Pulling the SYNC pin LOW (<0.4V) forces the converter into PFM mode. The ISL8026, ISL8026A enters a pulse-skipping mode at light load to minimize the switching loss by reducing the switching frequency. Figure 54 illustrates the skip mode operation. A zero-cross sensing circuit shown in Figure 3 on page 5 monitors the N-FET current for zero crossing. When 16 consecutive cycles are detected, the regulator enters the Skip mode. During the sixteen detecting cycles, the current in the inductor is allowed to become negative. The counter is reset to zero when the current in any cycle does not cross zero.

Once the skip mode is entered, the pulse modulation starts being controlled by the Skip comparator shown in Figure 3 on page 5. Each pulse cycle is still synchronized by the PWM clock. The P-FET is turned on at the clock’s rising edge and turned off when the output is higher than 1.2% of the nominal regulation or when its current reaches the peak skip current limit value. Then, the inductor current is discharged to 0A and stays at zero (the internal clock is disabled) and the output voltage reduces gradually due to the load current discharging the output capacitor. When the output voltage drops to the nominal voltage, the P-FET will be turned on again at the rising edge of the internal clock as it repeats the previous operations.

The regulator resumes normal PWM mode operation when the output voltage drops 2.5% below the nominal voltage.

FIGURE 54. SKIP MODE OPERATION WAVEFORMS
**Frequency Adjust**

The frequency of operation is fixed at 1MHz for ISL8026, 2MHz for ISL8026A when FS is tied to VIN. Adjustable frequency ranges from 500kHz to 4MHz via a simple resistor connecting FS to SGND, according to **Equation 2**:

\[
R_{FS} \,[\text{k} \Omega] = \frac{220 \cdot 10^3}{f_{OSC} \,[\text{kHz}]} - 14
\]  

**(EQ. 2)**

**Overcurrent Protection**

The overcurrent protection is realized by monitoring the CSA output with the OCP comparator, as shown in Figure 3 on page 5. The current sensing circuit has a gain of 140mV/A, from the P-FET current to the CSA output. When the CSA output reaches the threshold, the OCP comparator is tripped to turn off the P-FET immediately. The overcurrent function protects the switching converter from a shorted output by monitoring the current flowing through the upper MOSFET.

Upon detection of an overcurrent condition, the upper MOSFET will be immediately turned off and will not be turned on again until the next switching cycle. Upon detection of the initial overcurrent condition, the overcurrent fault counter is set to 1. If, on the subsequent cycle, another overcurrent condition is detected, the OC fault counter will be incremented. If there are 17 sequential OC fault detections, the regulator will be shut down under an overcurrent fault condition. An overcurrent fault condition will result in the regulator attempting to restart in a hiccup mode within the delay of eight soft-start periods. At the end of the 8th soft-start wait period, the fault counters are reset and soft-start is attempted again. If the overcurrent condition goes away during the delay of 8 soft-start periods, the output will resume back into regulation after hiccup mode expires.

**Negative Current Protection**

Similar to overcurrent, the negative current protection is realized by monitoring the current across the low-side N-FET, as shown in Figure 3 on page 5. When the valley point of the inductor current and the ON-resistance of the P-FET.

**Power MOSFETs**

The power MOSFETs are optimized for best efficiency. The ON-resistance for the P-FET is typically 36mΩ and the ON-resistance for the N-FET is typically 13mΩ.

**100% Duty Cycle**

The ISL8026, ISL8026A features a 100% duty cycle operation to maximize the battery life. When the battery voltage drops to a level that the ISL8026, ISL8026A can no longer maintain the regulation at the output, the regulator completely turns off the error amplifier. This voltage ramp limits the inductor current as well as the output voltage speed, so that the output voltage rises in a controlled fashion. When VFB is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz, so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in the Skip mode to support prebiased output condition.

**Soft Start-Up**

The soft start-up reduces the inrush current during the start-up. The soft-start block outputs a ramp reference to the input of the error amplifier. This voltage ramp limits the inductor current as well as the output voltage speed, so that the output voltage rises in a controlled fashion. When VFB is less than 0.1V at the beginning of the soft-start, the switching frequency is reduced to 200kHz, so that the output can start-up smoothly at light load condition. During soft-start, the IC operates in the Skip mode to support prebiased output condition.

Tie SS to SGND for internal soft-start, which is approximately 1ms. Connect a capacitor from SS to SGND to adjust the soft-start time. This capacitor, along with an internal 1.85μA current source sets the soft-start interval of the converter, \( t_{SS} \), as shown by **Equation 3**.

\[
C_{SS}[\mu F] = 3.1 \cdot t_{SS}[s]
\]  

**(EQ. 3)**

C_{SS} must be less than 33nF to insure proper soft-start reset after fault condition.

**Enable**

The Enable (EN) input allows the user to control the turning on or off of the regulator for purposes such as power-up sequencing. When the regulator is enabled, there is typically a 600μs delay for waking up the bandgap reference and then the soft-start up begins.

**Discharge Mode (Soft-Stop)**

When a transition to shutdown mode occurs or the VIN UVLO is set, the outputs discharge to GND through an internal 100Ω switch.

When the input voltage is below the Undervoltage Lockout (UVLO) threshold, the regulator is disabled.
**Power Derating Characteristics**

To prevent the regulator from exceeding the maximum junction temperature, some thermal analysis is required. The temperature rise is given by Equation 4:

\[ T_{\text{RISE}} = (PD) \theta_{JA} \]  

(EQ. 4)

Where PD is the power dissipated by the regulator and \( \theta_{JA} \) is the thermal resistance from the junction of the die to the ambient temperature. The junction temperature, \( T_J \), is given by Equation 5:

\[ T_J = (T_A + T_{\text{RISE}}) \]  

(EQ. 5)

Where \( T_A \) is the ambient temperature. For the TQFN package, the \( \theta_{JA} \) is 47 \(^\circ\text{C/W}\).

The actual junction temperature should not exceed the absolute maximum junction temperature of +125\(^\circ\text{C}\) when considering the thermal design.

The ISL8026, ISL8026A uses an internal compensation network and the output capacitor value is dependent on the output voltage. The ceramic capacitor is recommended to be X5R or X7R. The recommended X5R or X7R minimum output capacitor values are shown in Table 3 on page 4.

In Table 3, the minimum output capacitor value is given for the different output voltages to ensure that the whole converter system is stable. Additional output capacitance should be added for better performance in applications where high load transient or low output ripple is required. It is recommended to check the system level performance along with the simulation model.

**Output Voltage Selection**

The output voltage of the regulator can be programmed via an external resistor divider that is used to scale the output voltage, relative to the internal reference voltage, and feed it back to the inverting input of the error amplifier (refer to Figure 1 on page 1). The output voltage programming resistor, \( R_2 \), will depend on the value chosen for the feedback resistor and the desired output voltage of the regulator. The value for the feedback resistor, \( R_3 \), is typically between 10k\( \Omega \) and 100k\( \Omega \), as shown in Equation 7.

\[ R_2 = R_3 \left( \frac{V_O}{V_{\text{FBI}}} - 1 \right) \]  

(EQ. 7)

If the output voltage desired is 0.6V, then \( R_3 \) is left unpopulated and \( R_2 \) is shorted. There is a leakage current from \( V_{\text{IN}} \) to PHASE. It is recommended to preload the output with 10\( \mu \text{A} \) minimum. For better performance, add 22\( \mu \text{F} \) in parallel with \( R_2 \) (200k\( \Omega \)). Check loop analysis before use in application.

**Input Capacitor Selection**

The main functions for the input capacitor are to provide decoupling of the parasitic inductance and provide a filtering function to prevent the switching current flowing back to the battery rail. At least two 22\( \mu \text{F} \) X5R or X7R ceramic capacitors are a good starting point for the input capacitor selection.

**Loop Compensation Design**

When COMP is not connected to \( V_{\text{IN}} \), the COMP pin is active for external loop compensation. The ISL8026, ISL8026A uses constant frequency peak current mode control architecture to achieve a fast loop transient response. An accurate current sensing pilot device in parallel with the upper MOSFET is used for peak current control signal and overcurrent protection. The inductor is not considered as a state variable since its peak current is constant and the system becomes a single order system. It is much easier to design a type II compensator to stabilize the loop than to implement voltage mode control. Peak current mode control has an inherent input voltage feed-forward function to achieve good line regulation. Figure 56 on page 20 shows the small signal model of the synchronous buck regulator.
Figure 57 shows the type II compensator and its transfer function is expressed as shown in Equation 8:

\[
A_v(S) = \frac{\dot{V}_{\text{comp}}}{V_{\text{FB}}} = \frac{\text{GM} \cdot R_3}{(C_6 + C_7) \cdot (R_2 + R_3)} \left( 1 + \frac{S}{\omega_{cz1}} \right) \left( 1 + \frac{S}{\omega_{cz2}} \right) \left( 1 + \frac{S}{\omega_{cp1}} \right) \left( 1 + \frac{S}{\omega_{cp2}} \right)
\]

(EQ. 8)

Where,

\[
\omega_{cz1} = \frac{1}{R_6 C_6}, \quad \omega_{cz2} = \frac{1}{R_2 C_3}, \quad \omega_{cp1} = \frac{C_6 + C_7}{R_6 C_6 C_7}, \quad \omega_{cp2} = \frac{R_2 + R_3}{C_3 R_2 R_3}
\]

Compensator design goal:

High DC gain

Choose loop bandwidth \(f_c\) less than 100kHz

Gain margin: >10dB

Phase margin: >40°

The compensator design procedure is as follows:

The loop gain at crossover frequency of \(f_c\) has a unity gain. Therefore, the compensator resistance \(R_6\) is determined by Equation 9.

\[
R_6 = \frac{2\pi f_c V_o C_o R_1}{\text{GM} \cdot V_{\text{FB}}} = 12.2 \times 10^3 \cdot f_c V_o C_o
\]

(EQ. 9)

Where GM is the sum of the transconductance, \(g_{m}\), of the voltage error amplifier in each phase. Compensator capacitor \(C_6\) is then given by Equation 10.

\[
C_6 = \max \left( \frac{R_6 C_o}{R_6}, \frac{1}{\pi f_c R_6} \right)
\]

(EQ. 10)

Put one compensator pole at zero frequency to achieve high DC gain, and put another compensator pole at either ESR zero frequency or half switching frequency, whichever is lower in Equation 10. An optional zero can boost the phase margin. \(\omega_{cz2}\) is a zero due to \(R_2\) and \(C_3\).

Put compensator zero 2 to 5 times \(f_c\).

Example: \(V_{\text{IN}} = 5\text{V}, V_o = 1.8\text{V}, I_o = 6\text{A}, f_{sw} = 1\text{MHz}, R_2 = 200\text{k}\Omega, R_3 = 100\text{k}\Omega, C_6 = 2 \times 22 \mu \text{F} / 3 \text{mF}, L = 1\mu \text{H}, f_c = 100\text{kHz}\), then compensator resistance \(R_6\):

\[
R_6 = 12.2 \times 10^3 \cdot 100\text{kHz} \cdot 1.8\text{V} \cdot 44\mu \text{F} = 97.6\text{k}\Omega
\]

(EQ. 12)

\[
C_6 = \frac{1.8\text{V} \cdot 44\mu \text{F}}{6\text{A} \cdot 97.6\text{k}\Omega} = 135\text{pF}
\]

(EQ. 13)

\[
C_7 = \max (\frac{3\text{mF} \cdot 44\mu \text{F}}{97.6\text{k}\Omega} \cdot \frac{1}{\pi \cdot 1\text{MHz}(97.6\text{k}\Omega)}) = (1\text{pF}, 3.3\text{pF})
\]

(EQ. 14)

It is also acceptable to use the closest standard values for \(C_6\) and \(C_7\). There is approximately 3pF parasitic capacitance from \(V_{\text{COMP}}\) to GND. Therefore, \(C_7\) is optional. Use \(C_6 = 150\text{pF}\) and \(C_7 = \text{OPEN}\).

\[
C_3 = \frac{1}{\pi 100\text{kHz} \cdot 200\text{k}\Omega} = 16\text{pF}
\]

(EQ. 15)

Use \(C_3 = 15\text{pF}\). Note that \(C_3\) may increase the loop bandwidth from previous estimated value. Figure 58 on page 21 shows the simulated voltage loop gain. It is shown that it has a 150kHz loop bandwidth with a 42° phase margin and 10dB gain margin. It may be more desirable to achieve an increased phase margin. This can be accomplished by lowering \(R_6\) by 20% to 30%.
PCB Layout Recommendation

The PCB layout is a very important converter design step to make sure the designed converter works well. For the ISL8026, ISL8026A, the power loop is composed of the output inductor L's, the output capacitor (COUT), the PHASE pins and the PGND pin. It is necessary to make the power loop as small as possible and the connecting traces among them should be direct, short and wide. The switching node of the converter, the PHASE pins and the traces connected to the node are very noisy, so keep the voltage feedback trace away from these noisy traces. The input capacitor should be placed as close as possible to the VIN pin. The ground of input and output capacitors should be connected as close as possible. The heat of the IC is mainly dissipated through the thermal pad. Maximizing the copper area connected to the thermal pad is preferable. In addition, a solid ground plane is helpful for better EMI performance. It is recommended to add at least 5 vias ground connection within the pad for the best thermal relief.

![Simulated Loop Gain](image)

**FIGURE 58. SIMULATED LOOP GAIN**
Revision History

The revision history provided is for informational purposes only and is believed to be accurate, but not warranted. Please go to web to make sure you have the latest revision.

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<th>REVISION</th>
<th>CHANGE</th>
</tr>
</thead>
<tbody>
<tr>
<td>October 28, 2016</td>
<td>FN8736.2</td>
<td>On page 1, last paragraph - converted - 0.22in² to 142mm².</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added “1.5% reference accuracy over load/line/temperature (−40°C to +125°C)” to Features section on page 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated Ordering Information table on page 4:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added 2 parts - ISL8026FRTAJZ and ISL8026AFRTAJZ</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Removed “-T” from bulk parts and added Tape and Reel unit options to Note 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated Recommended Operating Conditions: Added full-range industrial temperature range</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Electrical Spec table updates:</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Reference Voltage added temp −40°C &lt; TJ &lt; +85°C and added row for −40°C &lt; TJ &lt; +125°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Transresistance - Added temp −40°C &lt; TJ &lt; +85°C and added row for temperature −40°C &lt; TJ &lt; +125°C</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Nominal Switching Frequency - added temperature −40°C &lt; TJ &lt; +85°C and added row for temperature −40°C &lt; TJ &lt; +125°C</td>
</tr>
<tr>
<td>June 26, 2015</td>
<td>FN8736.1</td>
<td>Updated the 4th Features bullet by changing from 1.2% to 1% and adding temperature range.</td>
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<tr>
<td></td>
<td></td>
<td>Updated Applications bullets. on page 1.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added Related Literature section.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Added evaluation boards to Ordering Information table on page 4.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>In “Electrical Specifications” on page 6, updated min/max specs for Reference Voltage parameter (min) from “0.593” to “0.594” and (max) from “0.607” to “0.606”.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated Equation 9 and Equations 12 through 14 on page 20.</td>
</tr>
<tr>
<td></td>
<td></td>
<td>Updated example I0 information from “5A” to “6A” on page 20.</td>
</tr>
<tr>
<td>May 13, 2015</td>
<td>FN8736.0</td>
<td>Initial Release</td>
</tr>
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</table>

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Package Outline Drawing
L16.3x3D
16 LEAD THIN QUAD FLAT NO-LEAD PLASTIC PACKAGE
Rev 0, 3/10

NOTES:

1. Dimensions are in millimeters.
   Dimensions in (    ) for Reference Only.


3. Unless otherwise specified, tolerance : Decimal ± 0.05

4. Dimension applies to the metallized terminal and is measured between 0.15mm and 0.25mm from the terminal tip.

5. Tiebar shown (if present) is a non-functional feature.

6. The configuration of the pin #1 identifier is optional, but must be located within the zone indicated. The pin #1 identifier may be either a mold or mark feature.

7. JEDEC reference drawing: MO-220 WEED.