HS-5104ARH, HS-5104AEH

Radiation Hardened, Low Noise Quad Operational Amplifiers

FN3025
Rev 5.00
July 12, 2013

The HS-5104ARH, HS-5104AEH are radiation hardened, monolithic quad operational amplifiers that provide highly reliable performance in harsh radiation environments. Excellent noise characteristics coupled with a unique array of dynamic specifications make these amplifiers well-suited for a variety of satellite system applications. Dielectrically isolated, bipolar processing makes these devices immune to Single Event Latch-Up.

The HS-5104ARH, HS-5104AEH show almost no change in offset voltage after exposure to 100kRAD(Si) gamma radiation, with only a minor increase in current. Complementing these specifications is a post radiation open loop gain in excess of 40k.

These quad operational amplifiers are available in an industry standard pinout, allowing for immediate interchangeability with most other quad operational amplifiers.

Features

- Electrically screened to SMD # 5962-95690
- QML qualified per MIL-PRF-38535 requirements
- Radiation environment
  - High dose rate (50-300rad(Si)/s). . . . . 100krad(Si)
  - Low dose rate (0.01rad(Si)/s) . . . . . .50krad(Si)
- No latch-up, dielectrically isolated device islands
- Low noise
  - At 1kHz . . . . . .4.3nV/$\sqrt{Hz}$ (Typ)
  - At 1kHz . . . . . .0.6pA/$\sqrt{Hz}$ (Typ)
- Low offset voltage . . . . . .3.0mV (Max)
- High slew rate . . . . . 2.0V/µs (Typ)
- Gain bandwidth product . . . . . .8.0MHz (Typ)

Applications

- High Q, active filters
- Voltage regulators
- Integrators
- Signal generators
- Voltage references
- Space environment

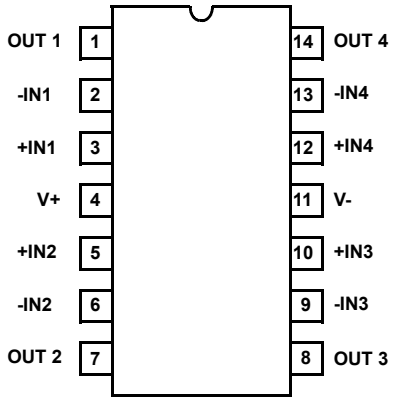
Ordering Information

ORDERING/SMD NUMBER	INTERNAL MKT. NUMBER (NOTE 1)	TEMP. RANGE (°C)	PART MARKING	PACKAGE (RoHS Compliant) (NOTE 2)	PKG. DWG. #
5962R9569001VXC	HS9-5104ARH-Q	-55 to +125	Q 5962R95 69001VXC	14 Ld Flatpack	K14.A
5962R9569002VXC	HS9-5104AEH-Q	-55 to +125	Q 5962R95 69002VXC	14 Ld Flatpack	K14.A
5962R9569001VCC	HS1-5104ARH-Q	-55 to +125	Q 5962R95 69001VCC	14 Ld SBDIP	D14.3
5962R9569002VCC	HS1-5104AEH-Q	-55 to +125	Q 5962R95 69002VCC	14 Ld SBDIP	D14.3
5962R9569001V9A	HS0-5104ARH-Q	-55 to +125		Die	
5962R9569002V9A	HS0-5104AEH-Q	-55 to +125		Die	
HS1-5104ARH/PROTO	HS1-5104ARH/PROTO	-55 to +125	HS1-5104ARH/PROTO	14 Ld SBDIP	D14.3
HS0-5104ARH/SAMPLE	HS0-5104ARH/SAMPLE	-55 to +125		Die	
HS9-5104ARH/PROTO	HS9-5104ARH/PROTO	-55 to +125	HS9-5104ARH/PROTO	14 Ld Flatpack	K14.A

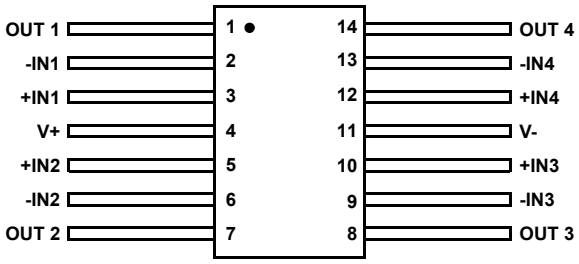
1. Specifications for Rad Hard QML devices are controlled by the Defense Logistics Agency Land and Maritime (DLA). The SMD numbers listed in the“Ordering Information” table must be used when ordering.
2. These Intersil Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.

Pin Configuration

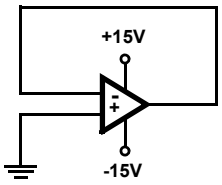
HS1-5104ARH, HS1-5104AEH
(14 LD SBDIP)
TOP VIEW



HS9-5104ARH, HS9-5104AEH
(14 LD FLATPACK)
TOP VIEW



Irradiation Circuit

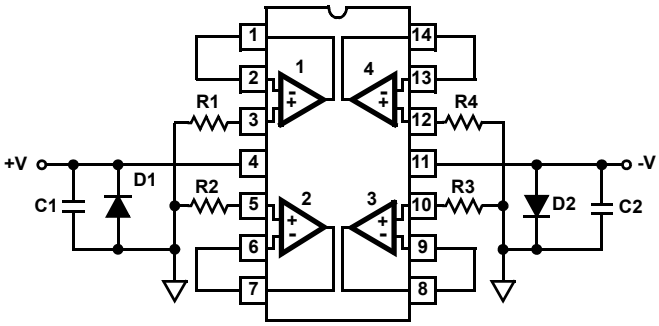


(ONE OF FOUR)

NOTES:

3. +V = 15V
4. -V = -15V
5. Group E Sample Size = 4 Die Per Wafer

Burn In Circuit



NOTES:

6. R1 = R2 = R3 = R4 = 1MW, 5%, 1/4W (Min)
7. C1 = C2 = 0.01µF/Socket (Min) or 0.1µF/Row (Min)
8. D1 = D2 = IN4002 or Equivalent/Board
9. |(V+) - (V-)| = 31V ±1V

Die Characteristics

DIE DIMENSIONS:

95 mils x 99 mils x 19 mils ±1 mils
(2420µm x 2530µm x 483µm ±25.4µm)

INTERFACE MATERIALS:

Glassivation:

Type: Nitride (SI3N4) over Silox (SIO2, 5% Phos.)
Silox Thickness: 12kÅ ±2kÅ
Nitride Thickness: 3.5kÅ ±1.5kÅ

Top Metallization:

Type: Al, 1% Cu
Thickness: 16kÅ ±2kÅ

Substrate:

Bipolar Dielectric Isolation

Backside Finish:

Silicon

ASSEMBLY RELATED INFORMATION:

Substrate Potential (Powered Up):

Unbiased

ADDITIONAL INFORMATION:

Worst Case Current Density:

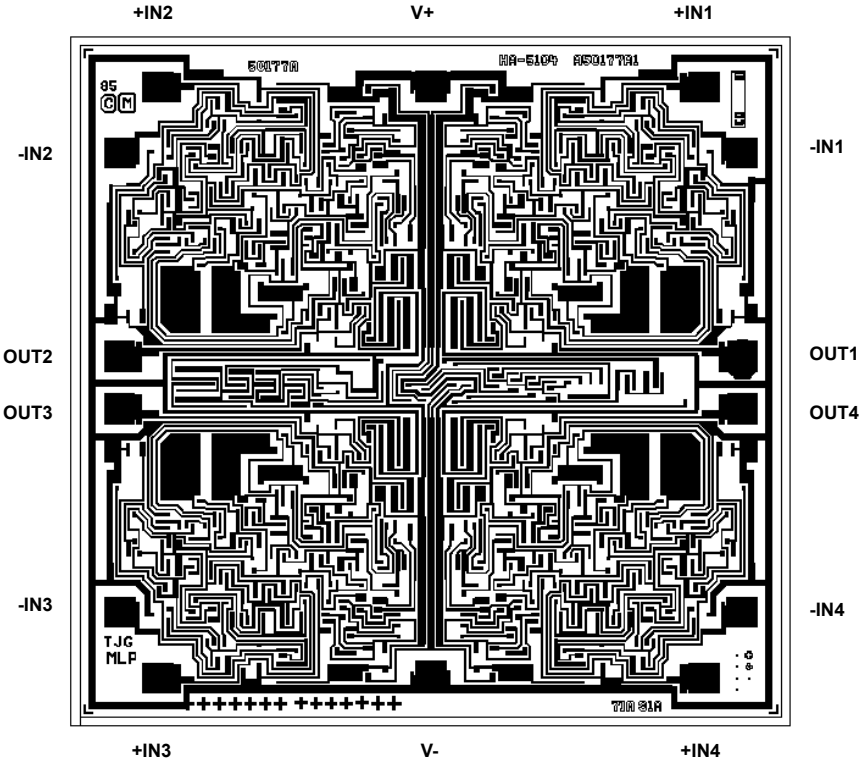
$< 2.0 \times 10^5$ A/cm^2

Transistor Count:

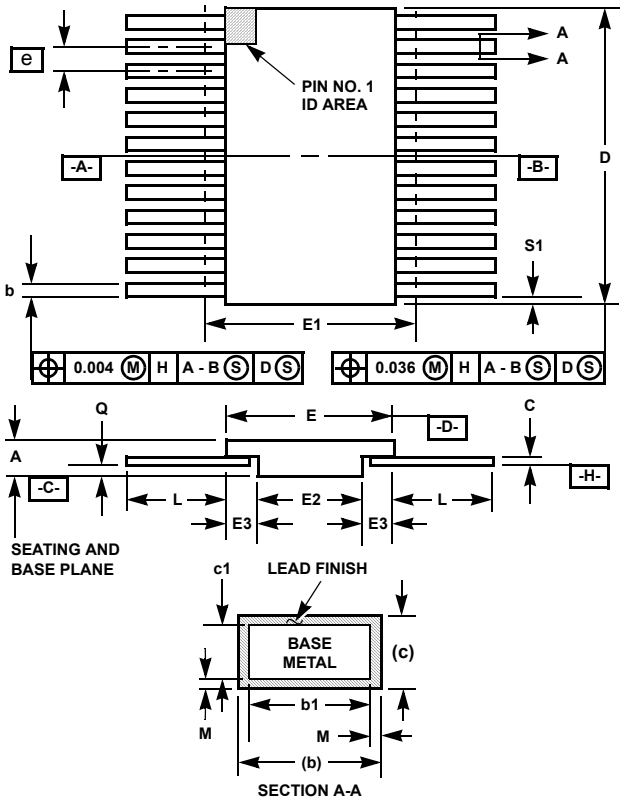
175

Metallization Mask Layout

HS-5104ARH, HS-5104AEH



Ceramic Metal Seal Flatpack Packages (Flatpack)



K14.A MIL-STD-1835 CDFP3-F14 (F-2A, CONFIGURATION B)
14 LEAD CERAMIC METAL SEAL FLATPACK PACKAGE

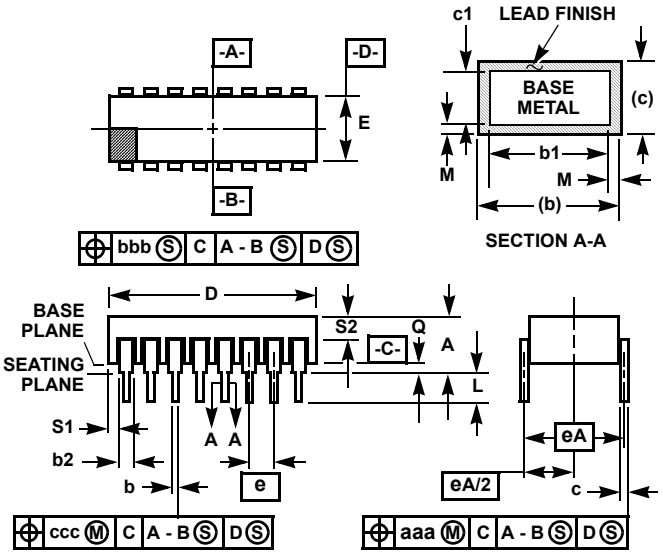
SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	0.045	0.115	1.14	2.92	-
b	0.015	0.022	0.38	0.56	-
b1	0.015	0.019	0.38	0.48	-
c	0.004	0.009	0.10	0.23	-
c1	0.004	0.006	0.10	0.15	-
D	-	0.390	-	9.91	3
E	0.235	0.260	5.97	6.60	-
E1	-	0.290	-	7.11	3
E2	0.125	-	3.18	-	-
E3	0.030	-	0.76	-	7
e	0.050 BSC		1.27 BSC		-
k	0.008	0.015	0.20	0.38	2
L	0.270	0.370	6.86	9.40	-
Q	0.026	0.045	0.66	1.14	8
S1	0.005	-	0.13	-	6
M	-	0.0015	-	0.04	-
N	14		14		-

Rev. 0 5/18/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark. Alternately, a tab (dimension k) may be used to identify pin one.
2. If a pin one identification mark is used in addition to a tab, the limits of dimension k do not apply.
3. This dimension allows for off-center lid, meniscus, and glass overrun.
4. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
5. N is the maximum number of terminal positions.
6. Measure dimension S1 at all four corners.
7. For bottom-brazed lead packages, no organic or polymeric materials shall be molded to the bottom of the package to cover the leads.
8. Dimension Q shall be measured at the point of exit (beyond the meniscus) of the lead from the body. Dimension Q minimum shall be reduced by 0.0015 inch (0.038mm) maximum when solder dip lead finish is applied.
9. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
10. Controlling dimension: INCH.

Ceramic Dual-In-Line Metal Seal Packages (SBDIP)



D14.3 MIL-STD-1835 CDIP2-T14 (D-1, CONFIGURATION C)
14 LEAD CERAMIC DUAL-IN-LINE METAL SEAL PACKAGE

SYMBOL	INCHES		MILLIMETERS		NOTES
	MIN	MAX	MIN	MAX	
A	-	0.200	-	5.08	-
b	0.014	0.026	0.36	0.66	2
b1	0.014	0.023	0.36	0.58	3
b2	0.045	0.065	1.14	1.65	-
b3	0.023	0.045	0.58	1.14	4
c	0.008	0.018	0.20	0.46	2
c1	0.008	0.015	0.20	0.38	3
D	-	0.785	-	19.94	-
E	0.220	0.310	5.59	7.87	-
e	0.100 BSC		2.54 BSC		-
eA	0.300 BSC		7.62 BSC		-
eA/2	0.150 BSC		3.81 BSC		-
L	0.125	0.200	3.18	5.08	-
Q	0.015	0.060	0.38	1.52	5
S1	0.005	-	0.13	-	6
S2	0.005	-	0.13	-	7
α	90^o	105^o	90^o	105^o	-
aaa	-	0.015	-	0.38	-
bbb	-	0.030	-	0.76	-
ccc	-	0.010	-	0.25	-
M	-	0.0015	-	0.038	2
N	14		14		8

Rev. 0 4/94

NOTES:

1. Index area: A notch or a pin one identification mark shall be located adjacent to pin one and shall be located within the shaded area shown. The manufacturer's identification shall not be used as a pin one identification mark.
2. The maximum limits of lead dimensions b and c or M shall be measured at the centroid of the finished lead surfaces, when solder dip or tin plate lead finish is applied.
3. Dimensions b1 and c1 apply to lead base metal only. Dimension M applies to lead plating and finish thickness.
4. Corner leads (1, N, N/2, and N/2+1) may be configured with a partial lead paddle. For this configuration dimension b3 replaces dimension b2.
5. Dimension Q shall be measured from the seating plane to the base plane.
6. Measure dimension S1 at all four corners.
7. Measure dimension S2 from the top of the ceramic body to the nearest metallization or lead.
8. N is the maximum number of terminal positions.
9. Braze fillets shall be concave.
10. Dimensioning and tolerancing per ANSI Y14.5M - 1982.
11. Controlling dimension: INCH.