

Recommended Test Procedures for Analog Switches

The following text describes the basic test procedures that can be used for most Intersil CMOS switches. Various test conditions are used with the various switches. Table 1 has been included to help define the specific test setups to be used with each variety of switch. One additional note, all schematics assume an open switch for high logic inputs (i.e., NC).

DC Switch Parameters

+V_S, -V_S: ANALOG SIGNAL RANGE

The analog signal range is the maximum input signal level which can be switched to the output with minimal distortion. For supply voltages lower than nominal, the analog signal range should be restricted to the voltage span between the supplies. Note that other parameters, such as “ON” resistance and leakage currents, are guaranteed over a smaller input range and tend to degrade toward the analog limits (+V_S and -V_S). Intersil switches can tolerate the positive analog signal limit (+V_S) applied to one side of a switch cell while the negative analog signal limit (-V_S) is applied to the other side (the switch must be open to avoid excessive currents).

The analog signal range is measured (Figure 1) by increasing an input waveform until the output shows evidence of distortion or the maximum analog level is reached (as stated in the maximum ratings section of the data sheet).

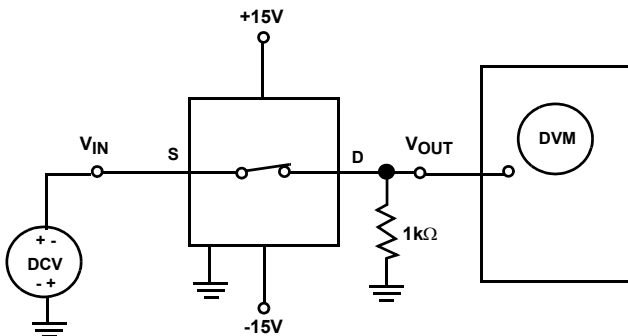
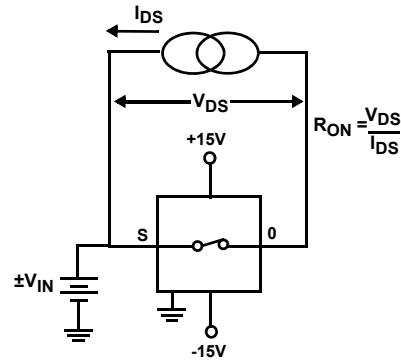


FIGURE 1. SUGGESTED CIRCUIT TO DETERMINE ANALOG SIGNAL RANGE

R_{ON}: ON RESISTANCE

“ON” resistance is the effective series on-switch resistance measured from input to output under specified conditions. Note that R_{ON} typically changes with temperature (highest at high temperature), and to a lesser degree with signal voltage and current.

R_{ON} is calculated from the voltage drop across a switch with a known current flow as in Figure 2.

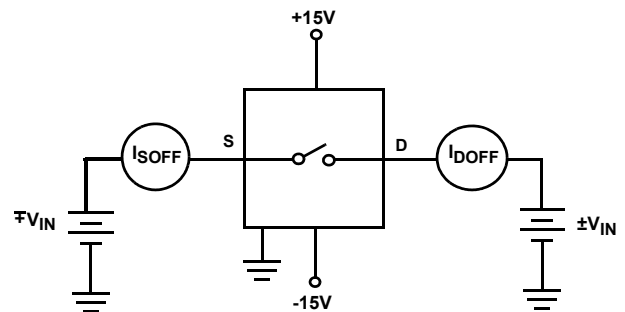


SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS
FIGURE 2. “ON” RESISTANCE TEST CIRCUIT

I_{S(OFF)}, I_{D(OFF)}, I_{D(ON)}: LEAKAGE CURRENTS

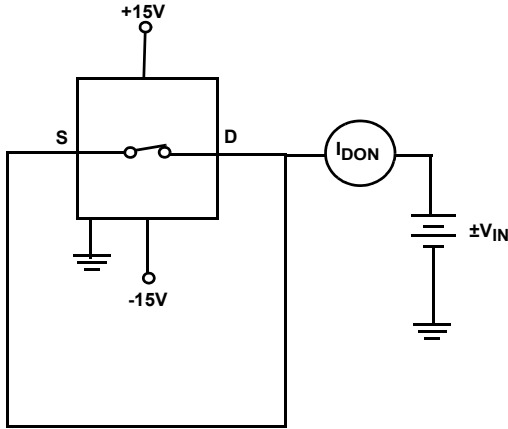
Intersil prefers to guarantee only worst case high temperature leakage currents because the room temperature picoampere levels are virtually impossible to measure repeatedly on currently available automated test equipment. Even under laboratory conditions, fixture and test equipment leakage currents may frequently exceed the device leakage currents. Since the leakage currents tend to double for every 10°C increase in temperature, it is reasonable to assume that the +25°C value is about 1/1000 the +125°C value; however, in some cases there may be ohmic leakage paths, such as across the package, which would tend to make the +25°C reading slightly higher than expected.

I_{S(OFF)}, measured directly with the circuit in Figure 3, consists largely of the diode leakage current from the source-body junction. I_{D(OFF)}, also measured directly with the circuit in Figure 3, is largely due to the diode leakage current in the drain-body junction.



SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS
FIGURE 3. OFF LEAKAGE CURRENT TEST CIRCUIT

“ON” leakage current ($I_{D(ON)}$) is the current flowing through both the source-body and drain-body junctions of a closed switch. $I_{D(ON)}$ tends to have the most noticeable effect since it creates an offset voltage across the switch equal to $I_{D(ON)} \cdot R_{ON}$. $I_{D(ON)}$ is measured directly with the circuit in Figure 4.



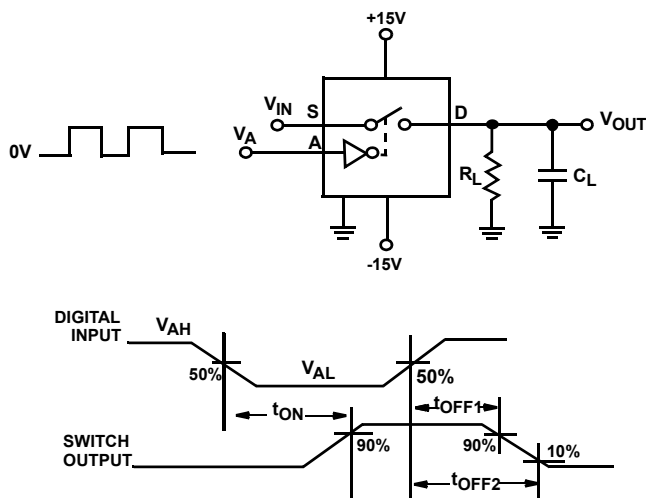
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS
FIGURE 4. “ON” LEAKAGE CURRENT TEST CIRCUIT

Dynamic Switch Parameters

t_{ON} , t_{OFF} : ACCESS TIME

Switch “Turn On” time t_{ON} is the time required to activate an “OFF” switch to an “ON” state. t_{ON} is measured from the 50% point of the logic transition to the 90% point of the output transition (Figure 5).

Switch “Turn Off” time t_{OFF} is the time required to deactivate an “ON” switch to an “OFF” state. t_{OFF} is measured from the 50% point of the logic transition to either the 90% point or 10% point (Figure 5).



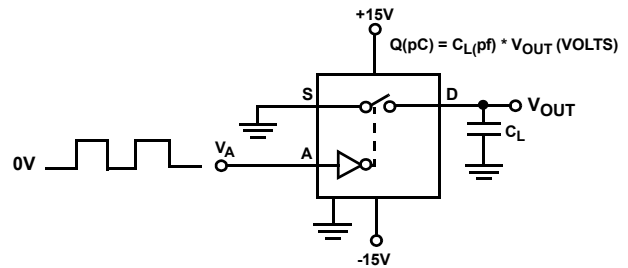
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 5. “TURN ON” AND “TURN OFF” DELAY TEST CIRCUIT AND WAVEFORMS

CHARGE INJECTION

Cycling a switch “ON” or “OFF” results in a small amount of charge being injected into the analog signal path. This charge injection is generated through the capacitive coupling between the digital control lines and the analog outputs. The ensuing voltage spikes create an acquisition interval during which the output level is invalid even when little or no steady state level change is involved. The total net energy (charge injection) coupled onto the analog lines is especially critical when switching voltage to a capacitor since the injection charge will change the capacitor voltage at the instant of switching.

Charge injection, measured in pico-coulombs, is measured with the aid of the circuit in Figure 6.

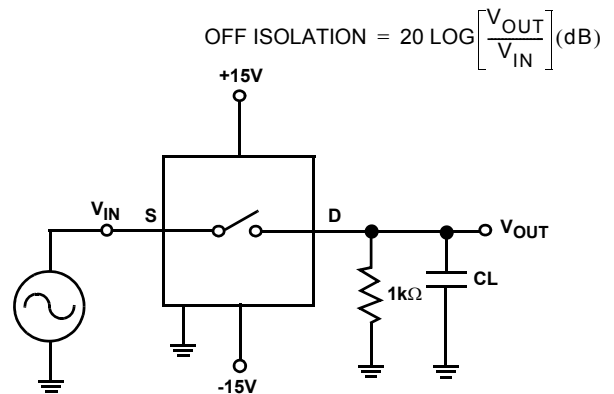


SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 6. CHARGE INJECTION TEST CIRCUIT

OFF ISOLATION

Off isolation is the degree of attenuation seen at the output of an “Open” switch when a high frequency signal is applied to the input. This feed through occurs through the source-body and drain-body capacitances and has a greater effect at higher frequencies. Off isolation is usually specified in decibels where $\text{Off Isolation} = 20 \log(V_{OUT}/V_{IN})$, see Figure 7. The isolation generally decreases by 10dB/decade with increasing frequency.

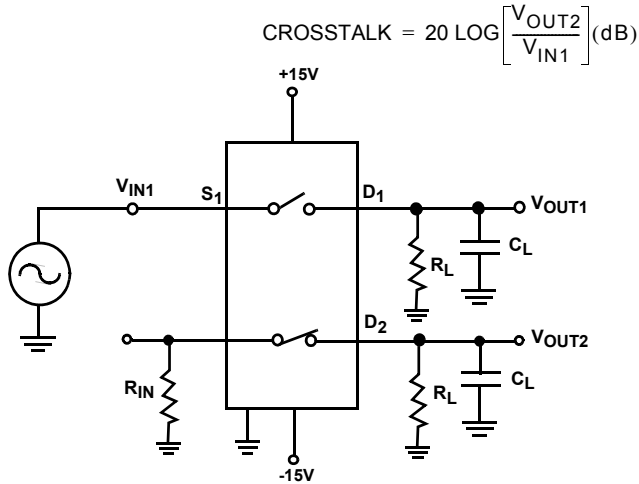


SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 7. OFF ISOLATION TEST CIRCUIT

CROSSTALK

Crosstalk is the amount of signal cross coupling from an “OFF” analog input to the output of another “ON” channel output. Crosstalk is usually measured in decibels where: $\text{Crosstalk} = 20\text{Log}(V_{\text{OUT}2}/V_{\text{OUT}1})$, see Figure 8.

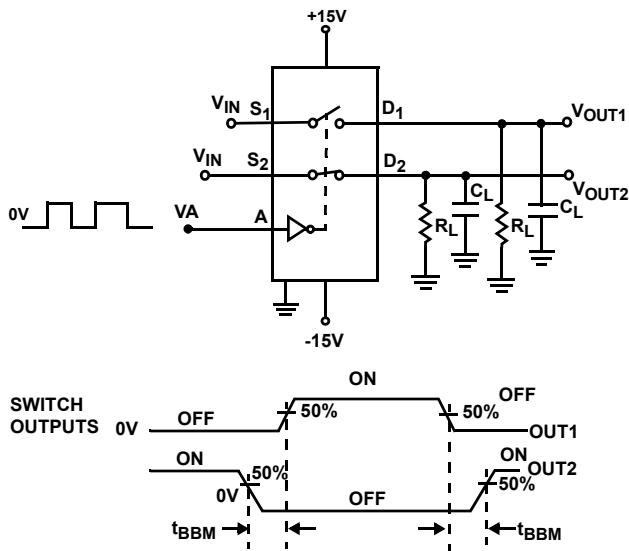


SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 8. GENERAL CROSSTALK TEST CIRCUIT

T_(BBM): BREAK-BEFORE-MAKE-DELAY

The break-before-make-delay $T_{(BBM)}$ is the elapsed time between the “Turn Off” of one switch and the corresponding “Turn On” of another for a common change in logic states (Figure 9). The delay measurement is taken at the 50% levels of the output transitions. The $T_{(BBM)}$ delay prevents the switches from being simultaneously closed during switching transitions.



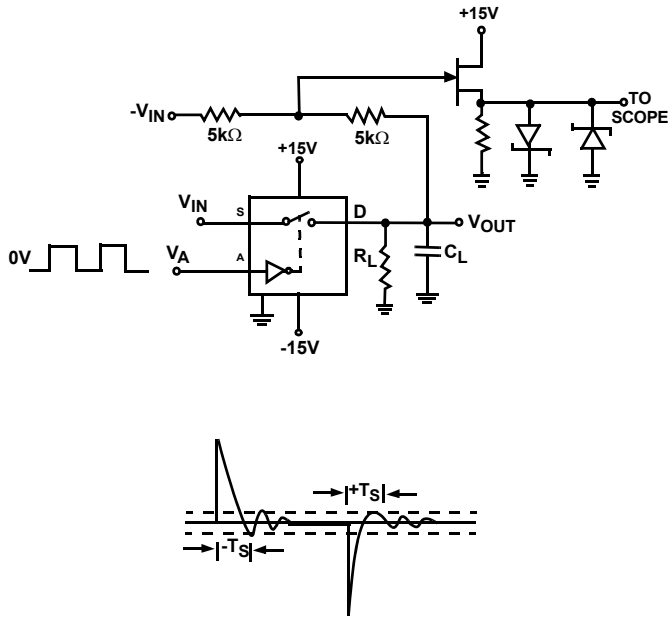
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 9. BREAK-BEFORE-MAKE-DELAY TEST CIRCUIT AND WAVEFORMS

SETTING TIME

Setting time is the time required for the switch output to settle within a given percentage of the final value following a change in the digital input level. Usually the worst-case settling time occurs when the switch is required to slew across its full dynamic range (generally a 0V to +10V transition). This is known as full-scale settling time.

The settling time circuit, Figure 10, employs two resistors to generate an error voltage equal to the output error. A FET is used to buffer the summing junction from the oscilloscope probe capacitance.



SETTLING TIME (T_S) IS MEASURED USING A HIGH SPEED RECOVERY OSCILLOSCOPE TO DISPLAY THE ERROR VOLTAGE V_E .

SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 10. SETTLING TIME TEST CIRCUIT AND WAVEFORM

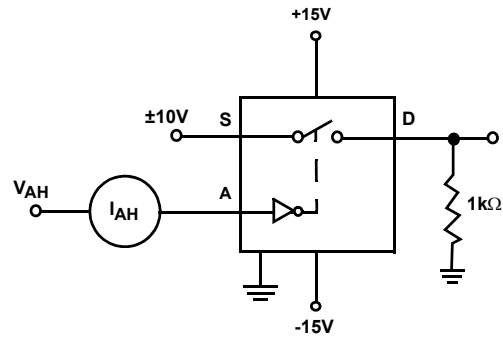
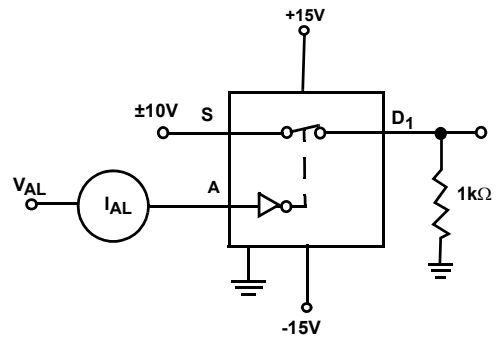
Switch Logic Parameters

V_{AL} , V_{AH} : INPUT THRESHOLDS

The input thresholds are the digital input upper and lower limits at which proper switching action is guaranteed to take place. The input low threshold V_{AL} is the maximum allowable voltage that can be applied to the digital input and still be recognized as a logic low ("0") input. The input high threshold V_{AH} is the minimum allowable voltage that can be applied to the digital input and still be recognized as a logic high ("1") input. All other parameters will be valid if the logic inputs are either below V_{AL} or above V_{AH} .

I_{AL} , I_{AH} : INPUT LEAKAGE CURRENT

Input leakage current is the bias current flowing either into or out of the digital input terminal. Input leakage current high (I_{AH}) is the current flowing while the digital input is in the high state ($\geq V_{AH}$), while input leakage current low (I_{AL}) is the current flowing when the digital input is in the low state ($\leq V_{AL}$). Input leakage currents are measured directly using the circuits in Figure 11.



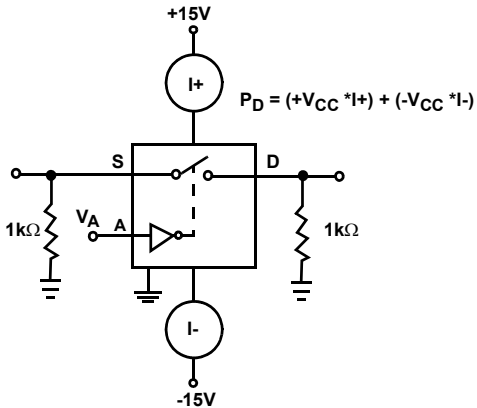
SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 11. INPUT LEAKAGE CURRENT TEST CIRCUITS

Static and Package Related Switch Parameters

I+, I-, P_D: POWER DISSIPATION

Quiescent power dissipation $P_D = (+V_{CC} * I_+) + (-V_{CC} * I_-)$ (Figure 12). P_D may be specified with the switch in either a cycling or a steady state condition. Note that, as with all CMOS devices, power dissipation increases with switching frequency.



SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS
FIGURE 12. SUPPLY CURRENT TEST CIRCUIT

C_{S(OFF)}, C_{D(OFF)}, C_{D(ON)}, C_{DS(OFF)}, C_A: SWITCH CAPACITANCE

The various switch capacitances are stated as typical values. These values are given by design and are not subject to production testing (Figure 13).

Capacitance Source-Off $C_{S(OFF)}$ is the capacitance with respect to ground seen at the analog input with the switch open. This capacitance is the sum of the source capacitance of the N-channel and P-channel switching devices.

$$C_{S(OFF)} = C_{SGP1} + C_{SBP1} + C_{SGN} + C_{SBN}$$

Capacitance Drain-Off $C_{D(OFF)}$ is the capacitance with respect to ground seen at the output terminal with the switch open. This capacitance is the sum of the drain capacitance of the N-channel and P-channel switching devices.

$$C_{D(OFF)} = C_{DGP1} + C_{DBP1} + C_{DGN} + C_{DBN}$$

Capacitance Drain-On $C_{D(ON)}$ is the capacitance with respect to ground at the drain with the switch closed. Generally $C_{D(ON)}$ is the total of the source-off and drain-off capacitances.

$$C_{D(ON)} = C_{D(OFF)} + C_{S(OFF)}$$

Input to output capacitance $C_{DS(OFF)}$ is the capacitance between the analog input and output with the switch open.

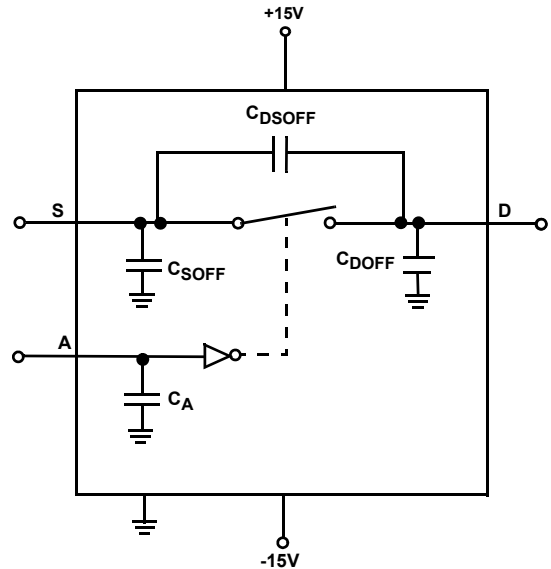
Digital input capacitance C_A is the capacitance with respect to ground at the digital input. C_A chiefly affects propagation delays when the switch is driven by CMOS logic.

Switch Test Fixture Design Rules

The high performance characteristics of Intersil switches require high quality test fixtures for accurate characterization. The following design rules should eliminate most sources of error and provide highly accurate results.

- Decoupling capacitors should be placed as close to the supply pins as possible.
- A ground plane should be used to minimize distributed capacitance.
- All grounds should terminate at a single point ground.
- All sensitive analog lines should be routed between ground traces and kept away from digital lines.
- Analog and digital lines should cross at right angles.
- All unused logic pins should be connected to either V_{AL} or V_{AH} .

- All unused analog pins should be connected to ground through a $1k\Omega$ resistor.
- Teflon sockets should be used to minimize socket capacitance.



SEE TABLE 1 FOR SPECIFIC TEST CONDITIONS

FIGURE 13. EQUIVALENT SWITCH CIRCUIT INCLUDING CAPACITANCES

TABLE 1. TEST CONDITIONS FOR "HI" TYPE SWITCHES

	LOGIC LEVELS	LOGIC REFERENCE	R _{ON}	I _S , I _D	t _{ON} , t _{OFF}	CHARGE INJECTION	CROSSTALK	OFF ISOLATION	SETTLING TIME	BREAK-BEFORE-MAKE	I _{AL} , I _{AH}	POWER DISSIPATION
HI-200	V _{AL} = 0.8V V _{AH} = 2.4V	V _{REF} OPEN	V _{IN} = +10V I _{DS} = 1mA	V _{IN} = +14V	V _{IN} = +10V R _L = 1kΩ C _L = 35pF V _A = 0V, 4V			V _{IN} = 3V _{RMS} f = 100kHz R _L = 1kΩ C _L = 10pF V _A = 5V, 0V		V _{AL} = 0V V _{AH} = 4V	V _{AL} min = 0V V _{AH} max = 5V	V _A = 0V or V _A = 3V
HI-201	V _{AL} = 0.8V V _{AH} = 2.4V	V _{REF} OPEN	V _{IN} = +10V I _{DS} = 1mA	V _{IN} = +14V	V _{IN} = +10V V _A = 0V, 4V R _L = 1kΩ C _L = 35pF			V _{IN} = 3V _{RMS} f = 100kHz R _L = 1kΩ C _L = 10pF V _A = 5V, 0V		V _{AL} = 0V V _{AH} = 4V	V _{AL} min = 0V V _{AH} max = 5V	V _A = 0V or V _A = 3V
HI-201HS	V _{AL} = 0.8V V _{AH} = 3.0V		V _{IN} = +10V I _{DS} = 1mA	V _{IN} = +14V	V _{IN} = +10V R _L = 1kΩ C _L = 35pF V _A = 3V, 0V	C = 1000pF	V _{IN} = 3V _{RMS} f = 100kHz R _L = 1kΩ V _A = 3V, 0V R _{IN} = 1kΩ	V _{IN} = 3V _{RMS} f = 100kHz R _L = 1kΩ C _L = 10pF V _A = 3V, 0V	V _{IN} = +10V R _L = 1kΩ C _L = 35pF V _A = 3V, 0V		V _{AL} min = 0V V _{AH} max = 5V	V _A = 0V or V _A = 3V
HI-303	V _{AL} = 0.8V V _{AH} = 4.0V		V _{IN} = +10V I _{DS} = 10mA	V _{IN} = +14V	V _{IN} = +3V R _L = 300Ω C _L = 33pF V _A = 4V, 0V	C = 10000pF V _A = 5.0V		V _{IN} = 1V _{RMS} f = 500kHz R _L = 1kΩ C _L = 15pF		V _{AL} = 0V V _{AH} = 5V R _L = 300Ω C _L = 33pF V _{IN} = +3V	V _{AL} min = 0V V _{AH} max = 5V	V _A = 0.8V or V _A = 4.0V
HI-307	V _{AL} = 3.5V		V _{IN} = +10V I _{DS} = 10mA	V _{IN} = +14V	V _{IN} = +3V R _L = 300Ω C _L = 33pF V _A = 5V, 0V	C = 10000pF V _A = 5.0V		V _{IN} = 1V _{RMS} f = 500kHz R _L = 1kΩ C _L = 15pF		V _{AL} = 0V V _{AH} = 5V R _L = 300Ω C _L = 33pF V _{IN} = +3V	V _{AL} min = 0V V _{AH} max = 15V	V _A = 0V or V _A = 15V
HI-390	V _{AL} = 0.8V V _{AH} = 4.0V		V _{IN} = +10V I _{DS} = 10mA	V _{IN} = +14V	V _{IN} = +3V R _L = 300Ω C _L = 33pF V _A = 5V, 0V	C = 10000pF V _A = 5.0V		V _{IN} = 1V _{RMS} f = 500kHz R _L = 1kΩ C _L = 15pF		V _{AL} = 0V V _{AH} = 5V R _L = 300Ω C _L = 33pF V _{IN} = +3V	V _{AL} min = 0V V _{AH} max = 5V	V _A = 0.8V or V _A = 4.0V
HI-5042 Thru HI-5051	V _{AL} = 0.8V V _{AH} = 3.0V	V _L = 5V V _R = 0V	V _{IN} = +10V I _{DS} = 1mA	V _{IN} = +10V	V _{IN} = +10V R _L = 1kΩ	C = 10000pF	V _{IN} = 2V _{P-P} f = 100kHz R _L = 100Ω C _L = 15pF R _{IN} = 0Ω	V _{IN} = 2V _{P-P} f = 100kHz R _L = 100Ω C _L = 15pF			V _{AL} min = 0V V _{AH} max = 5V	V _A = 0V or V _A = 3.0V

Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.
2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other claims involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or technical information described in this document, including but not limited to, the product data, drawings, charts, programs, algorithms, and application examples.
3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.
4. You shall not alter, modify, copy, or reverse engineer any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copying or reverse engineering.
5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.
"Standard": Computers; office equipment; communications equipment; test and measurement equipment; audio and visual equipment; home electronic appliances; machine tools; personal electronic equipment; industrial robots; etc.
"High Quality": Transportation equipment (automobiles, trains, ships, etc.); traffic control (traffic lights); large-scale communication equipment; key financial terminal systems; safety control equipment; etc.
Unless expressly designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not intended or authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems; surgical implantations; etc.), or may cause serious property damage (space system; undersea repeaters; nuclear power control systems; aircraft control systems; key plant systems; military equipment; etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or any third parties arising from the use of any Renesas Electronics product that is inconsistent with any Renesas Electronics data sheet, user's manual or other Renesas Electronics document.
6. When using Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat dissipation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions, failure or accident arising out of the use of Renesas Electronics products outside of such specified ranges.
7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics, such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Unless designated as a high reliability product or a product for harsh environments in a Renesas Electronics data sheet or other Renesas Electronics document, Renesas Electronics products are not subject to radiation resistance design. You are responsible for implementing safety measures to guard against the possibility of bodily injury, injury or damage caused by fire, and/or danger to the public in the event of a failure or malfunction of Renesas Electronics products, such as safety design for hardware and software, including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures. Because the evaluation of microcomputer software alone is very difficult and impractical, you are responsible for evaluating the safety of the final products or systems manufactured by you.
8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. You are responsible for carefully and sufficiently investigating applicable laws and regulations that regulate the inclusion or use of controlled substances, including without limitation, the EU RoHS Directive, and using Renesas Electronics products in compliance with all these applicable laws and regulations. Renesas Electronics disclaims any and all liability for damages or losses occurring as a result of your noncompliance with applicable laws and regulations.
9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall comply with any applicable export control laws and regulations promulgated and administered by the governments of any countries asserting jurisdiction over the parties or transactions.
10. It is the responsibility of the buyer or distributor of Renesas Electronics products, or any other party who distributes, disposes of, or otherwise sells or transfers the product to a third party, to notify such third party in advance of the contents and conditions set forth in this document.
11. This document shall not be reprinted, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.
12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.
(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its directly or indirectly controlled subsidiaries.
(Note 2) "Renesas Electronics product(s)" means any product developed or manufactured by or for Renesas Electronics.

(Rev.4.0-1 November 2017)



SALES OFFICES

Renesas Electronics Corporation

<http://www.renesas.com>

Refer to "<http://www.renesas.com/>" for the latest and detailed information.

Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338