

DC/DC Modules

Splitting an LVDS Signal to Drive Two Receivers from a Single Transmitter

AN1787

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FIGURE 1. DUAL LCD SCREEN DRIVEN BY A COMMON VIDEO SIGNAL

Overview

There are applications where a single data source needs to send LVDS data to two destinations. An example of this is a single video source sending data to two LCD panels as might be found in an automotive rear seat entertainment system. Traditionally SERDES links are point to point, a single transmitter sending serial data across a cable or circuit board to a single receiver. If a system requires that the same data be sent to two destinations, two complete links (4 x SERDES chips and 2 cables) would be required. An example of this is shown in Figure 1. The displays are shown close together for the convenience of the picture but then could be a meter or more apart in an end application.

Objective

Propose a technique that allows a system designer to split an LVDS cable so that a single ISL76341 or ISL76321 transmitter can drive two receivers. This eliminates one SERDES chip from the BOM and shortens the total cable length in the system.

Maintaining a 100Ω differential impedance environment throughout the entire data path is essential to eliminate reflections and maintain the common mode voltage.

Since this is a cost reduction standard circuit board, design techniques must be utilized.

Splitter Design

To accomplish the objectives a single board needs to be added to the system to split the LVDS signal into two identical signals. While some signal loss is expected we want to keep it to a minimum. Signal integrity must be maintained so there is no increase in EMI. The splitter board schematic is shown in Figure 2.

Each transmitter and receiver has an impedance of 100Ω. Analyzing the upper branch we start with that 100Ω. When we add R3 and R4 the impedance of that branch is 133Ω. The two receiver branches in parallel have an impedance of 66.5Ω. Last we add the 33Ω from the two series resistors from the transmit branch, R1 and R2 for a total of 99.5Ω as seen from the transmitter output. The analysis is the same for each of the branches so each SERDES chip see a 100Ω load. The six 16.5Ω resistors are standard 1% SMT values. These resistors pass very little current so any size SMT resistors can be used.

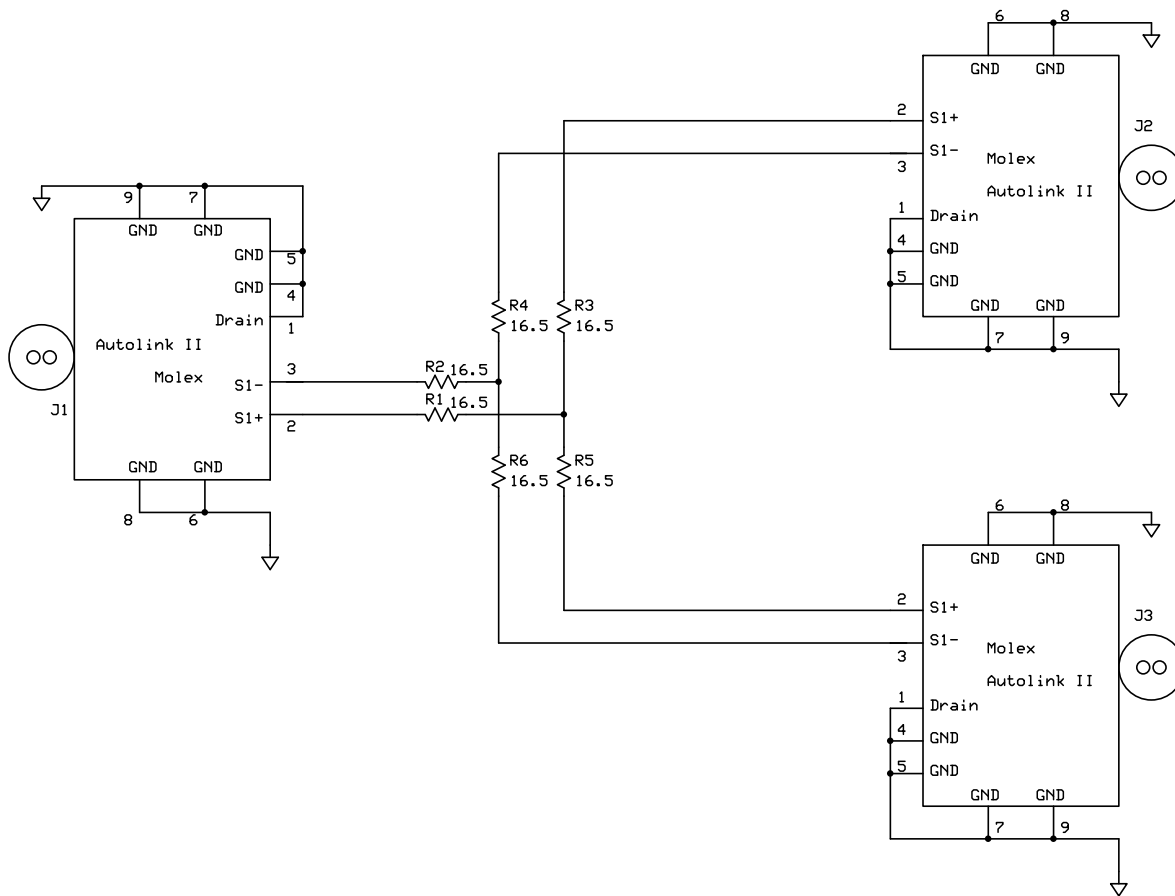


FIGURE 2. LVDS SPLITTER SCHEMATIC

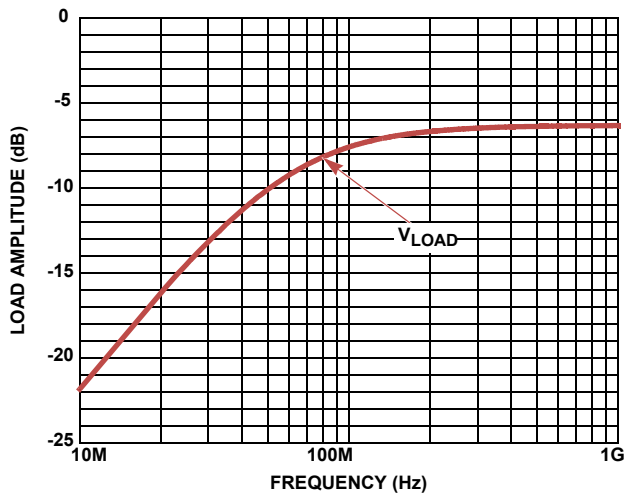


FIGURE 3. RECEIVER AMPLITUDE NORMALIZED TO THE TRANSMITTER

Figure 3 shows the simulated amplitude at the receiver termination resistor. As expected roughly half of the transmitted is available at each load. The roll off at lower frequencies is due to DC blocking capacitors on the transmitter board, which are required. See the appropriate SERDES datasheet for additional details.

Circuit Board Design

The splitter can be implemented in a 2- or 4-layer board design. The critical piece is maintaining a 50Ω single-ended and 100Ω differential transmission line environment. What makes this somewhat challenging is the fact that at least one pair will need to go from the top layer to the bottom layer of the board since the signals need to cross. With a 4-layer board it is easier to maintain impedance control by using both internal layers as reference planes (GND) and the top and bottom layers for signals. The required vias in the signal path will add only a small amount of inductance and a small negligible change in the characteristic impedance.

Two Layer Board Design

There is no reason that the splitter cannot be implemented on a 2-layer board but impedance control is more difficult. One issue with a two layer board is maintaining a controlled impedance when the signal trace goes from the top of the board to the bottom. Changing the signal layer requires changing the reference plane in the opposite direction. Ground vias need to be added and placed as close to the signal vias as possible. This allows any return current to flow under the signal trace. An example is shown in Figure 4. Only 3 vias are used in this design but there is no problem using more. A string of vias every 2mm to 3mm on each side of the differential traces is a good solution.

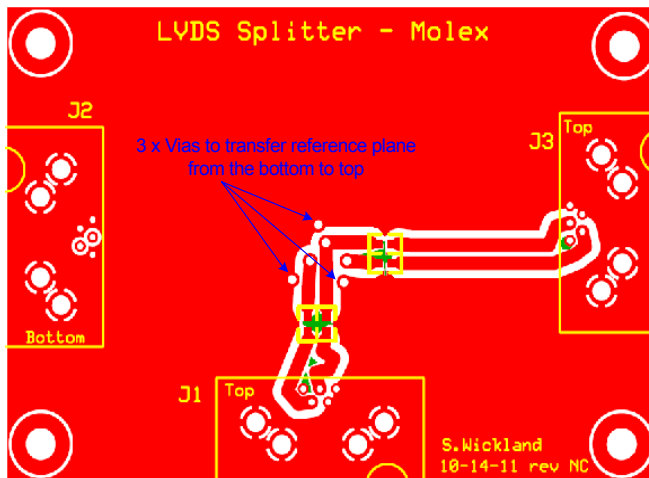


FIGURE 4. LVDS SPLITTER BOARD USING MOLEX AUTOLINKII CONNECTOR

Another issue with a 2-layer board is the distance from the signal trace to the reference plane. The board shown in Figure 4 is drawn with common layout rules for a 2-layer board. It is 62mils thick, which forces the signal traces to be 50mils wide with only 10mils separation from the differential partner. This spacing gets close to the design rule limits of some low cost PCB manufacturers.

Display Performance

The quality of the received video with a split signal depends on the signal frequency, the cable length and its quality. The longer the cable or the lower the quality of the cable, the smaller the amplitude of the signal that reaches the receiver. With a good splitter design, only half of the transmitted signal reaches the receiver. This means the maximum cable length of a split signal will be between 60% and 75% of a single display cable of the same length.

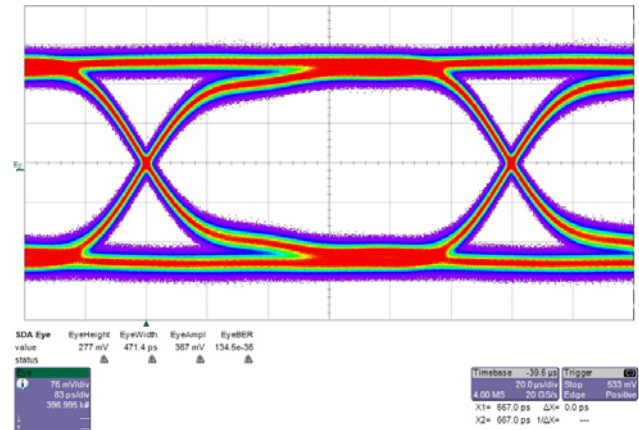


FIGURE 5. SPLITTER EYE WITH A PRBS²³ PATTERN CONNECTOR

Figure 5 shows the eye of the 2-layer board shown in Figure 4 with a 1GHz PRBS²³ pattern. The eye height is 277mV with the BERT output set to 600mV.

The Intersil SERDES is broadly adjustable with current drive, pre-emphasis and equalization. This gives the user maximum flexibility in compensating for cable and board losses, helping to facilitate this splitter scheme. With these adjustments, cable lengths greater than 10 meters are possible. The register details that enable programming these adjustments are available in the Technical Brief.

Related Documents

ISL3434X/32X Technical Brief

[ISL34321](#) 16-Bit Long-Reach Video SERDES with Bidirectional Side-Channel

[ISL34341](#) WSVGA 24-Bit Long-Reach Video SERDES with Bidirectional Side-Channel

[ISL76321](#) 16-Bit Long-Reach Video Automotive Grade SERDES with Bidirectional Side-Channel

[ISL76322](#) 16-Bit Long-Reach Video Automotive Grade SERDES

[ISL76341](#) 24-Bit Long-Reach Video Automotive Grade SERDES with Bidirectional Side-Channel

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Renesas Electronics America Inc.
1001 Murphy Ranch Road, Milpitas, CA 95035, U.S.A.
Tel: +1-408-432-8888, Fax: +1-408-434-5351

Renesas Electronics Canada Limited
9251 Yonge Street, Suite 8309 Richmond Hill, Ontario Canada L4C 9T3
Tel: +1-905-237-2004

Renesas Electronics Europe Limited
Dukes Meadow, Millboard Road, Bourne End, Buckinghamshire, SL8 5FH, U.K
Tel: +44-1628-651-700, Fax: +44-1628-651-804

Renesas Electronics Europe GmbH
Arcadiastrasse 10, 40472 Düsseldorf, Germany
Tel: +49-211-6503-0, Fax: +49-211-6503-1327

Renesas Electronics (China) Co., Ltd.
Room 1709 Quantum Plaza, No.27 ZhichunLu, Haidian District, Beijing, 100191 P. R. China
Tel: +86-10-8235-1155, Fax: +86-10-8235-7679

Renesas Electronics (Shanghai) Co., Ltd.
Unit 301, Tower A, Central Towers, 555 Langao Road, Putuo District, Shanghai, 200333 P. R. China
Tel: +86-21-2226-0888, Fax: +86-21-2226-0999

Renesas Electronics Hong Kong Limited
Unit 1601-1611, 16/F., Tower 2, Grand Century Place, 193 Prince Edward Road West, Mongkok, Kowloon, Hong Kong
Tel: +852-2265-6688, Fax: +852-2886-9022

Renesas Electronics Taiwan Co., Ltd.
13F, No. 363, Fu Shing North Road, Taipei 10543, Taiwan
Tel: +886-2-8175-9600, Fax: +886-2-8175-9670

Renesas Electronics Singapore Pte. Ltd.
80 Bendemeer Road, Unit #06-02 Hyflux Innovation Centre, Singapore 339949
Tel: +65-6213-0200, Fax: +65-6213-0300

Renesas Electronics Malaysia Sdn.Bhd.
Unit 1207, Block B, Menara Amcorp, Amcorp Trade Centre, No. 18, Jln Persiaran Barat, 46050 Petaling Jaya, Selangor Darul Ehsan, Malaysia
Tel: +60-3-7955-9390, Fax: +60-3-7955-9510

Renesas Electronics India Pvt. Ltd.
No.777C, 100 Feet Road, HAL 2nd Stage, Indiranagar, Bangalore 560 038, India
Tel: +91-80-67208700, Fax: +91-80-67208777

Renesas Electronics Korea Co., Ltd.
17F, KAMCO Yangjae Tower, 262, Gangnam-daero, Gangnam-gu, Seoul, 06265 Korea
Tel: +82-2-558-3737, Fax: +82-2-558-5338