

Reducing the Switching Frequency of the ISL8200M and ISL8200AM Power Modules

The ISL8200M and ISL8200AM power modules have a default nominal switching frequency of 700kHz. The datasheet describes two methods to increase the frequency up to 1.5MHz: 1) by tying a resistor (RFS) from the FSYNC\_IN pin to PGND, and 2) synchronizing to an external clock. There are also similar methods by which the switching frequency can be reduced.

Methods for Reducing the Switching Frequency

One option is to tie a resistor,  $R_{PULL-UP}$ , from FSYNC\_IN to a voltage supply higher than 1.2V and less than or equal to VCC, and a small capacitor, CFS, (in the 120pF to 150pF range) from FSYNC\_IN to ground (Figure 2). The concept is to “reduce” the resistor that the controller sees on the FSYNC\_IN pin by injecting a small amount of current into it with the capacitor acting as a small filter of the supply disturbance. Any variation in the supply will result in frequency variation. Figure 2 shows VCC as the supply to  $R_{PULLUP}$  because it is readily available from the module and is regulated.

The controller continuously senses the resistor value by measuring the internal current required to maintain the FSYNC\_IN pin voltage at 1.2V. The lower the resistor value, the higher the internal current needed, which results in higher switching frequency. Because additional current is injected from the external resistor tied to the external supply, the internal current becomes smaller. The controller acts as though a lower value resistor is connected to it, thereby reducing the switching frequency.

Figure 1 shows the change in switching frequency at various  $R_{PULL-UP}$  values for  $V_{IN}$  of 12V and 5V.  $C_{FS} = 150pF$  for these measurements.  $V_{OUT} = 3.3V$ , however, switching frequency is independent of output voltage.

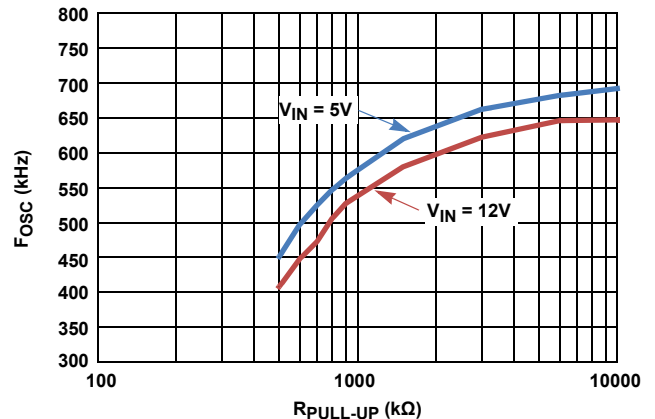


FIGURE 1.  $R_{PULL-UP}$  vs SWITCHING FREQUENCY

Another method to reduce the switching frequency is to synchronize to an external clock. While the datasheet states that the synchronization frequency is limited from  $F_{OSC}$  to 1.5MHz, where  $F_{OSC}$  is the nominal switching frequency of the internal oscillator, or 700kHz, the ISL8200M and ISL8200AM will actually synchronize to frequencies below  $F_{OSC}$ . The modules will synchronize to any external clock, including the clock from the ISL8225 power module (510kHz).

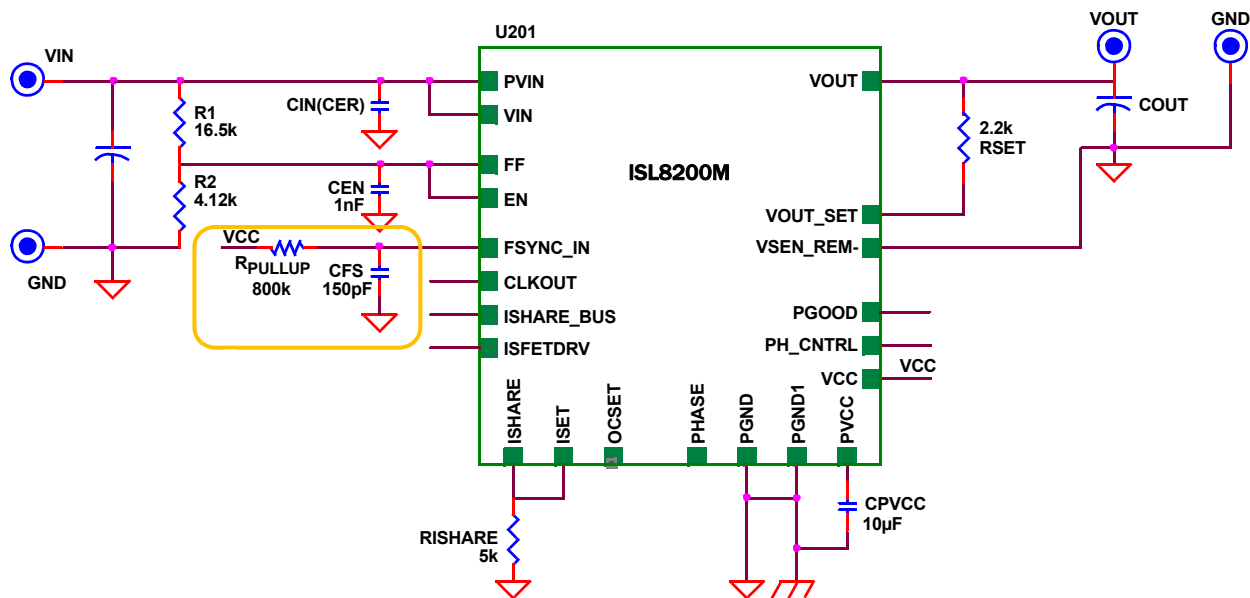


FIGURE 2. APPLICATIONS CIRCUIT FOR REDUCING  $F_{SW}$

## Reasons for Reducing the Switching Frequency

There may be several reasons why a designer might want to reduce the switching frequency of switching regulator and specifically the ISL8200M or ISL8200AM power module; increase efficiency, improve EMI, or to improve  $V_{IN}$  limitations. We will explore each of these to better understand the trade-offs.

### Increase Efficiency

Reducing the switching frequency is a common practice used to increase overall efficiency by reducing switching losses in the MOSFETs, reducing bias current to the IC and other components. However, at the same time doing so will increase inductor current ripple and consequently increase inductor core loss. For a given set of power stage components (MOSFETs, inductor), the optimal switching frequency for efficiency varies with input and output voltage conditions. In a power module, most of the components are internal to the module and fixed and it is possible that reducing the switching frequency will actually make efficiency worse depending on the conditions of the application.

Figures 3 and 4 show typical efficiency curves for  $V_{OUT} = 1.2V$  and  $3.3V$ , respectively, at  $V_{IN} = 5V$  and  $12V$  at both  $500kHz$  and  $700kHz$  switching frequencies. Under these conditions, it can be seen that efficiencies are generally improved at  $500kHz$ , but not under all conditions.

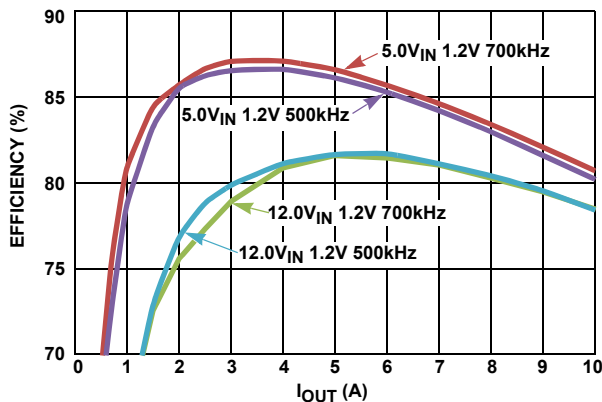


FIGURE 3. EFFICIENCY WITH  $V_{OUT} = 1.2$  AT  $V_{IN} = 5V$  AND  $12V$  AND  $F_{SW} = 700Hz$  AND  $500kHz$

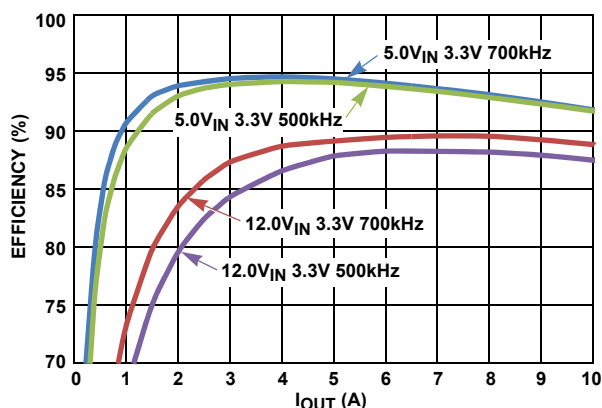


FIGURE 4. EFFICIENCY WITH  $V_{OUT} = 3.3$  AT  $V_{IN} = 5V$  AND  $12V$  AND  $F_{SW} = 700Hz$  AND  $500kHz$

### Noise/EMI Reduction

In some applications where noise sensitivity or in-band noise may be an issue, the system designer may want to avoid specific clock frequencies as they may be difficult or impossible to filter. Increasing the switching frequency is always an option, but this also has the tendency to increase overall EMI, so reducing the switching frequency may be desirable.

There may also be a system or master clock available to which the user may want to synchronize either for the reasons mentioned above, or to avoid having all the switching regulators free run. Free running clocks will periodically switch at the exact same time causing beat frequencies and increased noise.

Noise can be reduced further if each power module is synchronized to a phase shifted clock derived off the original master clock. The ISL8225M, ISL8200M and ISL8200AM, all have the capability of outputting clocks that are phase shifted by a programmable amount from the internal clock.

For example, if three power modules are used in a design, an optimum set up would be to have the master module output a  $120^\circ$  phase shifted clock to the second module. Similarly, the second module would again phase shift its clock  $120^\circ$  and output it to the third module. All three clocks are now  $120^\circ$  out-of-phase with each other.

There is also a side benefit in that the overall input capacitance can be reduced. This is because the phase shifted clocks will reduce the RMS input ripple current.

### Improve $V_{IN\_MIN}$ limitations

The ISL8200M and ISL8200AM have a worst case minimum PWM off time of  $410ns$ .  $V_{IN}$  is limited by this minimum off time. Equation 1 gives the formula for  $V_{IN\_MIN}$ .

$$V_{IN\_MIN} = \frac{V_{OUT} \times t_{SW}}{t_{SW} - t_{MIN\_OFF}} \quad (EQ. 1)$$

$$t_{SW} = \text{switching period} = 1/F_{SW}$$

Using an example of  $V_{OUT} = 3.3V$ ,  $t_{SW} = 1/700kHz = 1428ns$ ,  $V_{IN\_MIN} = 3.3V \times 1428 / (1428 - 410) = 4.63V$

If  $V_{IN} = 5V \pm 10\%$  or  $4.5V$  to  $5.5V$ , then we would not be able to use the ISL8200M or ISL8200AM for this application.

By reducing  $F_{SW}$ , or increasing  $t_{SW}$ , we can effectively reduce  $V_{IN\_MIN}$ . Using the ISL8225M output clock of  $510kHz$ , for example, yields:

$$V_{IN\_MIN} = 3.3 \times 1961 / (1961 - 410) = 4.17V$$

With  $V_{IN} = 5V \pm 10\%$ , we have sufficient margin operating at  $510kHz$ .

### Other Trade-Offs

As mentioned above, reducing the switching frequency of the ISL8200M or ISL8200AM power modules can result in system level improvements. Some trade-off considerations have been mentioned (possible reduction in efficiency, max off-time issues.) but there are a few more that need to be considered.

The first consideration is that any decrease in switching frequency will increase output ripple current and subsequently the output ripple voltage.

The output ripple current equation is given by Equation 2. As can be seen, any reduction in L will result in an increase in the ripple current.

$$I_{\text{RIPPLE}} = \Delta i = (V_{\text{IN}} - V_{\text{OUT}}) \times D / (f_{\text{SW}} \times L) \quad (\text{EQ. 2})$$

Where  $f_{\text{SW}}$  = switching frequency, L = Inductor value D = duty Cycle =  $V_{\text{OUT}}/V_{\text{IN}}$ .

The peak current through the inductor is show in Equation 3.

$$I_{\text{LPEAK}} = I_{\text{LOAD}} + \Delta i / 2 \quad (\text{EQ. 3})$$

Care should be taken when reducing  $F_{\text{SW}}$ , so that the peak current through the inductor does not cause an OCP (Over Current Protection) level to trip too early for the application. Operating with higher inductor current may enter a region of excessive inductor saturation. It is recommended to stay below 20A peak inductor current ripple.

Additionally, the output ripple voltage is given in Equation 4. Since it is proportional to  $\Delta i$ , it too will increase. The maximum allowable ripple voltage is really at the discretion of the designer.

$$V_{\text{RIPPLE}} = \Delta V = \Delta i \times \text{ESR} \quad (\text{EQ. 4})$$

Where ESR = the equivalent ESR of the output capacitance.

Another outcome of reducing the switching frequency is the tendency toward instability. Generally, if the switching frequency is reduced while keeping the same compensation, the loop bandwidth will become too large relative to the switching frequency. The ISL8200M family has integrated internal components for compensation, therefore the compensation is fixed. In many applications, this reduction will not be enough to cause any issues, but for applications where low amount of output capacitor is used or those with high ESR value, loop stability should be verified in the lab. It is recommended to not set the switching frequency below 500kHz.

## Conclusion

There are many reasons why the system designer may want to lower the switching frequency of the ISL8200M or ISL8200AM. Using either one of the two methods described above will give the desired result; however, care must be taken as there are several consequences to consider.

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