

Introduction

There are times when a digital video fade control is needed. DCPs are often overlooked for this application as they are thought to have too low a bandwidth for video. By selecting the proper DCP, the bandwidth is sufficient for NTSC and PAL video, as well as for HDTV.

Solution

The X9317ZS8 is a 1k Ω DCP and only a low value DCP can be used for video. The high operating capacitance of the CMOS switches used in the DCP causes the loss in bandwidth. This application note shows how to use a DCP as a video fader for digital control of the fade function. The fader function is done by using a DCP with one video source connected to one end of the DCP and a second video source connected to the other end of the DCP. Now, with the DCP set to one end only, the first video will be seen. Set at the other end of the DCP, only the second video will be seen. At the middle of the DCP setting, both videos will be seen but only at half level each. The other settings will be comparable ratios.

Video Sync

For two video sources to be faded they must be in sync. Some video sources can be synced from external sources. For those cases, the EL1881, EL1883 can be used as a sync source. The EL1881, EL1883 C SYNC output is low power, so it needs digital buffering to transmit over a cable. The EL1881, EL1883 also allows the fade to black function. The EL1881, EL1883 insures the constant sync needed for the fade to black function. The C SYNC out of the EL1881, EL1883 is too large to be used as the video sync, so it is attenuated to normal video level. If neither of these are used then the EL1881, EL1883 can be an unused option. For video sources that are not synced, there are costly converter boxes available to sync them.

Bandwidth Enhancement

The circuit uses one small capacitor for bandwidth recovery to compensate for the bandwidth loss of the DCP. The capacitor is very small value so has little risk of causing excess peaking. The capacitor C_5 from the op amp non-inverting input to the op amp output extends the bandwidth at all fader settings.

Circuit Biasing

The X9317 DCP is a 0V_{SUPPLY} to 5V_{SUPPLY} part and the video is AC coupled in so the DCP would see minus voltage and exceed the absolute maximum rating. To correct for this, a two diode clamp is used to clamp the sync tip to \sim 100mV above ground. The 100mV is the result of the difference in the bias current of the diodes, approximately 50 to 1 ratio. The clamp circuit also will reduce some power line noise on the video input signal. The output op amp also uses 0V_{SUPPLY} to 5V_{SUPPLY} and with only \sim 100mV on the sync tip output the coupling capacitor may be an option for some applications.

Cross Coupling

A small amount of cross coupling would be present from one input to the other at approximately 3.7% with no video input buffers. This can be corrected by using video buffers on the video source input lines. With buffers used, the bias input clamps are needed on both buffer inputs.

The circuit is shown with inputs terminated with 75 Ω to ground for a 75 Ω cable input. There is also an output series resistor, 75 Ω , for back-loaded cable driving. If there is no output cable load, then the amp gain may be set to one by changing the resistor value of the gain R_{14} to open and feedback R_{13} to zero.

The X9317ZS8 is a three wire up/down logic control DCP and the data sheet will give all the details needed for its proper operation.

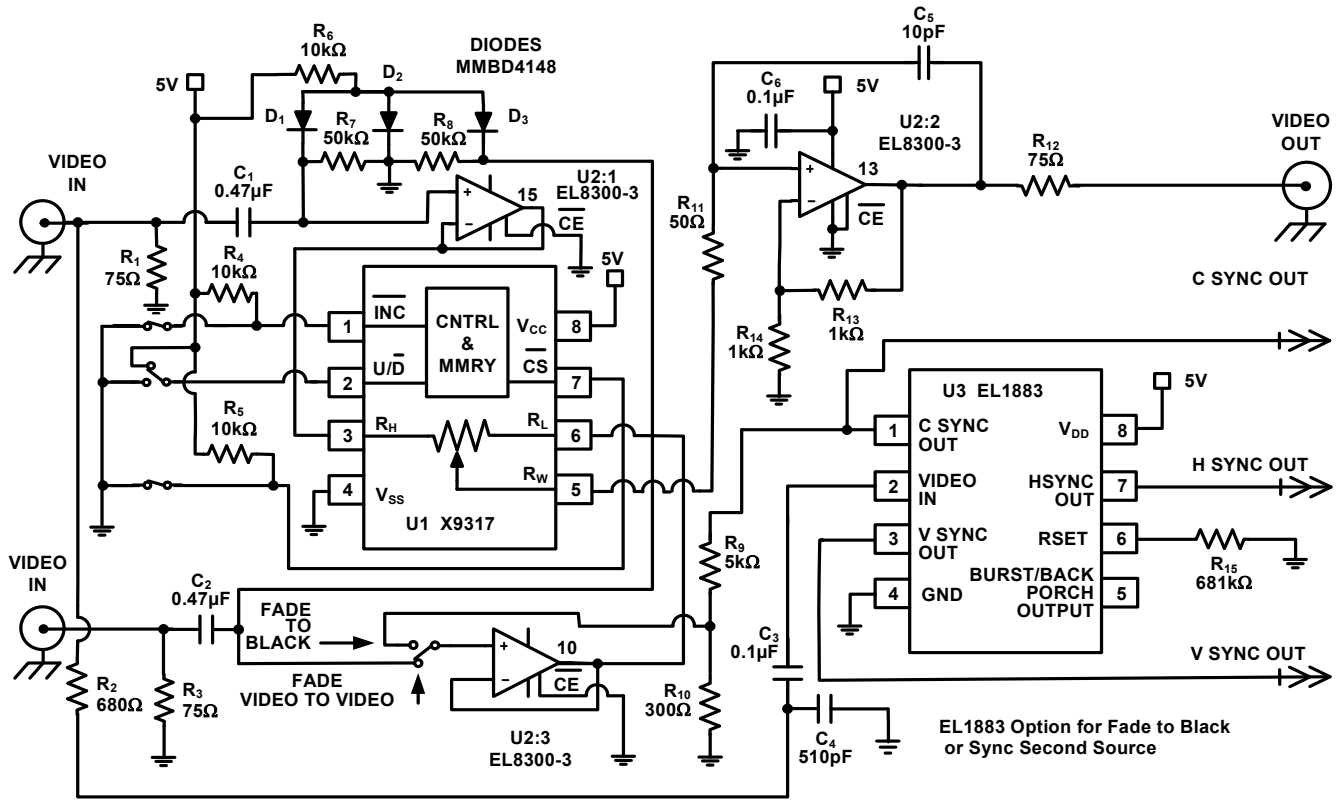


FIGURE 1. VIDEO FADER W/DCP DIGITAL CONTROL SCHEMATIC

NOTE: Figure 1 shows an updated, modified version of Figure 2 Eval Board Layout Schematic with the buffer amp U2C output directly connected to DCP Pin 6 and switch on U2C pin 8.

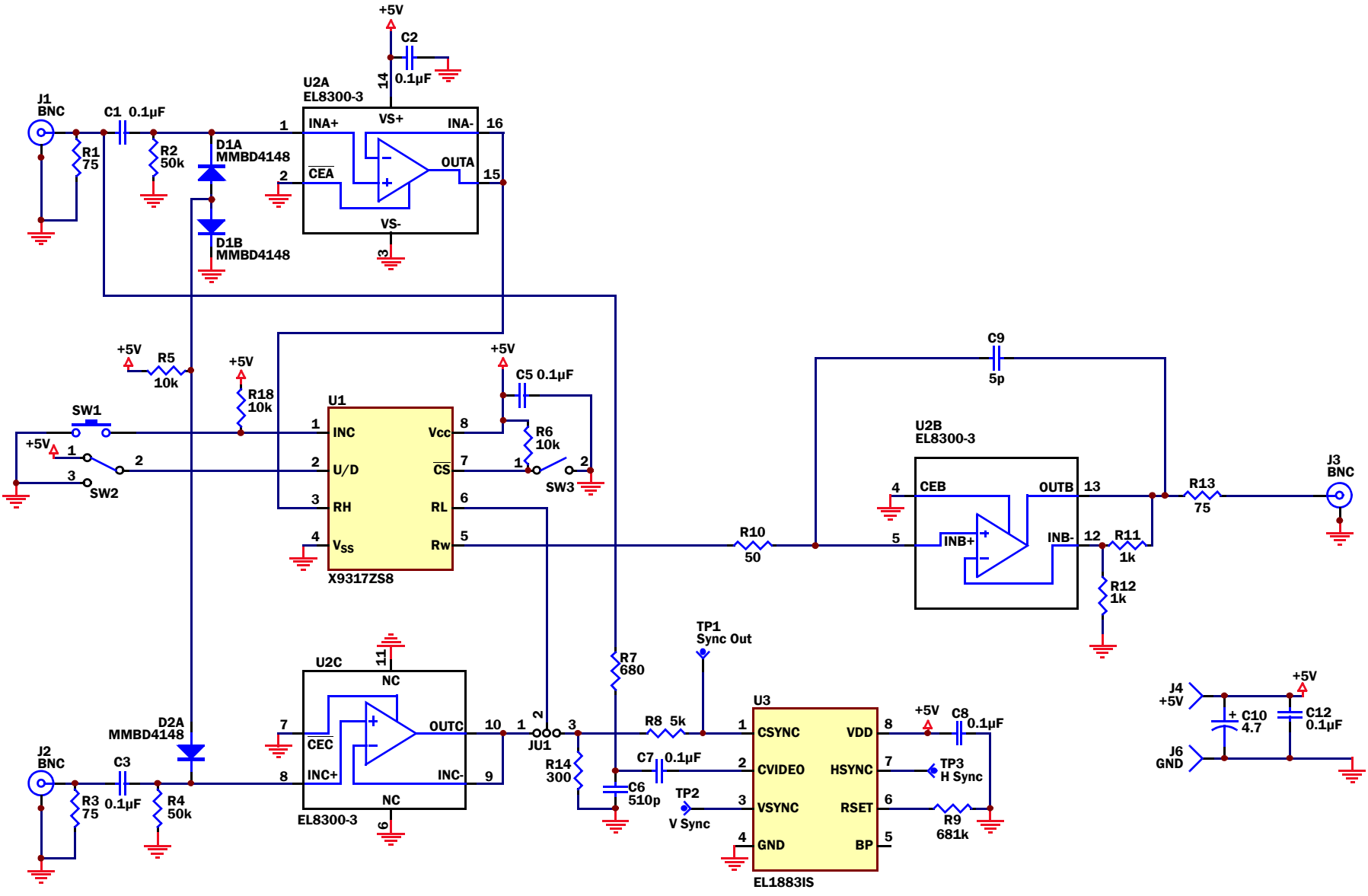


FIGURE 2. BOARD LAYOUT SCHEMATIC

Eval Board Layouts

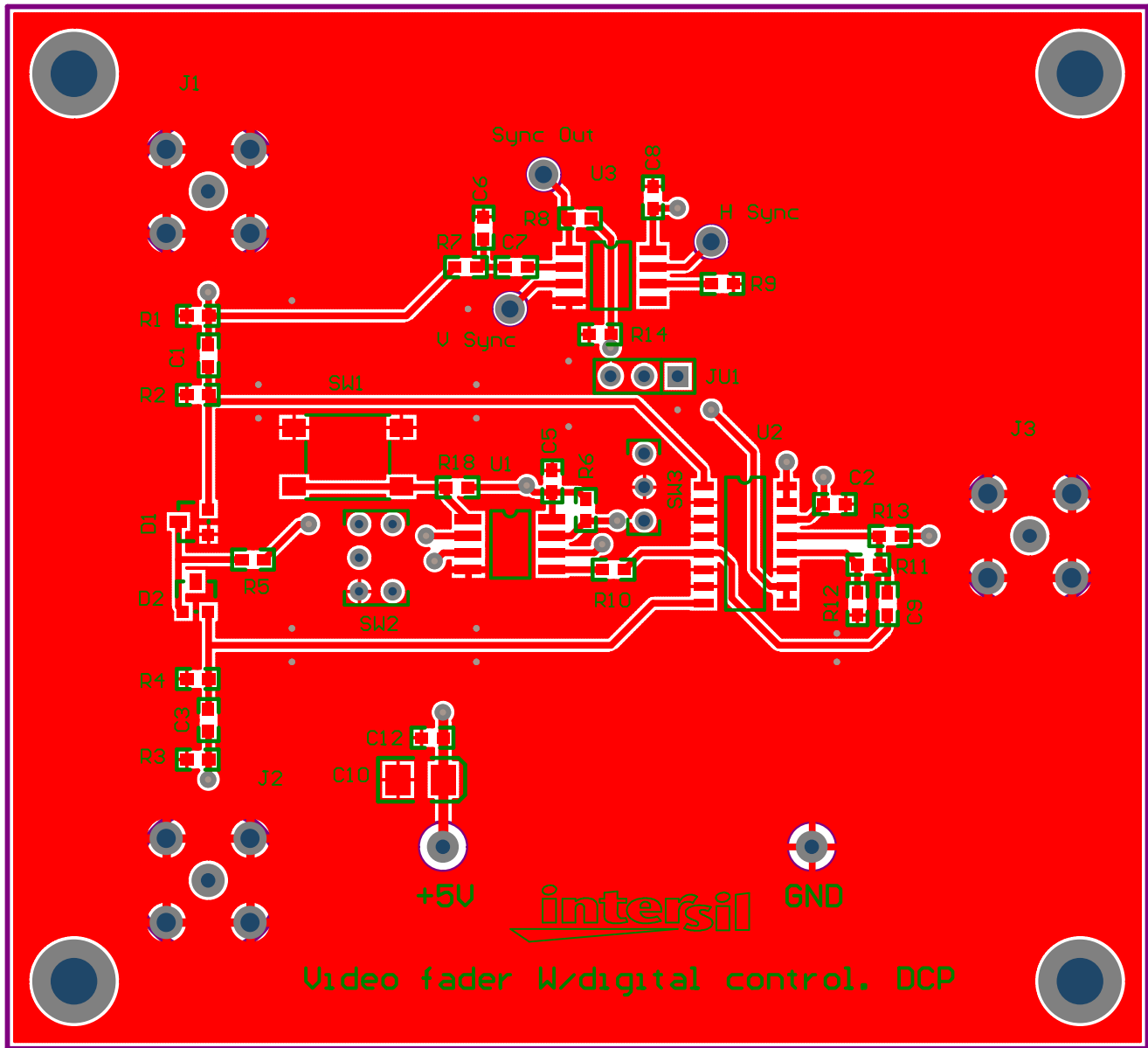


FIGURE 3. TOP LAYER

Eval Board Layouts (Continued)

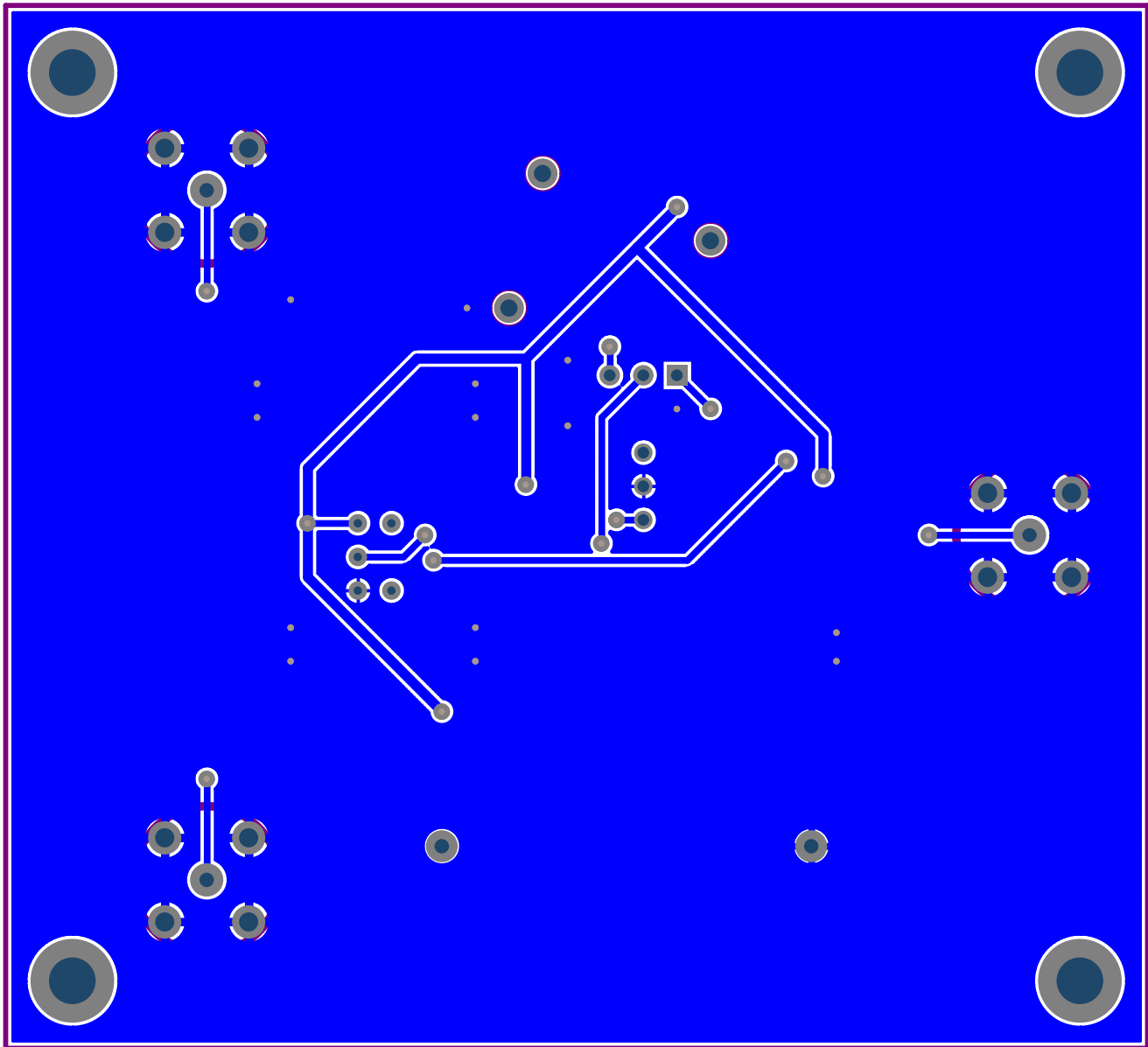


FIGURE 4. BOTTOM LAYER

Eval Board Layouts (Continued)

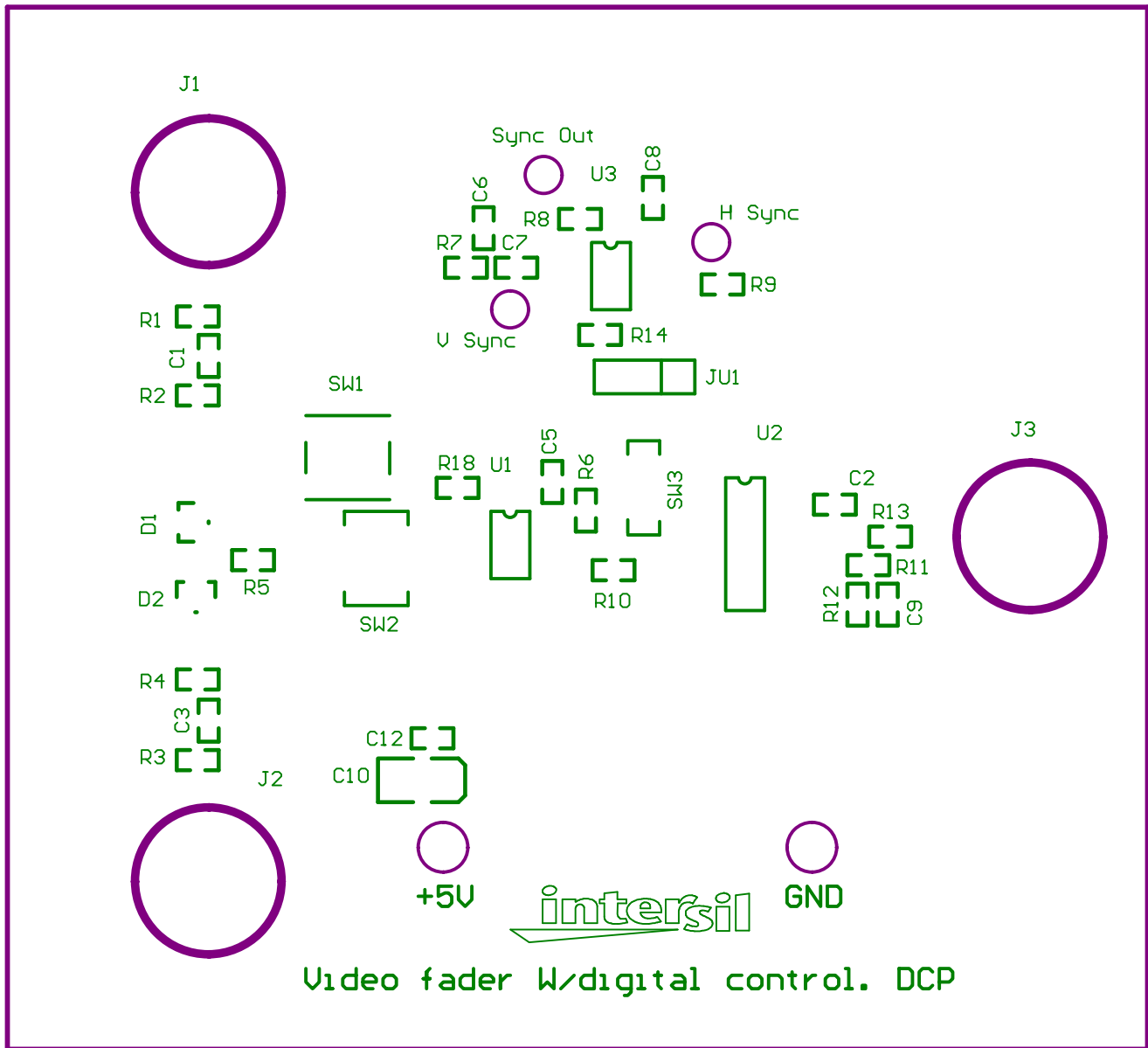


FIGURE 5. PART PLACEMENT

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