ISL70024SEH, ISL73024SEH

200V, 7.5A Enhancement Mode GaN Power Transistor

FN8976
Rev.5.00
Aug 16, 2019

The ISL70024SEH and ISL73024SEH are 200V N-channel enhancement mode GaN power transistors. These GaN FETs have been characterized for destructive Single Event Effects (SEE) and tested for Total Ionizing Dose (TID) radiation. Applications for these devices include commercial aerospace, medical, and nuclear power generation.

GaN's exceptionally high electron mobility and low temperature coefficient allows for very low $r_{DS(ON)}$, while its lateral device structure and majority carrier diode provide exceptionally low Q_G and near zero Q_{RR}. The end result is a device that can operate at a higher switching frequency with more efficiency while reducing the overall solution size.

By combining the exceptional performance of the GaN FET in a hermetically sealed Surface Mount Device (SMD) package with manufacturing in a MIL-PRF-38535 like flow results in best-in-class power transistors that are ideally suited for high reliability applications.

Applications

- Switching regulation
- Motor drives
- Relay drives
- Inrush protection
- Down hole drilling
- High reliability industrial

Features

- **Very low $r_{DS(ON)}$ 45mΩ (typical)**
- **Ultra low total gate charge 2.5nC (typical)**
- SEE hardness (see SEE report for details)
  - SEL/SEB LET_{TH} (V_{DS} = 160V, V_{GS} = 0V): 86MeV•cm^2/mg
- ISL70024SEH radiation acceptance (see TID report)
  - High dose rate (50-300rad(Si)/s): 100krad(Si)
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
- ISL73024SEH radiation acceptance (see TID report)
  - Low dose rate (0.01rad(Si)/s): 75krad(Si)
- Ultra small hermetically sealed 4 Ld Surface Mount Device (SMD) package
  - Package area: 42mm^2
- Full military-temperature range operation
  - T_A = -55°C to +125°C
  - T_J = -55°C to +150°C

Related Literature

For a full list of related documents, visit our website:

- ISL70024SEH, ISL73024SEH device pages

Figure 1. ISL70024SEH 4 Ld SMD Package

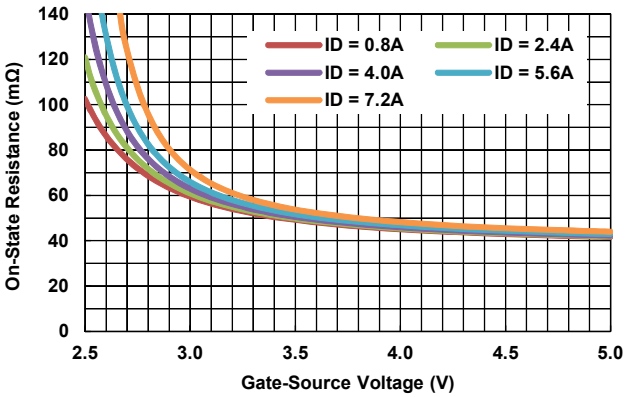


Figure 2. On-State Resistance (+25°C)

1. Overview

1.1 Ordering Information

Ordering Part Number (Note 1)	Radiation Hardness (Total Ionizing Dose)	Temperature Range (°C)	Package (RoHS Compliant)	Package Drawing
ISL70024SEHML	HDR to 100krad(Si) LDR to 75krad(Si)	-55 to +125	4 Ld SMD	J4.A
ISL73024SEHML	LDR to 75krad(Si)	-55 to +125	4 Ld SMD	J4.A
ISL70024SEHMX	HDR to 100krad(Si) LDR to 75krad(Si)	-55 to +125	Die	-
ISL73024SEHMX	LDR to 75krad(Si)	-55 to +125	Die	-
ISL70024SEHX/SAMPLE (Note 2)	N/A	+25	Die	-
ISL73024SEHX/SAMPLE (Note 2)	N/A	+25	Die	-
ISL70024SEHL/PROTO (Note 2)	N/A	-55 to +125	4 Ld SMD	J4.A
ISL73024SEHL/PROTO (Note 2)	N/A	-55 to +125	4 Ld SMD	J4.A
ISL70040SEHEV3Z (Note 3)	Evaluation board with the ISL70040SEH low-side driver and ISL70024SEH 200V GaN FET			
ISL73040SEHEV4Z (Note 3)	Half bridge power stage using the ISL73040SEH, ISL73024SEH, and the ISL71610M			

Notes:

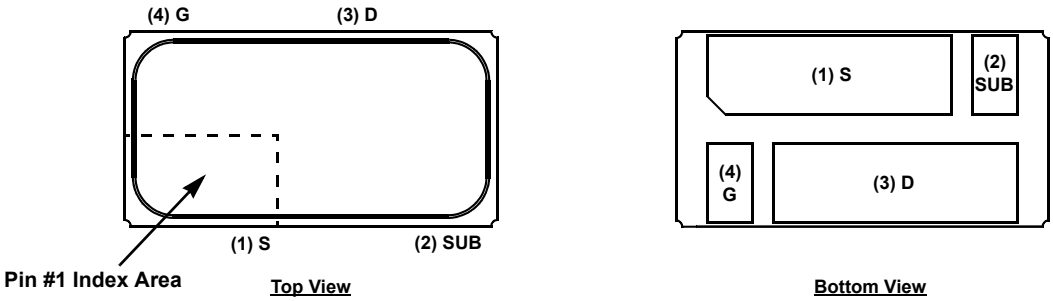
1. These Pb-free Hermetic packaged products employ 100% Au plate - e4 termination finish, which is RoHS compliant and compatible with both SnPb and Pb-free soldering operations.
2. The /PROTO and /SAMPLE parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity. These parts are intended for engineering evaluation purposes only. The /PROTO and /SAMPLE parts meet the electrical limits and conditions across the temperature range specified in this datasheet and are of the same form and fit as the ISL70024SEHML/ISL73024SEHML devices. The /PROTO and /SAMPLE parts do not come with a Certificate of Conformance (C of C) and have no accompanying data or documentation.
3. Evaluation boards use the /PROTO parts and /PROTO parts are not rated or certified for Total Ionizing Dose (TID) or Single Event Effect (SEE) immunity.

Table 1. Key Differences Between Family of Parts

Part Number	I_D (A)	$r_{DS(ON)}$ Typical (mΩ)	Breakdown Voltage	Radiation Assurance
ISL70024SEH	7.5	45	200V	HDR to 100krad(Si) LDR to 75krad(Si)
ISL73024SEH	7.5	45	200V	LDR to 75krad(Si)
ISL70023SEH	60	5	100V	HDR to 100krad(Si) LDR to 75krad(Si)
ISL73023SEH	60	5	100V	LDR to 75krad(Si)

1.2 Pin Configuration

4 Ld SMD



Note: The ESD triangular mark indicates Pin #1. It is a part of the device marking and is placed on the lid in the quadrant where Pin #1 is located.

1.3 Pin Descriptions

Pin Number	Pin Name	Description
1	S	Source connection for the GaN FET.
2	SUB	Substrate connection for the GaN FET which is internally shorted in to source. Tie this pin to source on the PCB.
3	D	Drain connection for the GaN FET.
4	G	Gate connection for the GaN FET. Minimize trace inductance from driver to reduce over-stressing the gate.
NA	Lid	Internally tied to the source pin.

2. Specifications

2.1 Absolute Maximum Ratings

Parameter	Minimum	Maximum	Unit
V_{DS}	0	200	V
V_{DS} (Note 4)	0	160	V
V_{GS}	-4	6	V
ESD Rating (Drain-to-Source)	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM3015)	2		kV
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V
ESD Rating (Gate-to-Source)	**Value**		**Unit**
Human Body Model (Tested per MIL-STD-883 TM3015)	500		V
Machine Model (Tested per JESD22-A115C)	200		V
Charged Device Model (Tested per JS-002-2014)	750		V

CAUTION: Do not operate at or near the maximum ratings listed for extended periods of time. Exposure to such conditions can adversely impact product reliability and result in failures not covered by warranty.

Note:

4. Tested in a heavy ion environment at LET = 86.4MeV•cm^2/mg at +125°C (T_C).

2.2 Thermal Information

ISL70024SEH, ISL73024SEH in SMD Package J4.A			
Thermal Resistance	**Typical**	**Maximum**	**Unit**
θ_{JA} (Note 5)	42.0	-	°C/W
θ_{JC} (Note 6)	18.7	23.4	°C/W

Notes:

5. θ_{JA} is measured in free air with the component mounted on a high-effective thermal conductivity test board with “direct attach” features. See TB379.
6. For θ_{JC}, the “case temp” location is on the solder terminations adjacent to the center of the package underside.

Parameter	Minimum	Maximum	Unit
Maximum Junction Temperature	-	+150	°C
Storage Temperature Range	-65	+150	°C

2.3 Recommended Operating Conditions

Parameter	Minimum	Maximum	Unit
Temperature	-55	+125	°C
V_{DS}	0	160	V
I_D (V_{GS} = 5.0V, T_C = +25°C) (Note 7)	0	7.5	A
I_D (V_{GS} = 5.0V, T_C = +105°C) (Note 7)	0	4.5	A

Note:

7. T_J = +150°C. Current limited by package constraints.

2.4 Electrical Specifications

Unless otherwise noted, V_{DS} = 160V. **Boldface limits apply across the operating temperature range, -55°C to +125°C; over a total ionizing dose of 100krad(Si) with exposure at a high dose rate of 50-300rad(Si)/s (ISL70024SEH only); or over a total ionizing dose of 75krad(Si) with exposure at a low dose rate of <10mrad(Si)/s.**

Parameter	Symbol	Test Conditions	Min (Note 9)	Typ (Note 9)	Max (Note 9)	Unit
Static Characteristics						
Drain-to-Source Breakdown Voltage	BV_{DSS}	V_{GS} = 0V, I_D = 125µA	**200**	-	-	V
Drain-to-Source Leakage Current	I_{DSS}	V_{DS} = 160V, V_{GS} = 0V	-	1	**115**	µA
Drain-to-Gate Leakage Current	I_{GSX}	V_{DS} = 160V, V_{GS} = 0V	-	1	**115**	µA
Gate-to-Source Forward Leakage	I_{GSS}	V_{GS} = 5V	-	0.8	**2.5**	mA
Gate-to-Source Reverse Leakage		V_{GS} = -4V	**-100**	-20	-	µA
Gate Threshold Voltage	$V_{GS(th)}$	V_{DS} = V_{GS}, I_D = 1.5mA	**0.8**	1.4	**2.5**	V
Drain-to-Source ON-Resistance	$r_{DS(ON)}$	V_{GS} = 5V, I_D = 7A	-	45	**110**	mΩ
Source-to-Drain Forward Voltage	V_{SD}	I_S = 0.5A, V_{GS} = 0V	**0.8**	1.8	**3.5**	V
Dynamic Characteristics						
Input Capacitance	C_{ISS}	V_{DS} = 100V, V_{GS} = 0V (Note 10)	-	270	-	pF
Output Capacitance	C_{OSS}	V_{DS} = 100V, V_{GS} = 0V, T_A = +25°C	-	150	200	pF
Reverse Transfer Capacitance	C_{RSS}	V_{DS} = 100V, V_{GS} = 0V (Note 10)	-	1	-	pF
Gate Resistance	r_G	T_A = +25°C (Note 10)	-	60	-	mΩ
Total Gate Charge	Q_G	V_{DS} = 100V, V_{GS} = 5V, I_D = 7A, T_A = +25°C	-	2.5	5	nC
Gate Charge at Threshold	$Q_{G(th)}$	V_{DS} = 100V, I_D = 7A (Note 10)	-	0.4	-	nC
Gate-to-Source Charge	Q_{GS}	V_{DS} = 100V, I_D = 7A, T_A = +25°C	-	0.8	2.0	nC
Gate-to-Drain Charge	Q_{GD}	V_{DS} = 100V, I_D = 7A, T_A = +25°C	-	0.6	2.0	nC
Output Charge	Q_{OSS}	V_{DS} = 100V, V_{GS} = 0V (Note 10)	-	23	-	nC

Notes:

8. Typical values shown are not guaranteed.
9. Parameters with MIN and/or MAX limits are 100% tested at -55°C, +25°C, and +125°C, unless otherwise specified.
10. Limits are established by characterization and/or design and are not tested.

3. Typical Performance Curves

Unless otherwise noted, V_{DS} = 160V; T_A = +25°C.

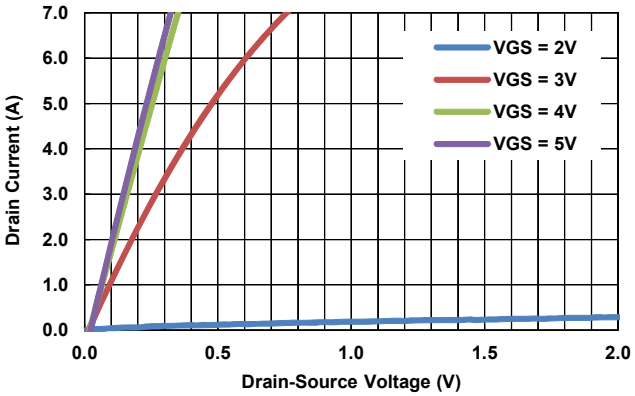


Figure 3. Output Characteristics (+25°C)

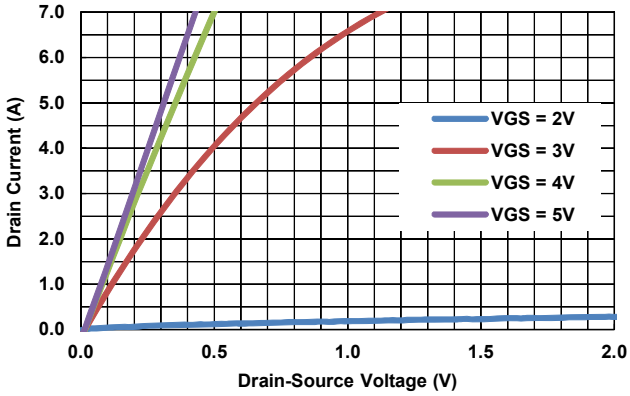


Figure 4. Output Characteristics (+125°C)

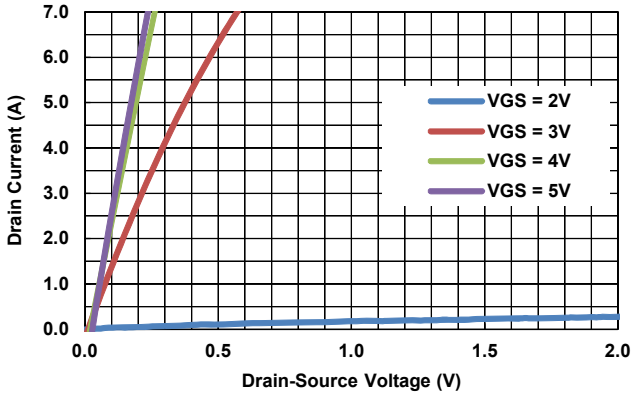


Figure 5. Output Characteristics (-55°C)

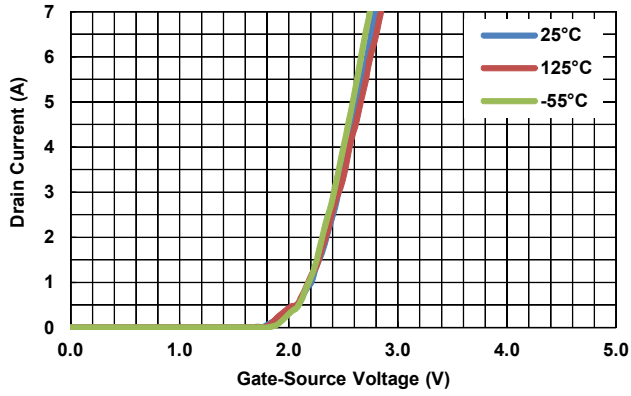


Figure 6. Transfer Characteristics

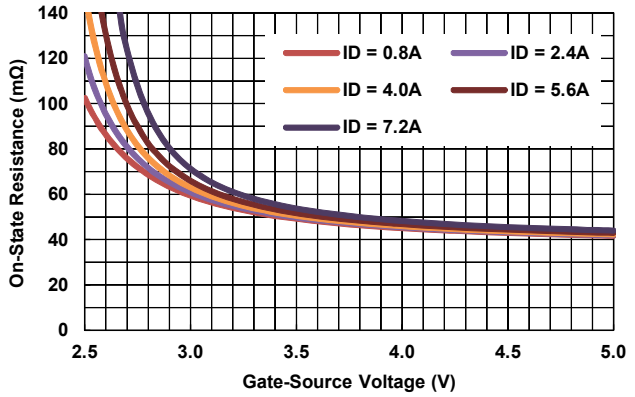


Figure 7. On-State Resistance (+25°C)

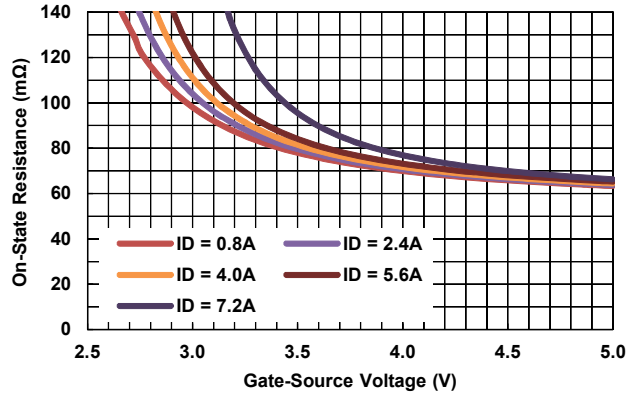


Figure 8. On-State Resistance (+125°C)

Unless otherwise noted, V_{DS} = 160V; T_A = +25°C. **(Continued)**

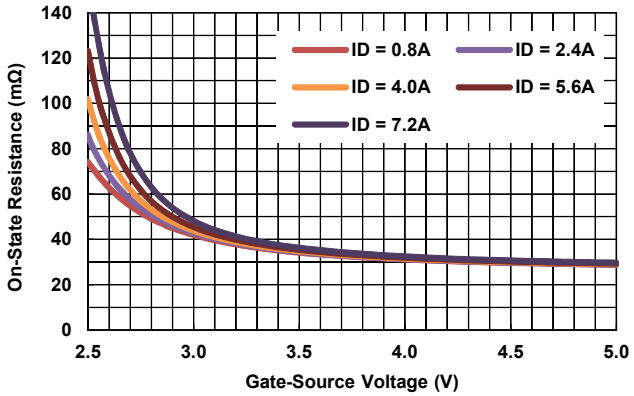


Figure 9. On-State Resistance (-55°C)

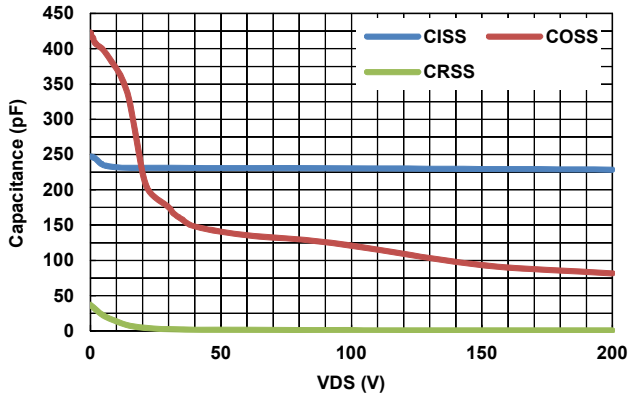


Figure 10. Capacitance (Linear Scale)

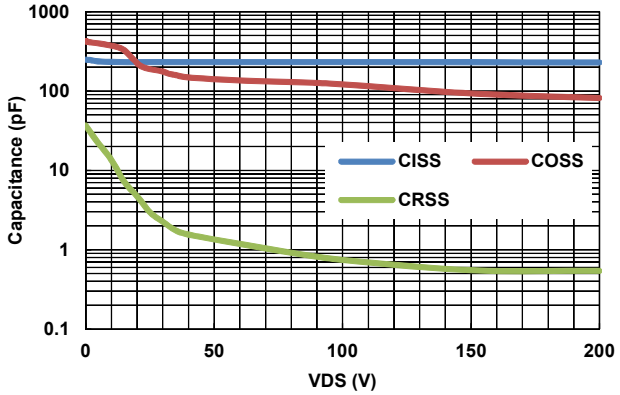


Figure 11. Capacitance (Log Scale)

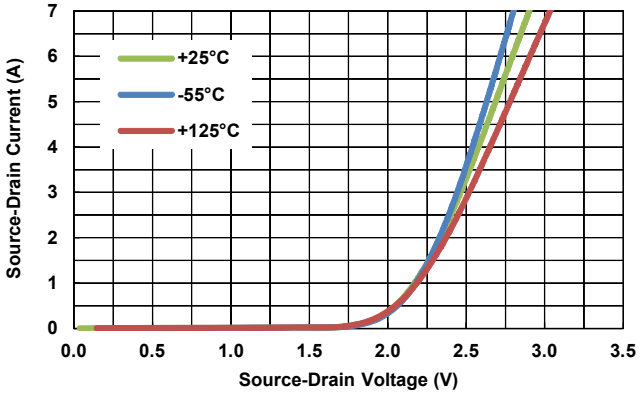


Figure 12. Reverse Drain-Source Characteristics

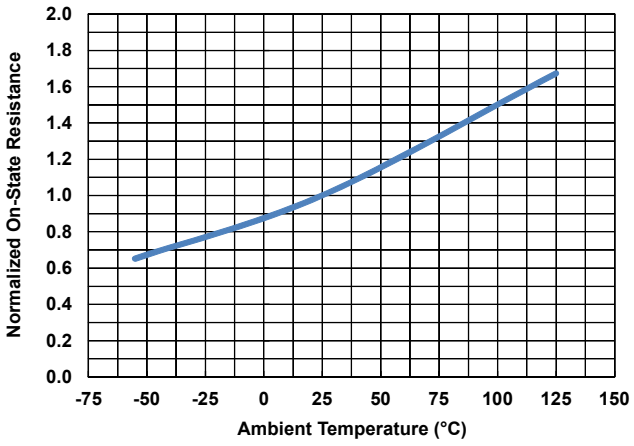


Figure 13. Normalized On-State Resistance

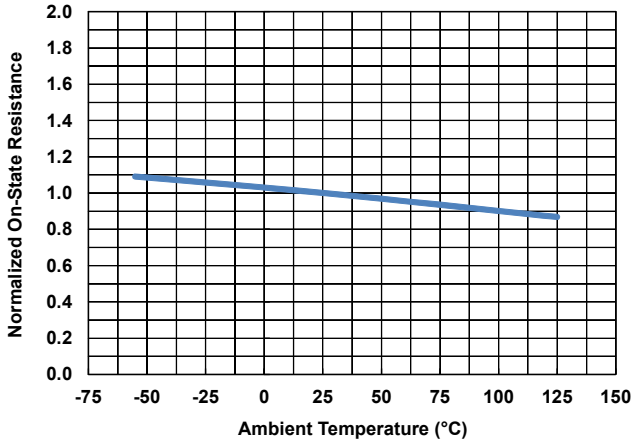


Figure 14. Normalized Threshold Voltage

Unless otherwise noted, V_{DS} = 160V; T_A = +25°C. **(Continued)**

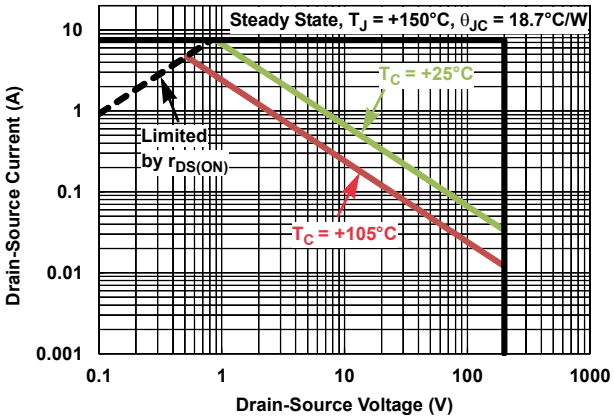


Figure 15. Safe Operating Area

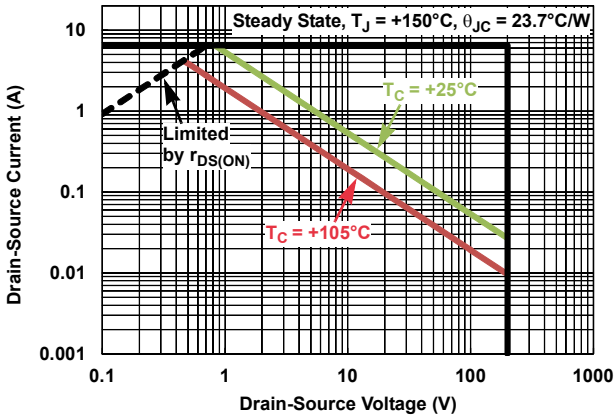


Figure 16. Safe Operating Area (Derated)

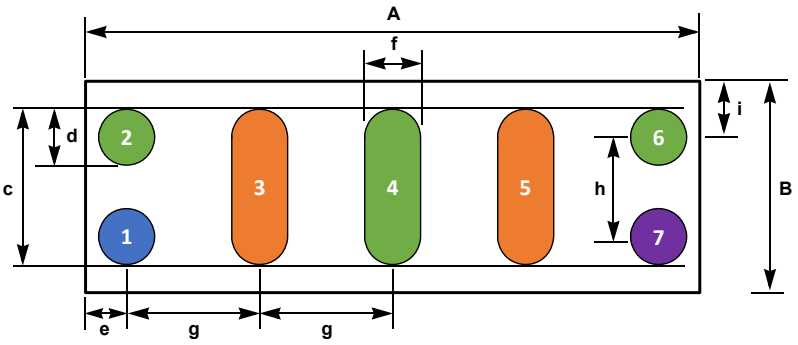
4. Die Characteristics

Table 2. Die and Assembly Related Information

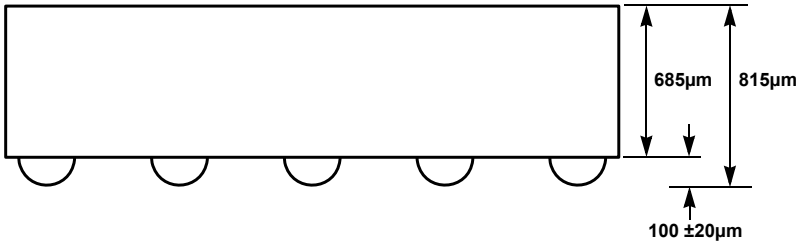
Die Information	
Dimensions	2766µm x 950µm (108.90 mils x 37.40 mils) Thickness: 685µm (26.97 mils)

ISL70024SEH, ISL73024SEH

Solder Bar View



Side View



Color Key:

Pads in Green are the Source

Pads in Orange are the Drain

Pad in Blue is the Gate

Pad in Purple is the Substrate

Table 3. Dimensions

Dimension	Min (µm)	Nominal (µm)	Max (µm)
A	2736	2766	2796
B	920	950	980
c	697	700	703
d	247	250	253
e	168	183	198
f	245	250	255
g	600	600	600
h	450	450	450
i	235	250	265

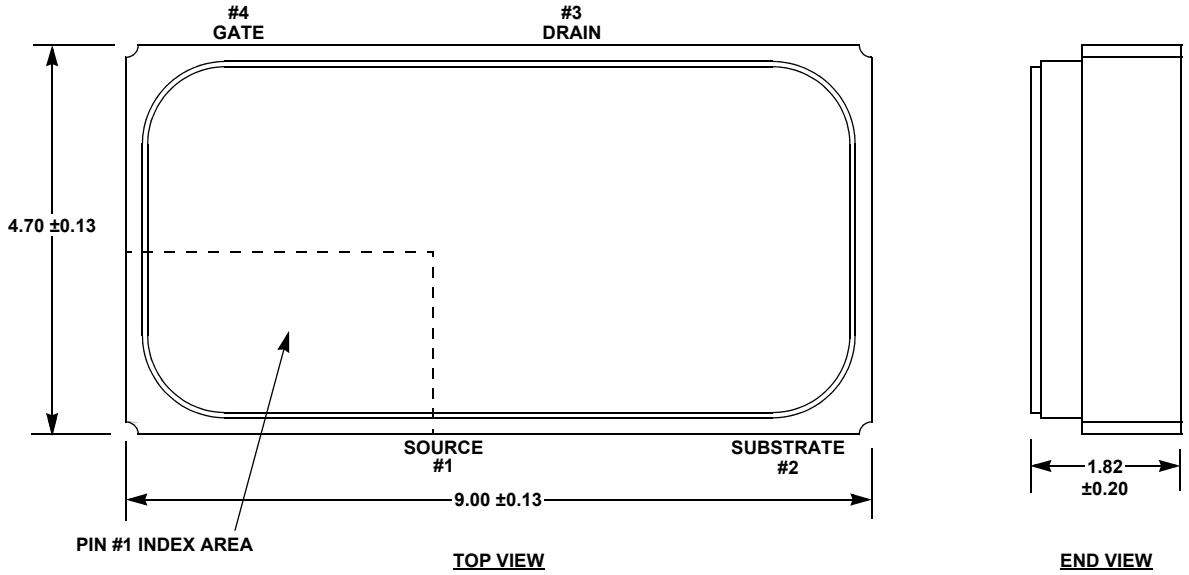
5. Revision History

Rev.	Date	Description
5.00	Aug 16, 2019	Updated SEE and TID ratings in Features section. Added radiation levels to ordering information table. Updated Table 1 on page 2.
4.00	Feb 8, 2019	Updated ordering information table by adding evaluation boards and Note 3. Updated disclaimer.
3.00	Mar 8, 2018	Updated ordering information table by correcting /SAMPLE part numbers and adding Die where applicable. Updated Section 4 heading from “Die and Assembly Characteristics” to “Die Characteristics”.
2.00	Feb 5, 2018	Changed 55mΩ to 45mΩ in the first Features bullet.
1.00	Jan 15, 2018	Updated Figure 1. Added ISL73024SEH part to datasheet. Ordering Information table on page 2 and updated Note 2. Added Table of Differences on page 2. Electrical Spec table - updated Note 9 on page 5. Added Die and Assembly Characteristics section on page 9. Removed “About Intersil” section. Updated disclaimer and moved to last page.
0.00	Oct 4, 2017	Initial release

6. Package Outline Drawing

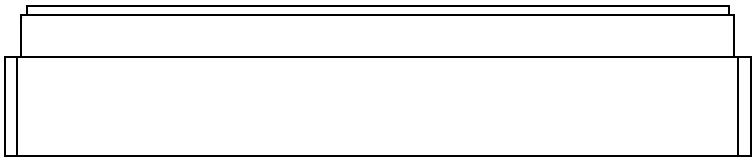
For the most recent package outline drawing, see J4.A.

J4.A
4 PIN 9.0mmx4.7mm HERMETIC SURFACE MOUNT PACKAGE
Rev 0, 2/16

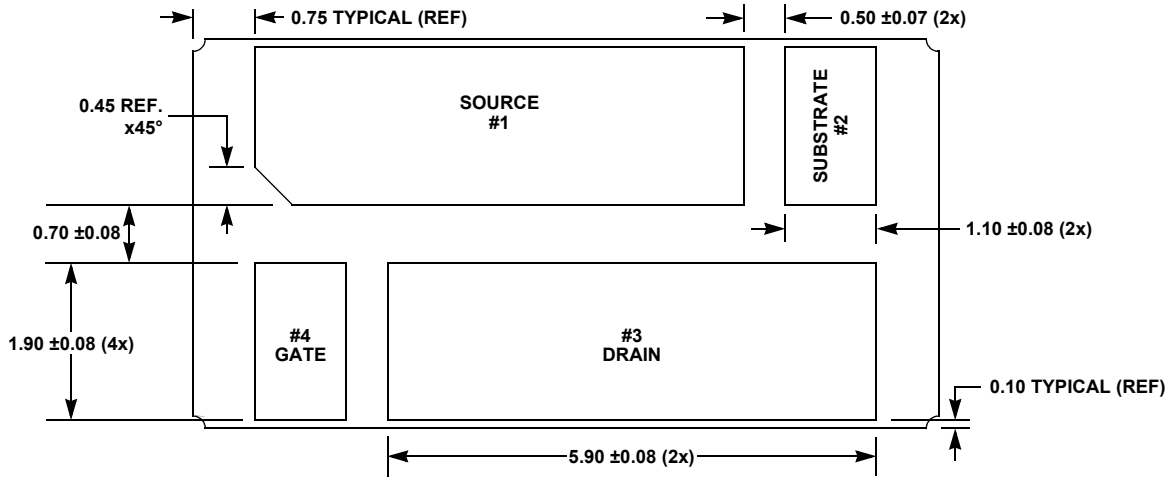


TOP VIEW

END VIEW



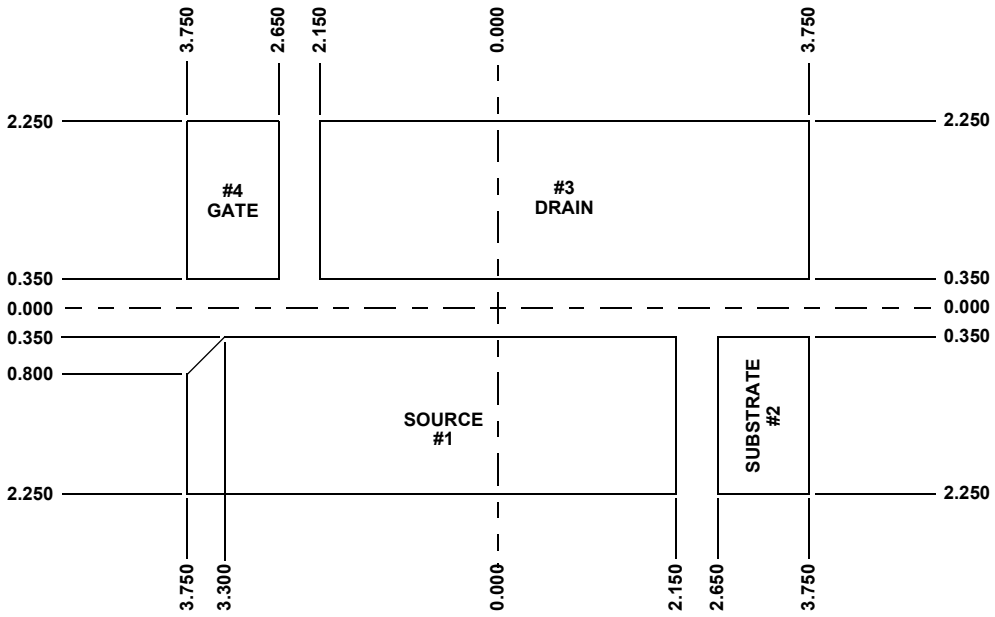
SIDE VIEW



BOTTOM VIEW

NOTES:

1. The corner shape (radius, chamfer, etc.) may vary at the manufacturer's option from that shown on the drawing.
2. The package thickness dimension is the package height before being solder dipped.
3. Dimensions are in millimeters.



TYPICAL RECOMMENDED LAND PATTERN

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Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Contact Information

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