Design Considerations for High-Speed RS-485 Data Links

Introduction

The trend in high-speed data networks continues to push for higher data rates over longer transmission distances, and under ever-harsher conditions, including electrically noisy environments, large ground potential differences, and high operating temperatures. The primary applications pushing reliable high-speed transmissions to the breaking point include:

- Data acquisition systems in seismic networks
- GPS data transmission links in telecom base stations
- Video transport in traffic monitoring systems
- PLC communication in factory automation
- Motor encoders

This article provides system designers new to high-speed RS-485 designs with an overview of standard and high-speed RS-485 networks. We begin with examining signal degradation on the bus and key transceiver requirements for reliable high-speed transmission, and then wrap up with design tips for system and bus node designs, along with a set of general high-speed design guidelines.

RS-485 Standard Networks

EIA/TIA-485, commonly referred to as the RS-485 standard, specifies the electrical characteristics of drivers and receivers for use in balanced (symmetrical) digital multipoint systems (see Figure 1).

Industrial networks often cover long distances and use a single twisted pair cable to keep cabling cost down. These networks operate in half-duplex mode, meaning a bus node either transmits or receives data over the same cable. One limitation of half-duplex networks is that the master node can only transmit or receive data, but not both at the same time. Masters in the full-duplex configuration can simultaneously transmit data to a node via the transmit bus and receive data from a node via the receive bus.

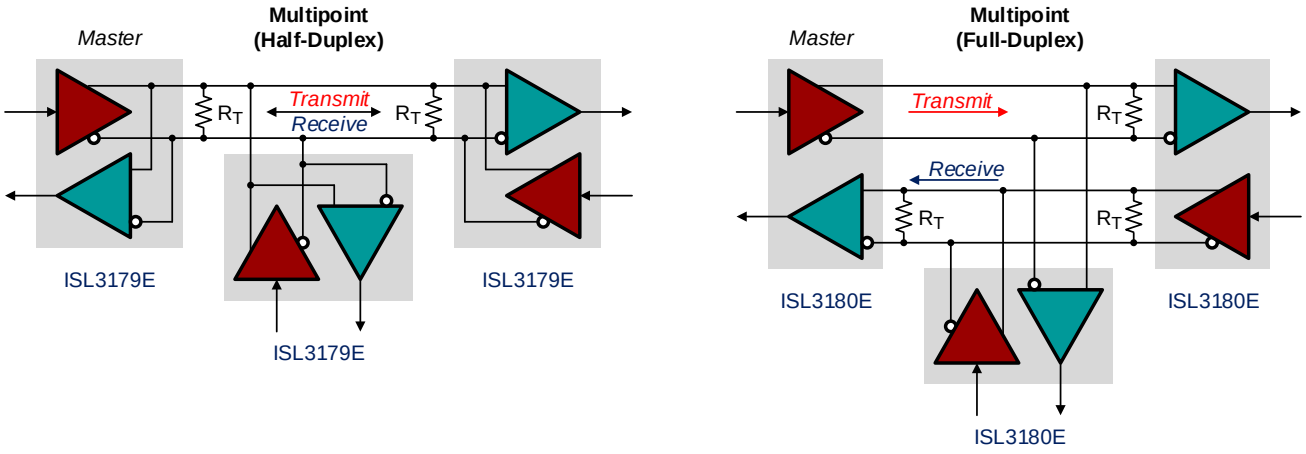

Figure 1. Multipoint systems allow for the direct connection of multiple transceivers on the same bus

Time critical networks utilize the full-duplex configuration, where a master node can simultaneously transmit and receive data on different cables. This method increases data throughput due to reduced latency but also doubles cabling requirements. Multipoint systems are commonly used at data rates below 2Mbps.

RS-485 High-Speed Networks

High-speed and ultra-high-speed data links commonly use simpler network configurations (see Figure 2).

- Single point-to-point links are applied when high data throughput is needed.
- Parallel data links are often found in established small computer serial interface (SCSI) applications with multiple high-speed channels, synchronized data systems transmitting clock and data, and deserializer-to-serializer interfaces.
- Multidrop links are used for legacy RS-422 applications and clock distribution networks in harsh environments.
- Full-duplex point-to-point links are needed in applications requiring low latency and high data throughput.
- Half-duplex point-to-point links reduce cabling cost, while assuring high data rates for applications without stringent latency requirements.

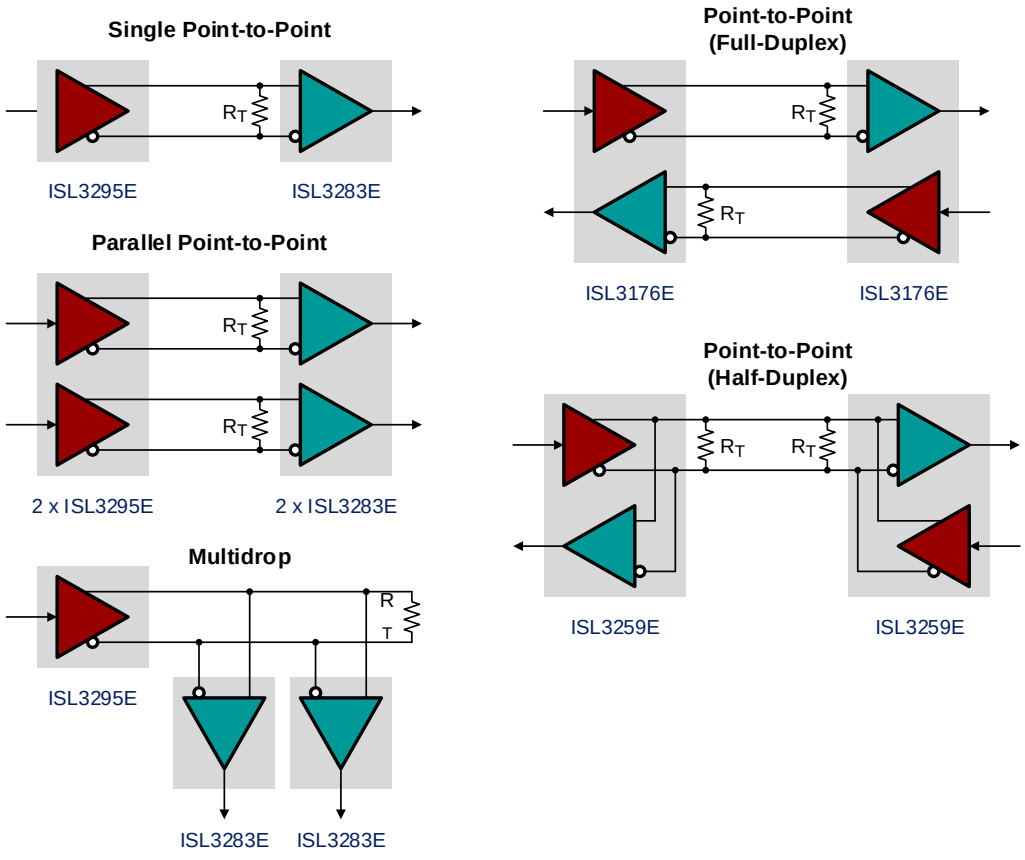

Figure 2. Common data link configurations for high-speed applications

Signal Degradation Through Jitter

High-speed RS-485 data links are limited in cable length because of signal degradation in the form of jitter. Both driver and receiver pulse skews and pattern-dependent cable skew is what causes signal jitter.

Driver and receiver pulse skew is the difference in propagation delays for the rising and falling edges of the driver and receiver ($t_{SKEW} = |t_{PLH} - t_{PHL}|$). Figure 3 shows that this skew determines the pulse distortion occurring between the single-ended input and the differential output of a driver, and between the differential input and the single-ended output of a receiver. The total pulse distortion is the sum of the skews through the Tx and the Rx in the signal path. The values in Figure 3 show total maximum pulse distortion of ±12% for all Renesas 40Mbps transceivers.

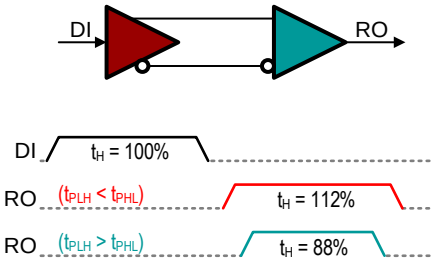

Figure 3. Total pulse distortion due to driver and receiver skews

Bit-pattern dependent cable skew is the variation of signal rise and fall times on the bus caused by varying bit sequences of ones and zeros. Figure 4 shows the fall and rise times for a single low pulse following two different bit patterns. One pattern is a long string of 1s charging the cable capacitance to the maximum level. The other pattern is a clock signal with equal charge/discharge times and a more consistent, although smaller, amplitude.

As you can see, the fall time of the bus signal starting at the higher voltage (red) is longer than that of the clock pulse (blue), and the red signal can't discharge to as low a voltage during the single low bit. Thus, the red signal's following rise time is shorter because the charging process now starts from a higher voltage than the clock signal.

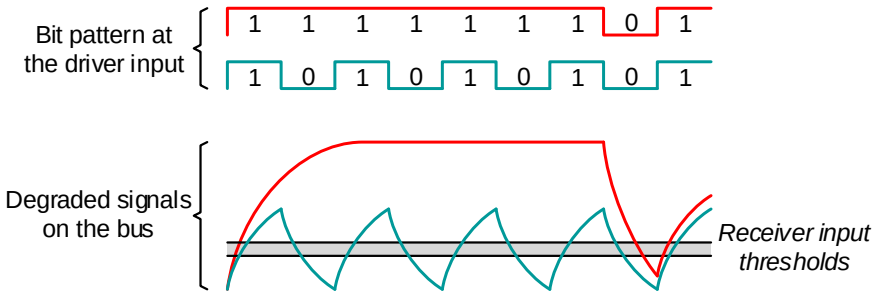

Figure 4. Tx output rise/fall times varying due to changing bit patterns

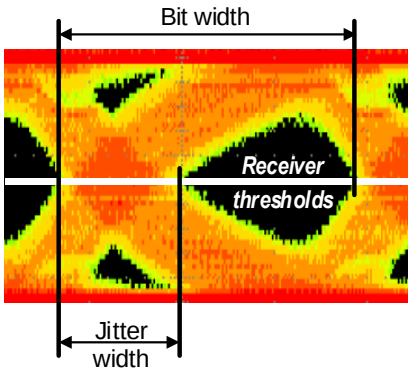

Figure 5. Typical eye-diagram

Data pulses respond to bit-pattern dependent skew with a loss in amplitude, rounded edges, displacement in time, and a "smearing" of the pulse into adjacent bit intervals.

Measuring the signal transitions over a wide range of pseudo random binary sequence (PRBS) data yields an eye-pattern such as the one in Figure 5. An eye-pattern allows a visual assessment of the quality of a

transmission link. The wider the eye opening, the smaller the jitter. Jitter is expressed as a percentage and is defined by the ratio of jitter width to bit width:

$$Jitter(\%) = 100 \times \frac{Jitter\ width(s)}{Bit\ width(s)} \qquad \text{EQ. 1}$$

In order to reduce jitter, data coding schemes such as Manchester coding, 8b/10b coding, or 33hex can be applied. Encoding the data stream removes the large DC content of long bit sequences of 1s and 0s by introducing more transitions into the data stream in order to charge and discharge the cable capacitance more equally, and generate more consistent signal amplitudes.

Manchester encoding combines the initial data with a clock signal via an XOR function. Here, the period of the clock equals the bit-width, which results in a rather inefficient use of bandwidth. The advantage of Manchester coding, however, is that its longest sequence of 1s or 0s is limited to just one bit time (see Figure 6), which significantly reduces bit pattern dependent jitter.

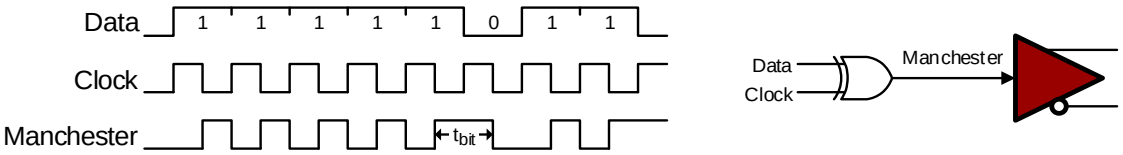

Figure 6. Manchester encoding: signal timing and coding principle

8-bit/10-bit coding uses look-up tables that assign 10-bit codes to 256 x 8-bit data words with no more than 5 consecutive 1s or 0s. It is often preferred over Manchester coding because of its more efficient use of bandwidth (see Figure 7).

Decimal	8-bit data	10-bit code
0	00000000	1001110100
1	00000001	0111010100
2	00000010	1011010100
:	:	:
253	11111101	1011100001
254	11111110	0111100001
255	11111111	1010110001

Figure 7. Excerpt from an 8b/10b coding table

33hex is a hex-code added to the original transmitter data and later subtracted in the receiver. It is a clock independent, low-cost method to break up long bit sequences (of the same polarity) into shorter sequences, and is specified in the e-meter protocol standard, DL/T645 (see Figure 8).

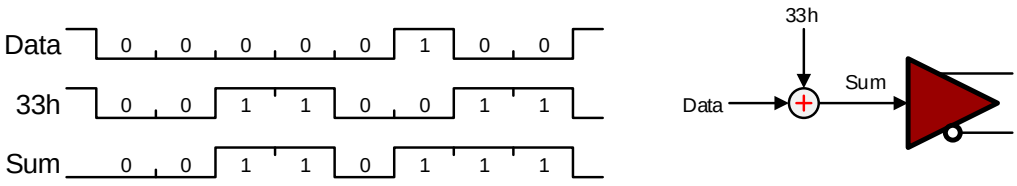

Figure 8. Low-cost encoder with 33hex

Data encoding shortens the charge and discharge time of the cable capacitance, which in turn lowers the bus signal amplitude. To assure that the receiver sees a valid input signal with sufficient noise margin, high-speed transceivers with large output drive capability are recommended.

Transceiver Requirements

To counteract the aforementioned signal degradation issues, choose high-speed transceivers with large differential output voltages (V_{OD}) and small skews.

Large driver V_{OD} overcomes the reduction in signal amplitude due to cable attenuation, data encoding and common mode loading (result of ground potential differences), and ensures sufficient noise margin at the remote receiver inputs.

For low-voltage designs, be careful using so-called "Poor Man's" 3V transceivers (see Figure 9) as these have poorly designed output stages that only provide RS-485 compliant output voltages at supply voltages ≥ 4V. At lower supply rails, the transistor efficiency drastically drops, producing a V_{OD} up to 40% below the 1.5V minimum required by RS-485. Output voltages that low will not yield sufficient noise margin to trigger a remote receiver.

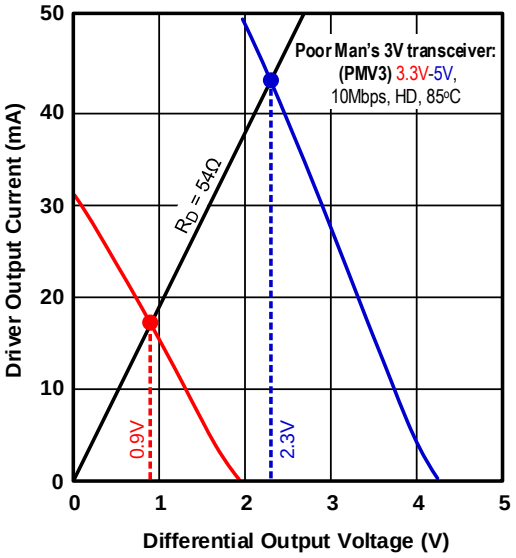

Figure 9. PM3V transceiver running out of steam at 3.3V supply

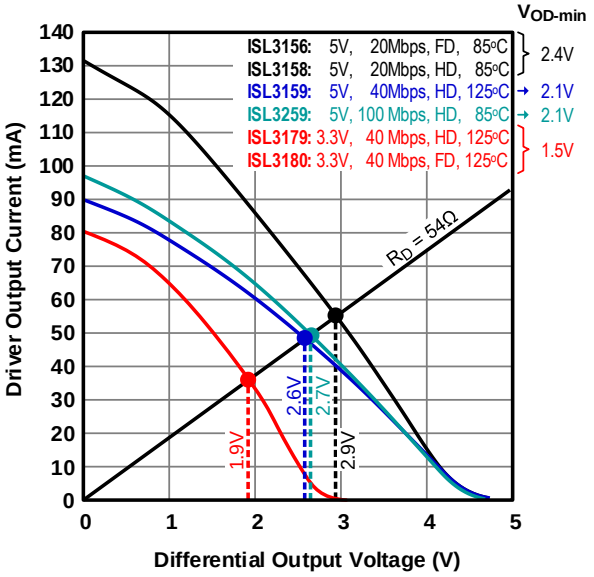

Figure 10. Renesas 3V and 5V high-speed transceivers greatly exceed the RS-485 specified minimum VOD of 1.5V

Figure 10 shows a wide selection of Renesas high-speed transceiver families with very high output drive capability. They offer a minimum V_{OD}s range from 160% of the specified 1.5V minimum at 4.5V supply down to 100% at 3.0V supply, thus delivering true 3V RS-485 compliant drive capability. The typical V_{OD}s measured at the highest operating temperatures even exceed RS-485 requirements by 27% for 3V and by 70% to 93% for 5V transceivers.

In addition, a small pulse skew minimizes transceiver contribution to the data link's total jitter budget. All Renesas high-speed transceivers are specified with a maximum pulse skew of 1.5ns. Having a small part-to-part skew is also important in synchronous applications, where the clock and data signals come from different transceivers and tight clock-to-data timing must be maintained.

Part-to-part skew is measured between any two transceivers under identical temperature and supply voltage test conditions. Because Renesas transceivers offer precise switching characteristics due to very low process variations, it is the only vendor of high-speed RS-485 transceivers specifying a part-to-part skew of ≤ 4ns.

Enhanced Robustness Features

To ease the process of network maintenance or the replacement of defective bus nodes during network operation, Renesas high-speed transceivers provide hot-plug capability as well as electrostatic discharge (ESD) immunity, conforming to IEC61000-4-2.

Hot plug capability ensures that during power up and power down, the transceiver's driver and receiver outputs maintain high-impedance, regardless of the logic state of the enable pins, DE and /RE. This prevents disturbances on the bus, which otherwise could falsely trigger other bus transceivers. It also gives the local node controller time to stabilize and drive the RS-485 control lines to the desired logic states.

The use of IEC61000-4-2 ESD protection circuitry safeguards the transceiver against damage from electrostatic discharges caused by field and maintenance personnel. Because these discharges occur in uncontrolled ESD environments, an IEC-ESD test generator creates transients with much shorter rise times and pulse widths, and significantly higher peak currents than an Human Body Model (HBM) ESD generator, whose application is intended for ESD controlled environments only (see Figure 11).

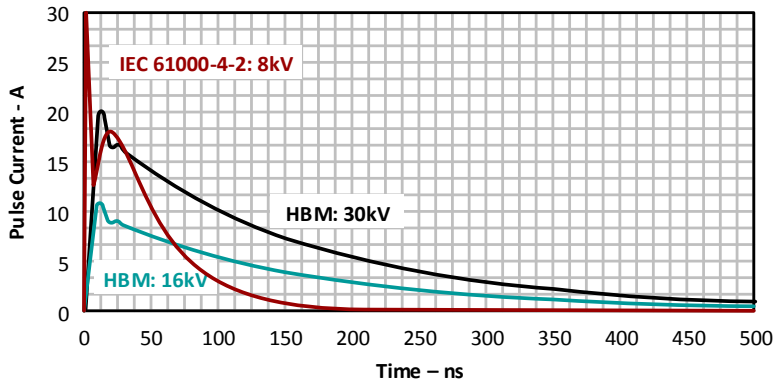

Figure 11. ESD transient comparison between IEC61000-4-2 and HBM

ESD protection structures designed for IEC61000-4-2 can often tolerate HBM test voltages of up to 2.5-times their IEC test voltage. Thus, an ESD structure designed for 8kV IEC contact discharge should be able to withstand a HBM contact discharge of up to 20kV. All Renesas high-speed transceivers are rated for the more stringent IEC-ESD requirements.

System Design Tips

Transmission Cable

RS-485 recommends the use of unshielded twisted pair (UTP) cable with a characteristic impedance of Z_0 = 120Ω nominal. Cables commonly used are either dedicated single-pair RS-485 cables with Z_0 = 120Ω or category 5 (CAT-5) cable with four signal pairs and Z_0 = 100Ω.

When using CAT-5 cable for single pair applications, the three unused signal pairs should be properly terminated to ground with R_T = 100Ω at both cable ends. This prevents noise coupling due to self-resonance at all sorts of frequencies from the unused wires into the data pair.

When selecting multi-pair cable other than CAT-5, do not use so-called “no-skew cable” as this is not intended for data transmission but rather for analog signals in high-resolution RGB video systems.

Multi-pair data cable is designed for the transmission of signals with large harmonic content. To avoid crosstalk between signal pairs each conductor pair receives a different twist rate. The difference in twist rates results in different pair-lengths and, hence, propagation delay differences, or cable skew.

No-skew cable, designed for analog signals with low or no harmonic content, use the same twist rate for all signal pairs, thus causing no skew. Transmitting data signals over this type of cable will result in large crosstalk and data errors.

Bus Termination

The RS-485 standard allows for two termination resistors, so high-speed data lines should always use termination resistors at both ends of the data link. The value of the termination resistors, R_T, should match the characteristic impedance of the cable, Z_0, or the characteristic impedance of the controlled-impedance transmission lines on a circuit board: $R_T = Z_0 = 100\Omega$.

Stub Length

The connection between a transceiver and the main data cable is known as a stub. A stub represents a piece of unterminated transmission line. Stubs must not be terminated in order to avoid excessive bus loading. Instead, their length should be kept short enough to prevent the build-up of signal reflections. A good approximation for calculating the maximum stub length is:

$$L_{Stub}(ft) = \frac{t_r(s)}{10} \times v \times c \qquad \text{EQ. 2}$$

where: L_{Stub} is the stub length (ft)
t_r is the driver rise time (s)
v = signal velocity as a percentage of c
c = speed of light (9.8×10^8 ft/s)

The minimum velocities of differential signals are 40% and 60% for FR4 printed circuit board (PCB) material and UTP cable, respectively. To prevent the transmission cable from contributing to stub length, connect the transceivers via daisy chaining to one another (see Figure 12).

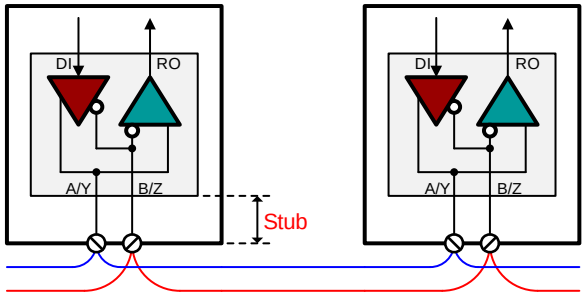

Figure 12. Daisy chaining bus transceivers makes PCB traces the only factor in stub length

Bus Node Design Tips

Component Layout

The pin-out of an RS-485 transceiver is tailored for a straightforward bus node design as the bus terminals (A/Y, B/Z) are located on one side of the IC, and the single-ended data lines (DI, RO) and control lines (DE, /RE) are on the opposite side (see Figure 13).

High-speed bus nodes require the application of controlled impedance transmission lines to assure low electromagnetic interference (EMI). On the bus side, the differential impedance of the bus traces must match the characteristic impedance of the transmission medium (100Ω or 120Ω). On the control side, the line impedance of the single-ended traces is commonly set to 50Ω.

Controlled impedance lines are accomplished through well-defined trace geometries (length, width, height, and trace spacing) and close electrical coupling with a low-inductance reference plane, either ground or power. This is easily accomplished with a bus node consisting of a transceiver and controller. However, if you add lightning protection components, such as the surge resistors and transient suppressors shown in Figure 13, the design quickly becomes more complicated.

In this case, the spacing of the differential traces is widened, which causes the differential impedance to deviate from its intended value. This constitutes an impedance discontinuity causing reflections and EMI. While discontinuities might be unavoidable, they should be lumped together to keep their area small.

To attain the required trace geometries accurately, use a field solver program. This software tool calculates characteristic impedance, signal speed, crosstalk and differential impedance. It also possesses the flexibility to consider almost any arbitrary cross section geometry. In addition to first-order terms such as line width, dielectric thickness and dielectric constant, second-order terms such as trace thickness, solder mask and trace etch-back can be considered.

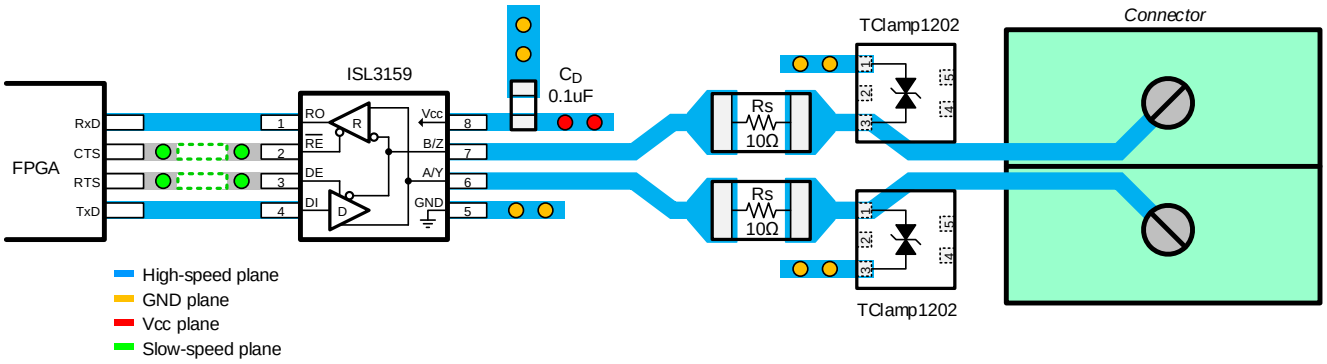

Figure 13. Suggested bus node layout with controller (FPGA), transceiver, surge proof resistors and transient suppressors for lightning protection

Layer Stack

A minimum of four layers are required to accomplish a low EMI PCB design (see Figure 14). Layer stacking should be in the following order (top-to-bottom): high-speed signal layer traces, ground plane, power plane and control signal layer, low-speed traces.

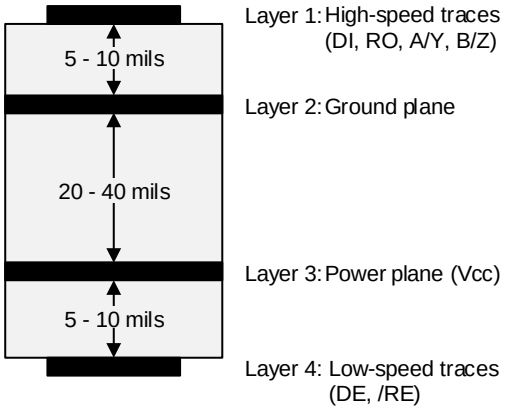

Figure 14. Recommended 4-layer stack for a bus node design

Routing the high-speed traces on the top layer avoids the use of vias (and the introduction of their inductances) and allows for clean interconnects from the bus connector to the transceiver bus terminals, and from the transceiver's high-speed single-ended data lines to the subsequent node controller circuit.

Placing a solid ground plane below the high-speed signal layer establishes controlled impedances for transmission line interconnects and provides an excellent low-inductance path for the return current flow. Placing the power plane below the ground plane creates additional high-frequency bypass capacitance.

Routing the slower speed control (enable) signals on the bottom layer allows for greater flexibility, as these signal links usually have margin to tolerate discontinuities such as vias, and the separation nearly eliminates crosstalk from the high-speed data traces.

Controlled Impedance Transmission Lines

The maximum length of the differential bus lines, or stub lengths, can be calculated with Equation 2, assuming a minimum signal velocity of 40% for FR4 material. With the driver rise time of the ISL3159E being 2ns, the maximum trace length is:

$$L_{Stub} = \frac{t_r}{10} \times v \times c \quad = \quad \frac{2 \times 10^{-9} s}{10} \times 0.4 \times 9.8 \times 10^8 \; ft/s \quad = \quad 0.078\, ft = 0.94\, in = 24\, mm$$

As previously mentioned, the data and control lines between transceiver and controller are designed for a 50Ω line impedance, which would require a 50Ω termination if their trace length exceeds a certain maximum. Because the receiver of the ISL3159E cannot drive such low impedance, the maximum trace length is calculated using Equation 2, again. For a microstrip line (that is a single-ended line close above a ground plane), the relative signal velocity, v, is 56%. With the receiver RO rise time of the ISL3159E being 2ns, the maximum trace length is:

$$L_{Trace} = \frac{t_r}{10} \times v \times c \quad = \quad \frac{2 \times 10^{-9} s}{10} \times 0.56 \times 9.8 \times 10^8 \; ft/s \quad = \quad 0.11\, ft = 1.32\, in = 33\, mm$$

Of course, if the FPGA's data output rise time (driving DI) is half the receiver's rise time, the maximum trace length will also be reduced by half.

Again, note that the traces of the enable signals, DE and /RE, change layers (from the top to the bottom layer) to prevent crosstalk from the high-speed data traces, DI and RO.

General High-Speed Design Guidelines

1) Use the smallest size possible for signal trace vias and connector pads so they have less impact on the 120Ω differential impedance. Large vias and pads can cause the impedance to drop below Z_0.

2) Use solid power and ground planes for impedance control and for minimum noise on the transceiver's power supply lines.

3) Keep the trace electrical length between the RS-485 connector and the transceiver as short as possible to minimize attenuation and reflection.

4) Place bulk capacitors (e.g., 10µF) close to power sources such as voltage regulators, or place them where the power is supplied to the PCB.

5) Place small 0.1µF and 0.01µF decoupling capacitors at the transceiver V_{CC} pin. Decoupling capacitors provide a local source of charge for ICs requiring a significant amount of supply current in response to internal switching. Insufficient decoupling causes a lack of supply current, which prevents the IC from working properly and results in data errors.

6) If vias are required, use multiple vias when connecting Vcc, GND, decoupling caps, and TVS diodes to high-speed ICs.

Conclusion

Renesas supports a wide range of high-speed RS-485 applications with a portfolio of high-speed and ultra-high-speed transceivers. The devices help designers overcome signal degradation issues through exceptionally high output drive capability and highly accurate switching performance for both 3.3V and 5V supplies. They also provide the highest robustness through hot plug capability and 16kV IEC61000-4-2 ESD immunity. Renesas transceivers are available in ultra-small, 3mm x 3mm DFN packages and support a wide operating temperature range from -45˚C to 125˚C.

Next Steps

- Find out more about the ISL3159E/79E
- Download the datasheets
- Watch an overview video
- Order free samples
- Learn more about Renesas' RS-485 solutions

# # #