

## Operational Amplifier

### Signal Gain versus Noise Gain and Input Referred Errors

#### Abstract

This document discusses the signal gain and noise gain for the non-inverting and inverting amplifier configurations and explains the various input referred error voltages.

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## 1. Signal Gain and Noise Gain of the Non-inverting Amplifier

The standard form of the amplifier output voltage,  $V_O = V_I \frac{A_{OL}}{1 + A_{OL} \beta}$  derived in TB514, Operational Amplifier Basics,

does not reveal by how much the amplifier's differential input voltage,  $V_{id}$ , is amplified towards the output.

However, this input voltage is the sum of all input referred error voltages, which are due to noise, finite open-loop gain, or common-mode and power-supply rejection. Therefore, it is good to know how much output error to expect that is due to the input referred errors being amplified by the circuit gain.

[Figure 1](#) shows the model for the non-inverting amplifier. The following loop equation shows the input voltage as the sum of the feedback and the differential input voltage,  $V_I = V_{id} + V_O$ . Then solving for  $V_O$  gives:

$$(EQ. 1) \quad V_O = \frac{1}{\beta} V_I - \frac{1}{\beta} V_{id} = \frac{1}{\beta} (V_I - V_{id})$$

This shows that for the non-inverting amplifier, the signal input and the differential input are equally amplified by the circuit gain,  $1/\beta$ , with  $V_{id}$  having the opposite polarity of  $V_I$ . Presenting  $V_{id}$  as an input error,  $E_I$ , then leads to the circuit diagram in [Figure 2](#).

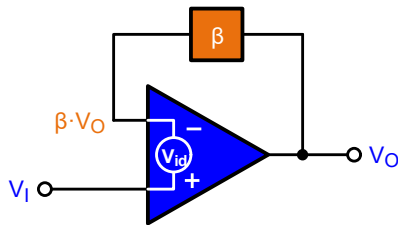


Figure 1. Non-inverting Amplifier Model

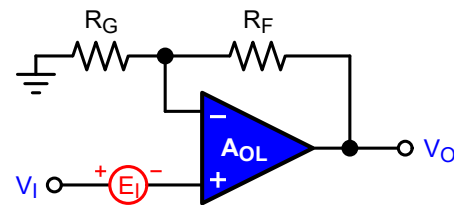


Figure 2. Non-inverting Amplifier with Error Voltage

## 2. Signal Gain and Noise Gain of the Inverting Amplifier

For the inverting amplifier configuration, the voltage at the inverting op-amp input is the sum of the signal input voltage attenuated by  $\alpha = R_F / (R_G + R_F)$  and the output voltage attenuated by  $\beta = R_G / (R_G + R_F)$ . This makes  $\alpha = 1 - \beta$ .

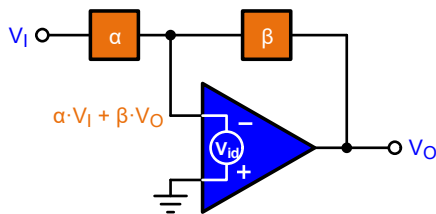


Figure 3. Inverting Amplifier Model

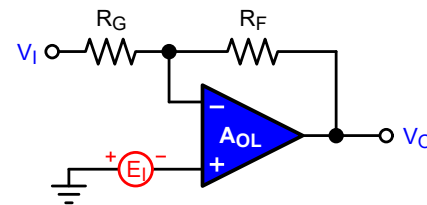


Figure 4. Inverting Amplifier with Error Voltage

Writing the loop equation for the inverting amplifier with  $0 = V_{id} + V_I(1 - \beta) + V_O \beta$  and solving for  $V_O$  results in:

$$(EQ. 2) \quad V_O = -V_I \left( \frac{1}{\beta} - 1 \right) - \frac{1}{\beta} V_{id}$$

[Equation 2](#) confirms the fact that the signal gain of the inverting amplifier is  $1V/V$  less than the  $1/\beta$  of the non-inverting amplifier, and the negative sign in front of  $V_I$  indicates the  $180^\circ$  phase inversion. However,  $V_{id}$  is amplified by the non-inverting gain,  $1/\beta$ , and therefore assigned to the non-inverting input. Then, replacing  $V_{id}$  through  $E_I$  results in the circuit diagram in [Figure 4](#).

Comparing [Equation 1](#) and [Equation 2](#) shows that independent of the amplifier configuration, the input error, or input noise, is amplified by the non-inverting gain,  $1/\beta$ , which is also known as noise gain.

### 3. Input Referred Errors

As mentioned earlier in this document, the differential input voltage is the sum of all the following:

- Input referred noise or error voltages including the input offset voltage
- Offset voltage due to bias current flowing through the biasing resistors
- Internal noise voltage
- Signal error due to finite open-loop gain
- Input errors due to common-mode and power-supply rejection.

$$V_{id} = V_{OS} + I_{B+} \cdot R_S - I_{B-} \cdot R_S + V_n + \frac{V_O}{A_{OL}} + \frac{\Delta V_{CM}}{CMRR} + \frac{\Delta V_S}{PSRR}$$

### 4. Input Offset Voltage ( $V_{OS}$ )

When both op-amp inputs have the same input potential, the output of an ideal op-amp should be 0V. For a practical op-amp (OPA) however, this is usually not the case. Here, the parameter mismatch of the input transistors causes a slight difference in bias voltage (see Figure 5), making  $V_O \neq 0V$  (see Figure 6). This difference is known as the offset voltage,  $V_{OS}$ . To measure  $V_{OS}$ , an external voltage ( $V_{EXT}$ ) is applied to the non-inverting input and adjusted until  $V_O = 0V$ . At this moment  $V_{EXT} = -V_{OS}$  (see Figure 7).

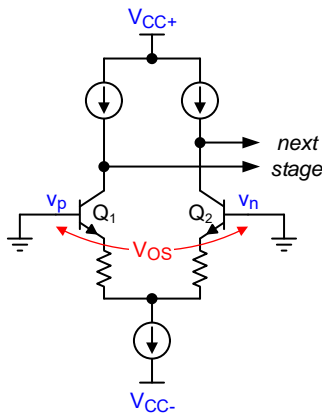


Figure 5. Mismatch in Transistor Parameters Causes  $V_{OS}$

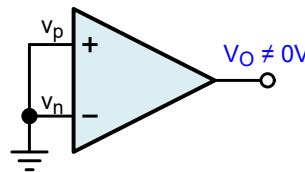


Figure 6. Grounding Both Inputs Still Produces  $V_O$

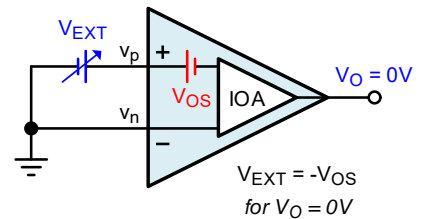


Figure 7. Adjusting  $V_{EXT}$  until  $V_O = 0V$  Makes  $V_{EXT} = -V_{OS}$

Therefore, a practical op-amp can be modeled as an ideal op-amp (IOA) with an offset voltage in series to its non-inverting input (see Figure 8). The input offset is also known as DC noise.

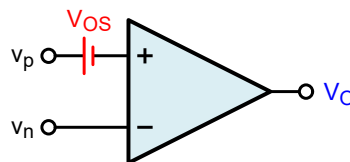
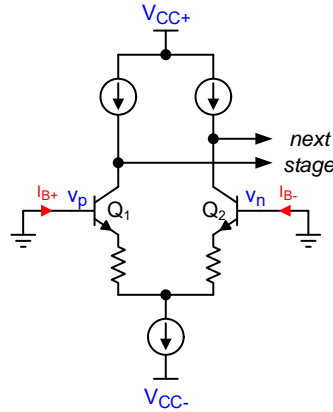


Figure 8.  $V_{OS}$  Model of Practical Op-amp

## 5. Input Bias Current ( $I_B$ )

Input bias currents are necessary because they determine the operating point of the input of the op-amp input stage transistors (see [Figure 9](#)). For NPN transistors these currents flow into the device; for PNP transistors they flow out of the device. In fact, both inputs must see a DC current path to ground for the bias currents to flow; otherwise, the op-amp does not work.



**Figure 9. Input Stage with  $I_{B+}$  and  $I_{B-}$**

Due to the mismatch of the transistor current gains, the bias current into the non-inverting input,  $I_{B+}$ , differs from the bias current into the inverting input,  $I_{B-}$ . Datasheets usually do not specify the bias currents individually but instead provide an average bias,  $I_B$ , and an offset current,  $I_{OS}$ . Their definitions are listed in [Equation 3](#) and [Equation 4](#).

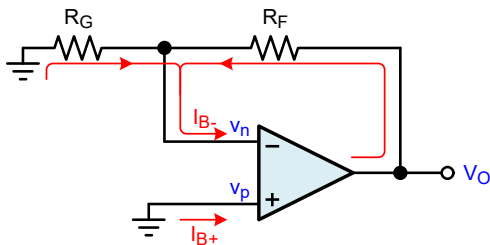
$$(EQ. 3) \quad I_B = \frac{I_{B+} + I_{B-}}{2} \quad \text{and} \quad (EQ. 4) \quad I_{OS} = I_{B+} - I_{B-}$$

**Note:**  $I_{OS}$  is usually a magnitude smaller than  $I_B$ .

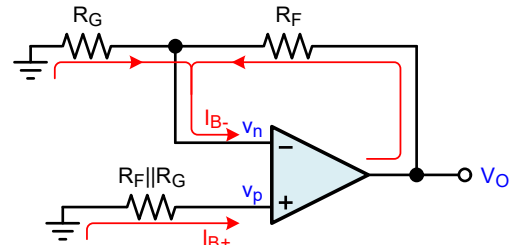
Through mathematical manipulation of [Equation 3](#) and [Equation 4](#), the individual bias currents are identified as:

$$(EQ. 5) \quad I_{B+} = I_B + \frac{I_{OS}}{2} \quad \text{and} \quad (EQ. 6) \quad I_{B-} = I_B - \frac{I_{OS}}{2}$$

The signal error caused by bias currents is due to the voltage drops they cause across the feedback and gain resistors. However, a simple error-compensation technique can be used to minimize this error. The following section discusses the signal error for the uncompensated and compensated case.



**Figure 10. Uncompensated Error Due to  $I_{B-}$  Flowing through  $R_F$  and  $R_G$**



**Figure 11. Compensated Error Due to  $R_p$  Reducing the Potential at  $v_p$**

To determine  $V_O$  due to bias current flow, we define  $I_{B-}$  as the sum of the two individual currents flowing into the  $v_n$  node, and then solve for  $v_n$ .

$$I_{B-} = \frac{-v_n}{R_G} + \frac{V_O - v_n}{R_F} \quad \Rightarrow \quad v_n = \frac{V_O}{1 + R_F/R_G} - I_{B-} R_G \parallel R_F$$

Due to op-amp action,  $v_n = v_p$ , we define  $v_p$  for the uncompensated and the compensated case and solve for  $V_O$ .

In the uncompensated case  $v_p = 0V$ , thus:

$$0 = \frac{V_O}{1+R_F/R_G} - I_{B-} R_G \parallel R_F$$

And solving for  $V_O$  gives:

$$V_O = (1+R_F/R_G) \cdot (R_F \parallel R_G) \cdot I_{B-}$$

Finally substituting  $I_{B-}$  with [Equation 6](#) results:

$$V_O = (1+R_F/R_G) \cdot (R_F \parallel R_G) \cdot (I_B - I_{OS}/2)$$

with the input error,  $E_I$ , being:

$$E_I = (R_F \parallel R_G) \cdot (I_B - I_{OS}/2)$$

In the compensated case  $v_p = -I_{B+} \cdot (R_F \parallel R_G)$ , thus

$$-I_{B+} R_G \parallel R_F = \frac{V_O}{1+R_F/R_G} - I_{B-} R_G \parallel R_F$$

And solving for  $V_O$  gives:

$$V_O = (1+R_F/R_G) \cdot (R_F \parallel R_G) \cdot (I_{B-} - I_{B+})$$

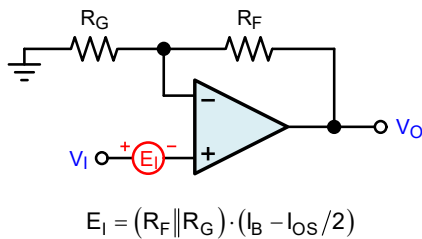
Finally substituting  $-(I_{B+} - I_{B-})$  with [Equation 4](#) results:

$$V_O = (1+R_F/R_G) \cdot (R_F \parallel R_G) \cdot (-I_{OS})$$

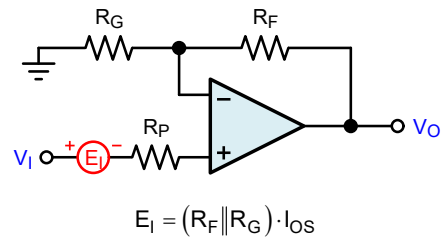
with the input error,  $E_I$ , being:

$$E_I = (R_F \parallel R_G) \cdot (-I_{OS})$$

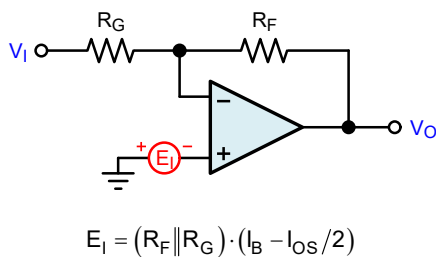
In both cases the input error is amplified by the non-inverting gain and therefore placed in series with the non-inverting input. As both amplifier inputs have been grounded for error analysis, the above models apply equally to the non-inverting and inverting amplifier configurations. [Figure 12](#) to [Figure 15](#) show the respective schematics.



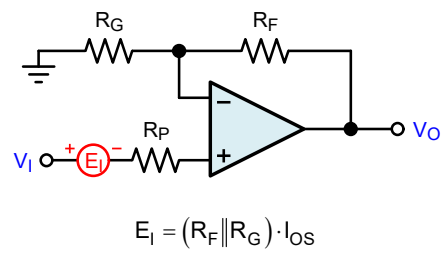
**Figure 12. Uncompensated Case of the Non-inverting Amplifier**



**Figure 13. Compensated Case of the Non-inverting Amplifier**



**Figure 14. Uncompensated Case of the Inverting Amplifier**



**Figure 15. Compensated Case of the Inverting Amplifier**

### 6. Finite Open-Loop Gain ( $A_{OL}$ )

As already shown in [Figure 1](#) and [Figure 3](#), even a noiseless op-amp requires a minimum differential input,  $V_{ID-min}$ , to sustain the desired output voltage. This  $V_{ID-min}$  is the ratio of the output voltage divided by the finite open-loop gain, and thereafter, represents an input error in itself:  $E_1 = V_O/A_{OL}$  (see [Figure 16](#)).

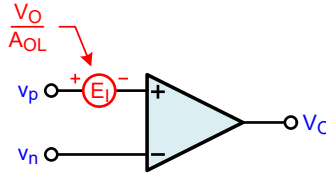


Figure 16. Input Error Due to Finite  $A_{OL}$

Entering this input error into Equations 1 and 2 and solving for  $V_O/V_I$  confirms the closed loop gains,  $A_{CL(non)}$  and  $A_{CL(inv)}$ , for the non-inverting and inverting amplifier, respectively.

$$V_O = \frac{1}{\beta} V_I - \frac{1}{\beta} V_{id-min} = \frac{1}{\beta} \cdot V_I - \frac{1}{\beta} \cdot \frac{V_O}{A_{OL}} \Rightarrow \frac{V_O}{V_I} = -\left(\frac{1}{\beta} - 1\right) \cdot \frac{1}{1 + \frac{1}{A_{OL}\beta}} = A_{CL(inv)}$$

$$V_O = -V_I \left(\frac{1}{\beta} - 1\right) - \frac{1}{\beta} V_{id} = -V_I \left(\frac{1}{\beta} - 1\right) - \frac{1}{\beta} \cdot \frac{V_O}{A_{OL}} \Rightarrow \frac{V_O}{V_I} = \frac{1}{\beta} \cdot \frac{1}{1 + \frac{1}{A_{OL}\beta}} = A_{CL(nin)}$$

### 7. Common-Mode Rejection Ratio (CMRR)

In the absence of input offset, an op-amp should respond only to the voltage difference between its inputs, so that  $V_O = A_{DM}(v_p - v_n)$ . However, a practical op-amp is also somewhat sensitive to changes in the common-mode input voltage (see [Figure 17](#)). This is because a change in  $V_{CM}$  changes the operating point of the input transistors (see [Figure 18](#)). The op-amp's transfer characteristic is therefore:

(EQ. 7)  $V_O = A_{DM}(v_p - v_n) + A_{CM} \cdot \Delta V_{CM}$

where  $A_{DM}$  is the differential-mode open-loop gain,  $A_{OL}$ , and  $A_{CM}$  is the common-mode gain.

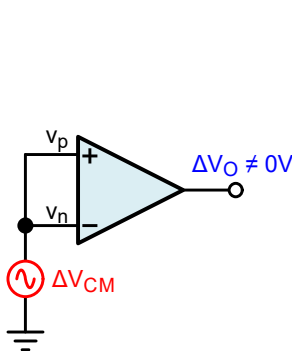


Figure 17. Changes in  $V_{CM}$  Cause Changes in  $V_O$

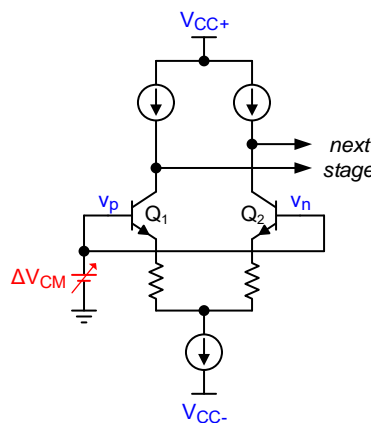


Figure 18.  $V_{CM}$  Alters Operating Points of  $Q_1$  and  $Q_2$

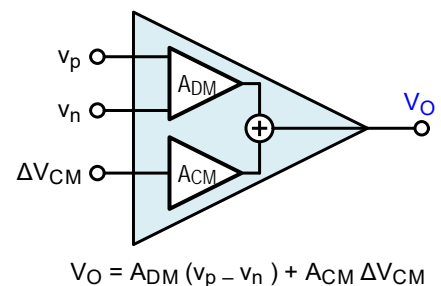


Figure 19. Op-amp Transfer Characteristic with  $V_{CM}$

Because the impact of common-mode voltage is undesired, an op-amps capability to reject common-mode signals is specified by its common-mode rejection ratio, CMRR, which is the ratio of differential-mode gain to common-mode gain:  $CMRR = A_{DM}/A_{CM}$ . Using this ratio to express the output voltage, we rewrite Equation 7 in the form:  $V_O = A_{DM}[v_p - v_n + (A_{CM}/A_{DM}) \cdot \Delta V_{CM}]$ , and substitute the term  $A_{DM}/A_{CM}$  through  $1/CMRR$ , so that:

$$(EQ. 8) \quad V_O = A_{DM} \left( v_p + \frac{\Delta V_{CM}}{CMRR} - v_n \right)$$

Thus, the ratio  $\Delta V_{CM}/CMRR$  represents an input error voltage,  $E_I$ , that is in series with the non-inverting input,  $v_p$ , and therefore amplified with the non-inverting gain:  $E_I = \Delta V_{CM}/CMRR$ .

The input error due to  $V_{CM}$  differs from the input errors due to  $V_{OS}$  and  $I_B$  in two points:

1.  $\Delta V_{CM}/CMRR$  is frequency dependent because CMRR is frequency dependent. At low frequencies, CMRR can reach high values in the range of 80 to 140dB, depending on the type of op-amp. At high frequencies, CMRR rolls off at a rate of 20db/decade (see [Figure 20](#)).

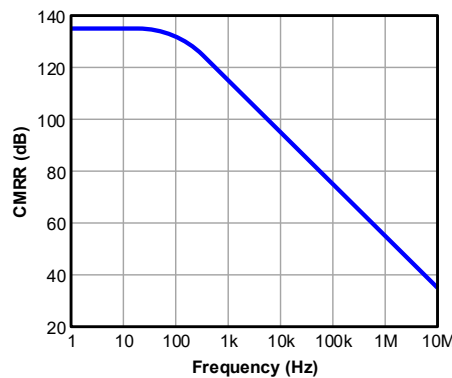


Figure 20. CMMR over Frequency

2.  $\Delta V_{CM}/CMRR$  differs between the non-inverting and inverting amplifier configurations due to the difference in  $\Delta V_{CM}$  between the two.

Because op-amp action ensures that  $v_p = v_n$ ,  $v_p$  becomes the common-mode input voltage for the op-amp. For the non-inverting amplifier this means that  $\Delta v_p = \Delta v_n = \Delta V_{CM}$  and the input error becomes rather large. However, for the inverting amplifier,  $v_p$  is connected to a constant reference potential. This makes  $\Delta v_p = \Delta V_{CM} = 0V$  and the input error equals zero. Therefore, applications with large input signal swings can apply the inverting configuration to eliminate common-mode error.

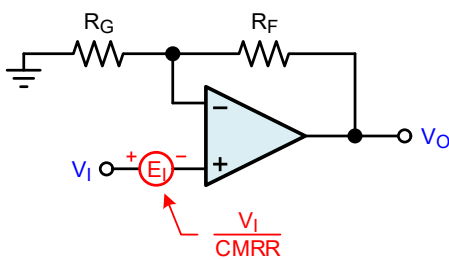


Figure 21. Non-inverting Amplifier with Common-mode Error:  $E_I = V_I / CMRR$

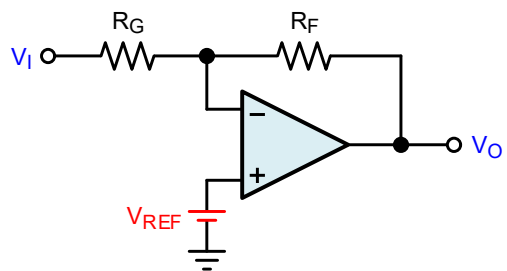


Figure 22. Inverting Amplifier with no Common-mode Error

### 8. Power-Supply Rejection Ratio (PSRR)

Like the common-mode phenomenon, changes in the op-amp the power supply causes changes in the output voltage (see [Figure 23](#)). This is because a change in  $V_S$  alters the operating point of the input transistors (see [Figure 24](#)). An op-amp's capability to reject supply changes is expressed through its power supply rejection ratio, or PSRR (see [Figure 25](#)).

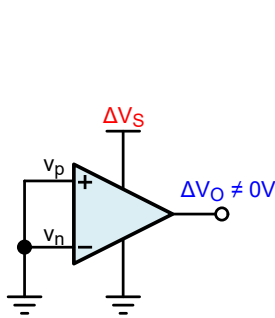


Figure 23. Changes in  $V_S$  Cause Changes in  $V_O$

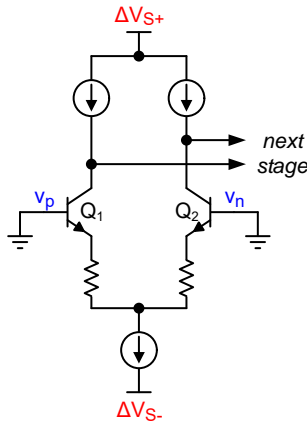


Figure 24.  $\Delta V_S$  Alters Operating Points of  $Q_1$  and  $Q_2$

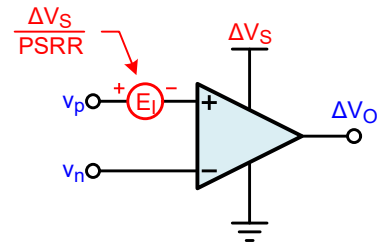


Figure 25. Input Error Due to Supply Changes,  $\Delta V_S$

In analogy to the CMRR, the PSRR can be modeled as an input error,  $E_I = \Delta V_S / PSRR$ , which is in series with the non-inverting input and is amplified with the non-inverting gain (see [Figure 25](#)). Like CMRR, the PSRR is frequency dependent with high values at low frequencies and a 20dB/decade roll-off at high frequencies (see [Figure 26](#)).

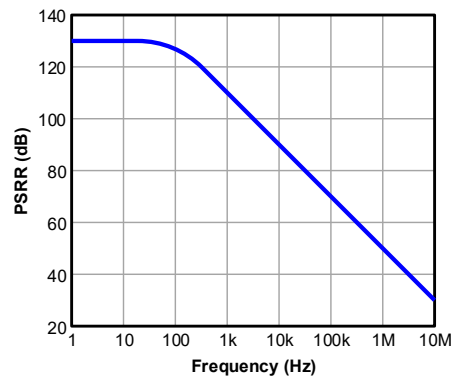


Figure 26. PSRR over Frequency

Unlike the input error due to CMRR, the input error due to PSRR affects the non-inverting and inverting amplifier configurations equally.

### 9. Conclusion

The op-amp input referred errors can be modeled as input error voltages assigned to the non-inverting op-amp input. Apart from the CMRR induced error, all other error voltages are amplified by the non-inverting gain (such as noise gain, independent of the amplifier configuration). The CMRR induced error,  $\Delta V_{CM} / CMRR$ , does not exist in the inverting amplifier; it is only present in the non-inverting amplifier.

### 10. Revision History

| Rev. | Date     | Description     |
|------|----------|-----------------|
| 1.00 | Oct 2.19 | Initial release |



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