

## Introduction

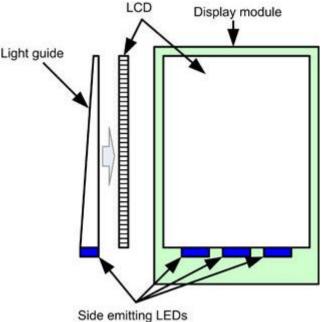
DC-DC voltage converters are widely used in applications ranging from consumer electronics to high-power energy conversion systems. Among these, flyback converters are popular for low power applications such as backlighting for LCD monitors and TV's, micro pumps (i.e. microbiological experiments), piezo electronics, and Geiger Counter tubes.

This kind of flyback converter is highly scalable and reusable for applications ranging from 30V to 450V by simply varying configuration parameters of a GreenPAK<sup>™</sup> IC.

For instance, High-voltage LEDs offer the optimum solution for indoor retrofit lamps. High-voltage LEDs usually have a higher turn-on voltage, greater than 20V, as compared to conventional LEDs which is typically around 3V (for white LEDs). This low current high voltage architecture enables simpler, smaller, cheaper and more efficient driver topologies. A high voltage low current LED string matches the LED output voltage more closely to its AC input voltage as compared to a low voltage high current string, utilizing the same number of LEDs and lumen output.

For LCD backlight lamps, the LEDs are on the edge of the display, and a light guide plate aids in achieving uniform backlighting. White LEDs usually employ a constant-current drive using a pulse-width modulation (PWM) for dimming control. You can drive the LEDs in series through the fly back converter in order to produce enough voltage to illuminate a large LED string. Along with easy control, series connections also simplify pc-board routing and enable optimum current matching between LEDs. Therefore, series connection is the preferred approach.

In medical or biological devices for precision controlled liquid delivery, such as infusion pumps, insulin pumps or nebulizers, piezoelectric micropumps offer an attractive alternative to standard pumps.



Side emitting LEDS

#### Figure 1. Display monitor structure

Piezoelectric micropumps are small, lightweight, low power, low cost, and accurate. They are miniaturized mechanical pumping devices employing a piezoelectric actuator in combination with passive check valves. When voltage is applied, a piezoelectric actuator expands or contracts, which causes the liquid or gas to be sucked into or expelled from the pump chamber. The check valves on both sides of the pump chamber govern the flow in one direction.

Flyback converters benefit from galvanic insulation, multi input and/or output stages, compactness and simple construction. Their key component is the high frequency transformer. A detailed explanation of the DC-DC fly-back converter using the GreenPAK technology will be presented which can dynamically control the output voltage. Simulation results and design steps will be shown in detail. The GreenPAK offers a new point of view to develop applications by merging analog and digital configurable blocks.

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The main advantages are miniaturization, flexibility of multiple configurations, and simple programming. Complex circuits can be realized by mixing analog and digital elements without requiring another programming language.

In this application example we will show how the GreenPAK can be used to:

1. Read the analog output voltage for feedback control

2. Comparing read voltage with a fixed value chosen for delivery the exact output voltage

3. Pulse width modulation in order to drive the power MOSFET

4. Precise operation sequencing through the internal Oscillator.

# Flyback Operating Principles and Model

The basic topology of a fly-back circuit is shown in Fig. 1. When a MOSFET is switched ON and a voltage is applied to the primary winding, the primary current rises linearly. The change of input current is determined by the input voltage, the transformer primary inductance, and the on time. During this time, the energy is stored in the core of the transformer. The output Diode D1 is reverse biased, due to the voltage induced by the primary, and the energy is not transferred to the output load.

The current in the primary rises linearly

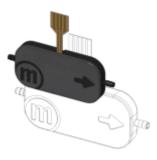
$$\mathbf{I} = \frac{\mathbf{V}_{\mathrm{IN}}}{L_1} t$$

And the voltage in the secondary is:

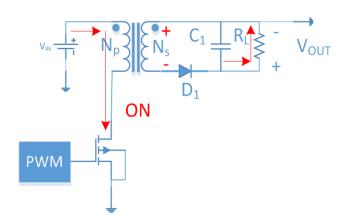
$$V_{SEC} = N_S V_{IN}$$

So the Reverse voltage of the diode should be at least

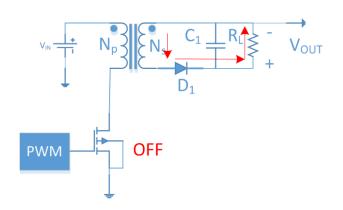
$$V_{Rev} = N_S V_{IN} + V_{OUT}$$















When the MOSFET switches off, the energy accumulated in the primary is:

$$E = \frac{1}{2} LI^2$$

Due the fact the primary is opened, the voltage is induced in the secondary and the diode is forward biased. The current is fixed by the transformer ratio:

$$n = \frac{N_S}{N_p}$$
$$I_S = \frac{I_p}{n}$$

And the voltage:

$$V_S = V_{OUT} + V_D$$

If the voltage drop across the switching MOSFET and the output rectification diode are ignored, the voltage during the on time ( $T_{ON}$ ) should be equal to the voltage during the off time ( $T_{OFF}$ ), in steady state operation:

$$V_{IN} T_{ON} = V_{OUT} \frac{N_p}{N_s} T_{OFF}$$

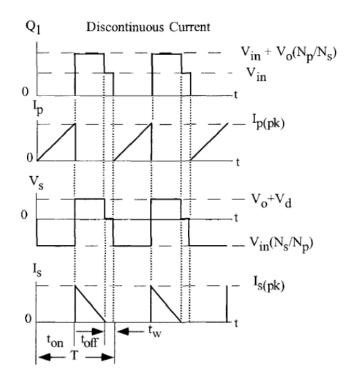
If we define D as the duty cycle:

$$D = \frac{T_{ON}}{T_{ON} + T_{OFF}}$$

We can obtain the relationship between turn ratio and input voltage to the output voltage:

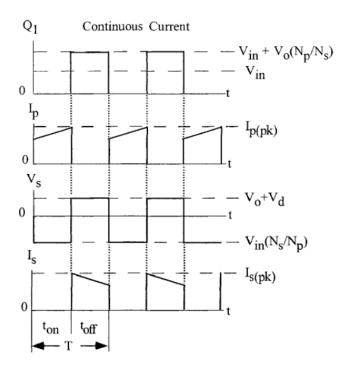
$$V_{OUT} \approx V_{IN} \frac{D_{MAX}}{1 - D_{MAX}} \frac{N_S}{N_p}$$

The increase of maximum duty cycle reduces the peak current in the primary of the transformer, resulting in better transformer utilization in the primary, and lower ripple on the input source. At the same time, the increase of the maximum duty cycle increases the maximum stress voltage between drain to source of the main switching MOSFET, and increases the peak current on the secondary side. A flyback converter has two different modes of operation, discontinuous mode and continuous mode. In the discontinuous mode, all the energy stored in the primary during the on time is completely delivered to the secondary and to the load before the next cycle, and there is also a dead time between the instant the secondary current reaches zero and the start of the next cycle. In continuous mode, there is still some energy left in the secondary at the beginning of the next cycle. The flyback can operate in both modes, but it has different characteristics.



#### Figure 5. Discontinuous Current Mode

The discontinuous mode has higher peak currents, and therefore it has higher output voltage spikes during the turn-off.



### Figure 6. Continuous Current Mode

On the other hand, it has faster load transient response, lower primary inductance, and therefore the transformer can be smaller in size. The reverse recovery time of the diode is not critical because the forward current is zero before the reverse voltage is applied. Conducted EMI noise is reduced in discontinuous mode because transistor turn-on occurs with zero drain current.

The continuous mode has lower peak currents, and therefore, lower output voltage spikes. Unfortunately, it makes the control loop more complicated because of its right half plane (RHP) zero that forces to reduce the overall bandwidth of the converter.

## **Flyback Circuit Design and Simulation**

In order to verify the circuit design, a simulation in PSpice has been performed.

A transformer with turn ratio 1:10 has been chosen with an input voltage of 5V. R1 and C3 components form a snubber network to protect the MOS1 transistor from high voltage spikes.

Si7898DP is a high voltage N-channel MOSFET with 150V Maximum Drain voltage and low drainsource resistance ( $R_{DS-ON}0.095$  @I<sub>D</sub> = 3A and  $V_{GS}$  = 6V). The diode has been chosen with high speed (Reverse Recovery<4ns) and high peak reverse voltage (100V). The two capacitors are suited for high voltage applications with a maximum voltage rate of 1000V.

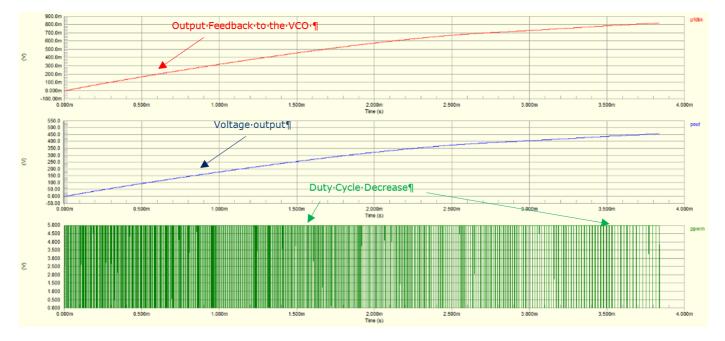
The PWM signal which drives the MOSFTET is simulated by a voltage controlled oscillator (VCO-Sqr) and it will be generated by the GreenPAK. The control signal is the voltage on the resistor divider  $R_2$  and  $R_3$  that acts as feedback of the output.

In the first graph (red line) the feedback voltage scaled by the divider is sent to the Pulse width modulator. By this, the Voltage controlled oscillator sets the duty cycle to the MOSFET (green line in the third graph). As shown, the duty cycle and the frequency decrease when the voltage goal is reached.

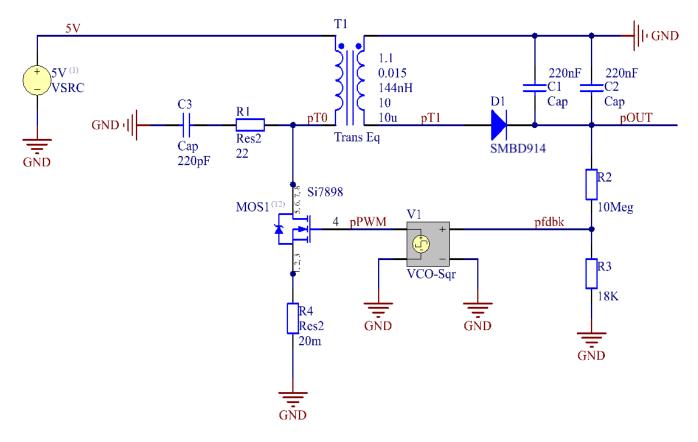
The VCO generates a square wave (green line Fig. 9) of 200kHz, and at every falling edge the energy stored in the transformer is delivered to the load, increasing the output voltage. The voltage increase in the load is reflected on the primary and attenuated by the RC snubber network.















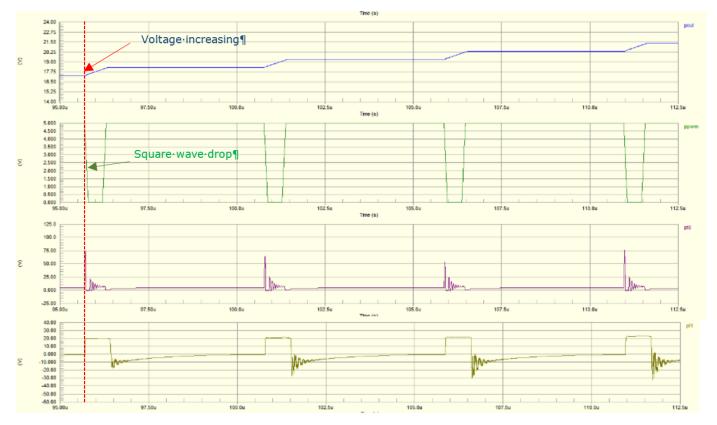


Figure 9. Enlarged Graph Simulation

## **GreenPAK Design**

The heart of the flyback converter is the GreenPAK4. It converts the output voltage from the divider to a pulse width modulation in which the duty cycle varies in order to obtain the prefixed output voltage. When the output voltage is lower than a prefixed threshold, the duty cycle is maximized to reach that voltage, then the duty cycle decreases and the output voltage becomes stable. Our purpose is to arrive at 450V, and for this reason an external power supply has been used through an USB connection.

The Voltage at GreenPack 4 on PIN 6 is the output feedback control and it's compared through the ACMP0 to the DAC0 output. This value is set as the goal voltage to reach by the output:

 $V_{OUT} \frac{R3}{R3 + R2} = 450V \frac{18k\Omega}{18k\Omega + 10M\Omega} = 0.809$ 

The DAC register is set to 206 which means:

$$V_{REF_{DAC}} * \frac{206}{255} = 1V \frac{206}{255} = 0.808$$

In this way, when the voltage at the input pin 6 is lower than the DAC output value the Analog Comparator goes down, and through INV0 the counter is up counting. The CNT8 is set initially to 255 and the difference between the two signals is always positive and duty cycle is maximum (99.6%) in order to obtain the desired output voltage value. When the Voltage reaches 0.808V the ACMP goes low, INV0 goes high, the counter is down counting and the DUTY cycle decreases.

To set a different voltage, exactly the same configuration can be maintained and only a software change is required. By following the previous equation for 250V and 100V we can obtain:



$$V_{OUT_{250V}} \frac{R3}{R3 + R2} = 250V \frac{18k\Omega}{18k\Omega + 10M\Omega} = 0.449$$

And the DAC register should be set through the following equation to 115:

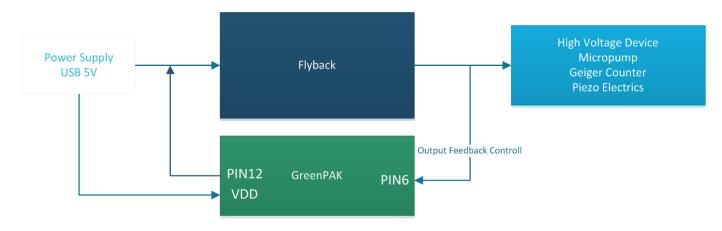
$$V_{REFDAC} * \frac{N_{Step}}{255} = 0.449 => 1V \frac{N_{Step}}{255} = 0.449 => N_{Step} = 0.449V * \frac{255}{1V} = 115$$

In the same way for 100V we obtain:

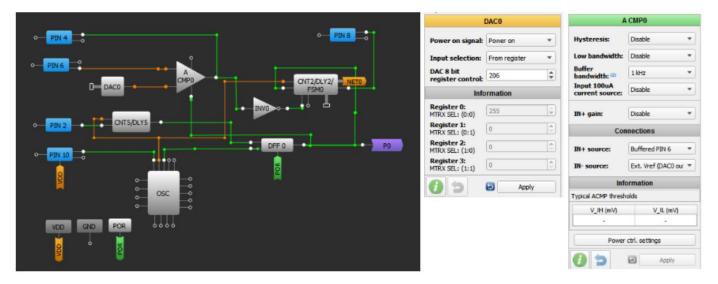
$$V_{REFDAC} * \frac{N_{Step}}{255} = 0.180 => 1V \frac{N_{Step}}{255} = 0.180 => N_{Step} = 0.180V * \frac{255}{1V} = 46$$

### **GreenPAK Simulation and Validation**

The PWM generator of the flyback circuit was simulated using Proteus© simulation suite. Figure shows the digital simulation diagram of the PWM generation section. Starting from the left, two resistors simulate the voltage divider at the flyback output stage. The divider input was simulated with a sinusoidal generator having approx. 5V DC offset. This means that the IN+ of the comparator is at 2.5V with an AC coupled sinusoid of 200mV peak to peak.

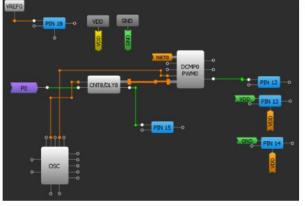


#### Figure 10. Flyback System Design









Mode:	Counter/PWM ramp	•
Counter data:	255	Ŷ
	(Range: 1 - 255)	
Output period (typical):	9.48148 us Formu	de la
Edge select:	Both	•
Counter value control:	None	-
DFF bypass enable:	None	,
Co	nnections	
FSM data:	None	•
Clock:	Ring OSC CLK	•
Clock source:	Ring OSC Freq.	
Clock frequency:	27 MHz	
6 5	Apply Apply	

DCM	PO/PWM0	
DCMP/PWM power register:	Power on	
Function selection:	PWM	•
PD sync to clock:	off	•
Clock source:	OSC X CLK	
Clock invert:	Disable	
PWM & ADC clock source :	RC OSC	*
PWM data sync with SPI clock:	Disable	*
Duty cycle:	0%-99.6%	•
PWM deadband time:	10 ns	•
Register 0: MTRX SEL: (0:0)	255	1
Register 1: MTRX SEL: (0:1) 4		ł
Register 2: MTRX SEL: (1:0)	0	1
Panister 3	0	4
Con	nections	
IN+ selector:	F5M0 [7:0]	•
IN-selector:	CNT8 -> Q [7:0]	•
0 5	Acoly	

		OS	it.	
LF OSC	RC OS	C	RING OSC	
RC OSC p mode:	ower	AU	to power on	
RC 05C frequency: RC matrix power down:		25 kHz		*
		Disable 1 1		*
RC clock predivider by: 'OUTO' second divider by:				
Clock se	lector:	RC OSC		٣
	Inf	orm	ation	
Notes				
for OSC (M Clock out		fiqu	ration	
RC OSC	Output		Value	
RC OSC	NUS BARRON			
	NUS BARRON	R	Value	
OUTO	NUS BARRON	R	Value OSC Freq.	2
OUTO CLK /4	NUS BARRON	RORO	Value COSC Freq. COSC Freq. /4	
OUTO CLK /4 CLK /12	NUS BARRON	R( R( R(	Value OSC Freq. OSC Freq. /4 OSC Freq. /1	4
OUT0 CLK /4 CLK /12 CLK /24	Output	R( R( R( R(	Value COSC Freq. /4 COSC Freq. /1 COSC Freq. /2	4
OUT0 CLK /4 CLK /12 CLK /24 CLK /64	Output	R( R( R( R( LF	Value COSC Freq. /4 COSC Freq. /4 COSC Freq. /2 COSC Freq. /2 COSC Freq. /6	4
OUTO CLK /4 CLK /12 CLK /24 CLK /64 LF OSC C	Output	RC RC RC RC RC RC RC RC	Value OSC Freq. /4 OSC Freq. /1 OSC Freq. /2 OSC Freq. /6 OSC Freq.	4
OUTO CLK /4 CLK /12 CLK /24 CLK /64 LF OSC CL Ring OSC	Output	RO RO RO RO RO RO RO RO RO RO RO RO RO R	Value OSC Freq. /4 OSC Freq. /1 OSC Freq. /2 OSC Freq. /6 OSC Freq. ng OSC Freq.	4
OUT0 CLK /4 CLK /12 CLK /24 CLK /64 LF OSC CL Ring OSC OUT1	Output LK ; CLK	R( R( R( R( R( R( R( R( R( R( R( R( R( R	Value COSC Freq. /1 COSC Freq. /1 COSC Freq. /2 COSC Freq. /6 OSC Freq. ng OSC Freq. ng OSC Freq.	4
OUT0 CLK /4 CLK /12 CLK /24 CLK /64 LF OSC CL Ring OSC OUT1 ADC CLK	Output LK CLK /256	RO RO RO RO RO RO RO RO RO RO RO RO RO R	Value OSC Freq. /4 OSC Freq. /4 OSC Freq. /2 OSC Freq. /6 OSC Freq. /6 OSC Freq. ng OSC Freq. ng OSC Freq. OSC Freq.	4
OUTO CLK /4 CLK /12 CLK /24 CLK /64 LF OSC CL Ring OSC OUT1 ADC CLK ADC CLK	Output LK CLK /256	RC RC RC RC RC RC RC RC RC RC RC RC RC R	Value COSC Freq. /4 COSC Freq. /4 COSC Freq. /2 COSC Freq. /2 COSC Freq. ng OSC Freq. ng OSC Freq. COSC Freq. COSC Freq. COSC Freq. /2	4
OUTO CLK /4 CLK /12 CLK /24 CLK /64 LF OSC CL Ring OSC OUT1 ADC CLK ADC CLK EXT, CLK0	Output LK CLK /256	RC RC RC RC RC RC RC RC RC RC RC RC RC R	Value COSC Freq. /4 COSC Freq. /4 COSC Freq. /2 COSC Freq. /2 COSC Freq. /6 OSC Freq. Mg OSC Freq. COSC Freq. COSC Freq. /2 COSC Freq. /2 COSC Freq. /2 COSC Freq. /2	4

Figure 12. GreenPAK Matrix 1 Design

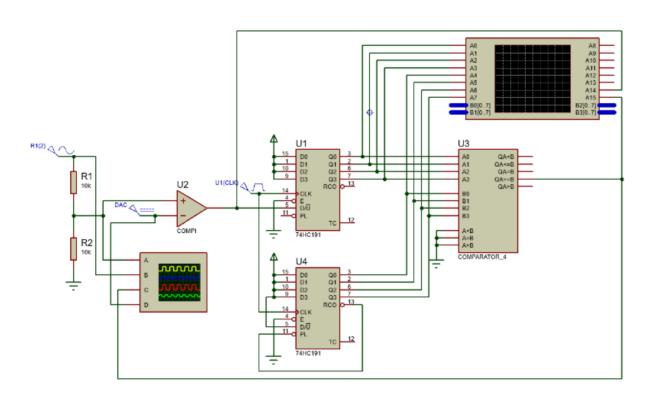


Figure 13. PWM digital Simulation



The sinusoid variations around the DC value simulate the variation of the high voltage output around the setpoint of 450V. A fixed voltage reference of 2.5V is connected to the inverting input of the comparator. The constant voltage simulates the output of the GreenPAK DAC. The discrete counter U4 simulates the GreenPAK ramp generator (i.e. CNT8/DLY8). It's a free running counter starting from the maximum value toward the zero value. In fact, due to the connection of the pin D/ $\overline{U}$  to the high level, it is in down counter mode. The counter U1 is in free running mode too. In this case the D/ $\overline{U}$  input is controlled by the comparator output voltage level.

When IN+>IN-, the analog comparator output is high and the U1 counter is in DOWN mode. Vice versa when IN->IN+, the analog comparator output is low and U1 counter is in UP mode. The outputs of the two counters are digitally compared through a digital comparator U3. The output was kept on the A>=B pin of the digital comparator. For the sake of simplicity, the simulation was performed by considering 4-bit counters and a digital comparator. One digital oscilloscope is used to show the signals during the simulation. Channel A monitors the resistor divider output, channel B the resistor divider input, channel C the PWM output, and channel D the voltage reference at the DAC output. Besides the oscillator, a logic analyzer shows the counter outputs, the analog comparator output, and the digital PWM output.

Looking at Figure 14, the C trace (PWM output) was exchanged with the analog comparator output. The blue trace is the input voltage at the resistor divider.

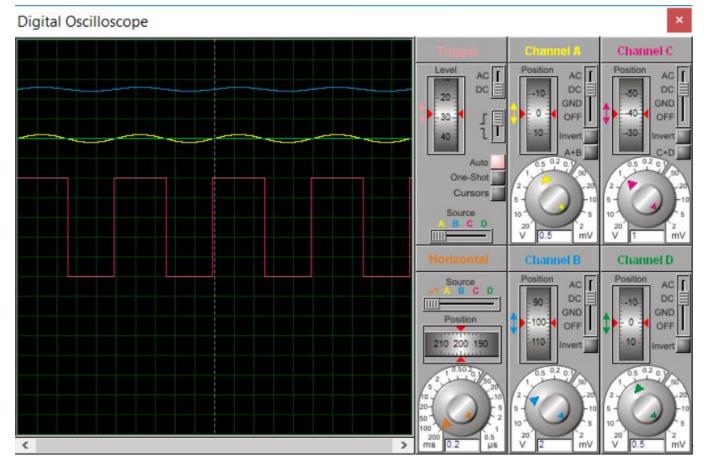


Figure 14. Analog input stage simulation



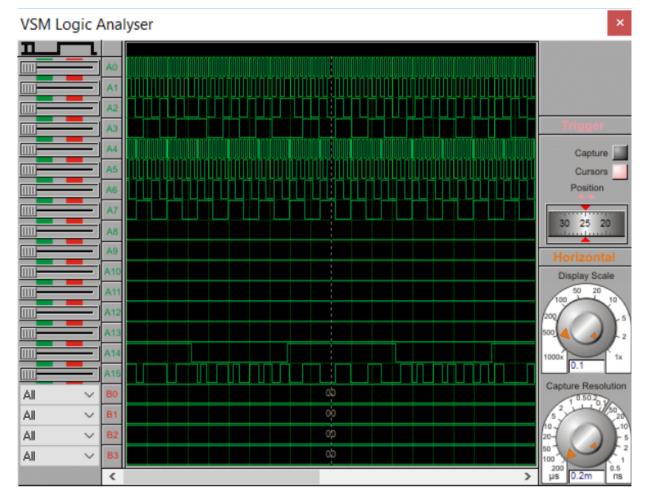


Figure 15. Logic Analyzer Signals

The green trace is the DAC reference voltage output (IN+) while the yellow one is the voltage at the middle of the voltage divider (IN-). As you can see, when the yellow trace is above the reference voltage, the comparator output goes high. The opposite is true when the yellow trace is below the green one. The comparator output is represented by the pink trace.

Figure 15 shows the digital comparator outputs (channels A0..A7), the analog comparator level (channel A14) and the PWM digital output (channel A15). The clock signal is fed at lower frequency than the real application circuit to improve the signal visibility and understanding.

What's worth to notice is that when the analog comparator is at the high voltage level, the PWM is relaxed, but more active in the opposite case. Considering the high level case, this mean that the flyback high voltage output is increasing so the PWM signal must be relaxed, leaving the flyback output settling toward the setpoint value.

The main features of this architecture are:

- A minimum PWM signal is always guaranteed.
- No synchronization is needed between the GreenPAK blocks.
- Around the setpoint value, the output tracking is digitally performed.



In the attached video you can see that as the ramp value changed, the Duty cycle changed accordingly.

## **GreenPAK Application Circuit and Testing**

Figure 16 shows the real circuit with the GreenPAK development board on the left and the flyback circuit on the right, assembled on a breadboard. The GreenPAK development board was supplied by the internal 5V regulator, while the flyback circuit was supplied by a USB 5V HUB. This choice was adopted to avoid a huge load on the internal regulator of the GreenPAK. The ground reference is the same for both. Figure 17 shows the GreenPAK programming interface.



Figure 16. Application circuit and testing

As you can see, the internal regulator is used, while the analog comparator input (TP6), the PWM signal output (TP12) and the GND signal, are routed on the Expansion Connector.

The connections were realized with rigid wire cable and with female standard headers. The TP12 pin is connected to the gate of the MOSFET, while the middle point of the resistor divider is connected to the TP6 pin. The reset/delay input TP2 was emumulated with a button in non-latched mode configuration. As you can see, the EC flag is selected on the TP6 and TP12 enabling the External connection. A digital tester is connected to the flyback output with a full scale of 1000V. We expect an output voltage approx. 450V and the multimeter measurement is shown in Fig. 18.

The circuit starts running by pressing the Testing/Emulation mode button. The reset button (TP2) is fixed to the logic high level (5V). Before you start running the flyback, **please take care that all the connections are right and don't touch any parts during the high voltage generation**. When the circuit is supplied, you can see the voltage on the digital multimeter display is increasing. The voltage increase is very fast and reaches the setpoint value of 450V in a few seconds. The value is stable around the setpoint value until you disable the Emulation mode by clicking on the Emulation button. When the GreenPAK development board is switched off, the output goes to zero in a short time.

Please refer to the video for more details.

#### Please take care and be sure that the voltage on the multimeter is null before handling the flyback circuit.

Voltages above 400V are useful for other applications as well. For example, a Geiger tube can be connected to the flyback output, and with slight modifications to the base circuits, radiation particles can be detected and counted. Furthermore, a display or a PC interface can be implemented to show parameters through a Labview GUI or a TFT display unit



This was not demonstrated here because a stable Printed Circuit Board (PCB) is required. Somewhat lower voltages (between 100V and 250V) are usually useful to drive piezo-electric devices like micropumps and MEMS devices. For that example, the output voltage can changed by setting the correct value in the DAC register input.

$$V_{DIV} = 450 \left(\frac{18k}{10M + 18k}\right) \cong 808mV$$

Finally, the DAC input register value is:

$$DAC_{REG} = \frac{808}{3.92} = 206$$



Figure 17. GreenPAK programming interface

If the DAC full scale value is at 1V, with 8 bit of resolution, we have one LSB value of:

$$LSB = \frac{1}{2^8 - 1} = \frac{1}{255} \cong 3.92mV$$

With a resistor divider (designed with  $10M\Omega$  and  $18k\Omega$ ), when the flyback output voltage is at 450V, the middle point of the resistor divider will be:

## Conclusion

The goal of this application note is to give a starting point on high voltage unit circuit design. The flyback configuration is the best choice to achieve high voltage values, and the GreenPAK technology yields the best support to develop this kind of application. The added value here is the GreenPAK technology that simplifies project development in analog and mixed signal design.

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## A High Voltage DC-DC Converter



Figure 18. Flyback Output Voltage

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