Introduction
Most RL78 MCUs have a 16-bit TAU timer that can be used to implement a PWM output, where that digital output can be RC-filtered to create a DAC-like DC output voltage proportional to the PWM duty cycle. This app note describes a method to utilize the TAU timer in 8-bit PWM mode and use PWM dithering (modulation) method to implement a 12-bit effective DAC function.

Target Device
RL78/G14 MCUs having 16-bit TAU timer and fSUB = 32768HZ oscillator. Note: RL78, S3 core MCUs having 16-bit TAU timer, 10bit ADC, and DTC (Data Transfer Control), such as RL78/G11, G1F, G1H, I1D, I1E, L1C, F13, F14, and F15 may also be used, but should be tested thoroughly to assure compatibility.

Contents
1. Overview ................................................................................................................................... 3
2. PWM Dithering method .......................................................................................................... 3
  2.1 8-bit Dithering over 16 PWM output cycles ........................................................................ 3
  2.2 PWM dithering control options: ........................................................................................... 5
3. RL78 MCU resources used ..................................................................................................... 5
  3.1 MCU Hardware ....................................................................................................................... 5
  3.2 MCU CPU processing ............................................................................................................ 6
4. Software Environment ........................................................................................................... 6
5. PWM Dithering (High-level Flowchart and Interrupt processing) ................................ 7
6. PWM dithering method details ............................................................................................ 8
  6.1 PWM Dither Adder Sequence table .................................................................................... 8
  6.2 DTC PWM Dithering adder example ............................................................................... 8
  6.3 Tradeoffs for PWM dither update rate versus CPU overhead ....................................... 9
  6.4 Measuring PWM dithering ripple at RC low-pass filter output ....................................... 9
  6.5 Typical PWM dithering ripple amplitude from RC low filter ......................................... 10
  6.6 Understanding PWM DC offset errors due to VOL and VOH offsets ............................ 10
7. Limitation of Dynamic range using PWM Dithering method ........................................... 12
8. Typical monitoring results of PWM dithering Output ..................................................... 12
  8.1 UART output for RC filtered PWM dithering, open-loop mode .................................... 12
  8.2 UART output for RC filtered PWM dithering, closed-loop mode .................................. 12
  8.3 UART output for measuring PWM output offset errors ............................................... 13
9. PWM Dithering increase/decrease, closed-loop algorithm .............................................. 14
9.1 PWM Dithering Increase

9.2 PWM Dithering Decrease

10. HW implementation for Sample SW project

11. Documents for Reference
1. Overview

Most RL78 MCUs have a 16-bit TAU timer that can be used to generate a PWM output with variable duty cycle by using a TAU master channel and slave channel. That PWM output can be filtered by a simple RC low pass filter to create a DC level proportional to the duty cycle percentage. The key is to reduce the ripple of the filtered PWM target DC voltage, so the ripple amplitude is less than 1lsb at the desired effective bit resolution. Even though the 16-bit timer can create constant, repetitive PWM waveforms directly, with up to 16-bit resolution, the PWM period for 12-bit to 16-bit PWM resolution can be quite long, requiring an inordinately long RC filter time taking one second or longer to settle. However, an 8-bit resolution PWM with 256 possible duty cycle/factor values provides a short PWM period that can be RC filtered to a proportional DC value much more quickly. Then to achieve higher equivalent bit resolution, a PWM duty cycle dithering method can be utilized, similar to PWM dithering implemented on the 16bit KB timer hardware found in RL78/I1A, L1C and L13 series MCUs.

For example, in LED lighting or analog control systems that need a logarithmic type transfer function, a total of 256 linear levels may not be adequate, since the control needs to have finer resolution steps at lower drive levels. By modulating or dithering the PWM output between 2 consecutive 8-bit code duty cycles and smoothing the output by RC low-pass filter, a variable duty cycle can achieve more than 256 DC output levels from an 8-bit PWM timer output.

This application note provides a framework to implement the PWM dithering method to increase the resolution of effective filtered PWM output DC levels. It is up to the user to perform a full evaluation to measure DC accuracy, and response time versus PWM dithering update frequency and RC low-pass filter characteristics. The DC output accuracy and performance also depends on the user’s Hardware implementation, including measures to minimize residual digital noise level in the user’s board design.

2. PWM Dithering method

The dithering method is accomplished by modulating the PWM output between 2 adjacent duty cycle percentage values in a periodic manner, automatically, by using DTC (Data Transfer Control) function. For example, the simplest PWM dithering method could be implemented by toggling between a PWM duty cycle value of 128/256 (50% duty cycle) and 129/256 (~50.4% duty cycle), alternating between these 2 duty cycles continuously. This waveform would look almost like a square wave (with a peak-to-peak value of VDD-VSS voltages) alternating between 50% and 50.4% duty cycle. If this (almost 50%/50%) square wave is filtered by a sufficiently designed low pass filter, an equivalent DC value of 128.5 out of full-scale 255 amplitude levels above 0Volts could be obtained, emulating approximately 9 bits of resolution. The low pass filter is used to reduce the dithering pattern ripple to less than 1 LSB at the new effective 9-bit resolution. Note: Figure 1 example shows a 5.6KΩ series resistor and 5.6uF filter capacitor for reducing ripple in a repeating 256uSEC PWM dither pattern, but values could be modified as required if using different PWM dithering timing.

![Figure 1: Low Pass RC filtering of dither PWM Output](image)

2.1 8-bit Dithering over 16 PWM output cycles

By modulating or dithering the PWM duty cycle values over a longer repeat period, with different dither patterns, more equivalent DC resolution bits can be obtained. This App note shows a method to create 4 additional bits of resolution, by outputting PWM output patterns that repeat every 16 PWM cycles. With the 16 cycle pattern smoothed out by an RC low pass filter, it is capable of producing one of 15 intermediate DC voltage values between two adjacent 8-bit PWM filtered DC values. Thus, the effective DC output resolution can be almost 12 bits, with some limitations (described later).
In Figure 1 above, the RC filter of R = 5.6KΩ and C = 5.6uF (RC time constant = 31.4mSEC) was chosen to reduce the ripple amplitude of a PWM carrier with 16uSEC duration to about ½ lsb at 12-bit effective resolution. A larger series and smaller shunt C could also be used to implement the RC time constant of 31.4mSEC, although DC accuracy could be affected more by test instrument loading. Generally, the RC low-pass Filter time constant should be about 2048 x PWM period to achieve ½ lsb at 12-bit effective DC resolution.

(a) Example 1: PWM output dithered between codes 0x80 and 0x81 (dither pattern for 0x80 + 7/16)

(b) Example 2: PWM output dithered between codes 0xA7 and 0xA8 (dither pattern for 0xA7 + 10/16)

The Data Transfer Control (DTC) function is used to automatically update the changing PWM duty cycle for 16 states of Dithering pattern, without CPU intervention needed until the last of 16 cycles, when the DTC is re-set for next 16-state operation. The RC filter with 31.4mSEC Time constant shown in Figure 1 is used to implement the PWM dithering Application Note Software project. With a PWM duty factor update cycle time of 16uSEC, and the dither pattern repeating every 256uSEC, a single stage RC filter with time constant of 31.4mSEC can reduce the ripple to less than 1 lsb amplitude at the new, higher effective resolution, targeted at 12 bits. The target low-pass filter RC time constant is estimated by RC = 2048 x 16uSEC = 32.768mSEC.

As shown in the Figure 1 block diagram, the ADC input can be used to monitor the filtered PWM dithering, and apply a correction (closed-loop method) for better DC output accuracy, within the absolute accuracy of the ADC conversion measurements.
2.2 PWM dithering control options:

(a) Using open-loop PWM dithering WITHOUT ADC monitoring:

This method will create monotonic DC steps, with almost 12-bit resolution (limitations discussed later). However, the filtered 8-bit PWM duty cycle to DC accuracy will be affected by voltage offsets due to port pin VOL voltage when the PWM output is at low state and by VOH voltage when the PWM output is at high state. In other words, PWM peak-peak output swing will most likely not be between VDD and VSS, where the full-scale analog references are usually AVREFP=VDD, and AVREFM=VSS. The open-loop method may be more useful when an absolute DC voltage level is not required, but DC level feedback is done by a human interacting with pot adjustment or up-down pushbutton control.

**Tradeoffs**: Using the open-loop PWM dither mode will settle to the target DC value more quickly but will have larger absolute offset error compared to using the closed method with ADC monitoring and feedback.

(b) Using closed-loop PWM dithering WITH ADC monitoring and feedback:

The RL78 10-bit ADC maximum overall error is +/-3.5 LSB (when using AVREFP and AVREFM full-scale analog voltage reference). By calibrating the individual RL78 MCU ADCs on each board in the factory, even better accuracy might be obtained for the ADC conversion results, and therefore to the filtered PWM dithered DC output. By summing and averaging 16 consecutive 10-bit ADC conversions, it is possible to measure the target 12 bits effective resolution of the filtered PWM dithering DC output.

Due to system digital noise it’s inevitable that each averaged/scaled sum of 16 consecutive 10-bit ADC conversion of filtered PWM dithered values will still vary by 1-2 LSB (or possibly more) out of 12-bit effective value. So there will be some random amplitude jitter on the corrected PWM dithered 12-bit effective resolution when using ADC averaged measurements and feedback. The app note Software project takes 256 ADC samples (1638.4HZ sample rate) and updates the Dither factor by +1, or -1 (for correction) or zero (if no offset is detected), every 256 ADC samples which is at a 6.4HZ (156.25mSEC) update rate. This simple correction method is often referred to as “bang-bang” feedback.

**Tradeoffs**: the closed-loop PWM Dithering method provides better DC accuracy, but takes longer (typically 500-600mSEC or more) to settle to a new target 12-bit effective DC value.

3. RL78 MCU resources used

3.1 MCU Hardware

(1) 16bit TAU timer Channels 0 and 1. Ch0 is used to create PWM carrier frequency and constant 16uSEC DTC update rate to PWM duty cycle value, and Ch1 for generating 8bit variable duty cycle PWM output.

(2) DTC (Data Transfer Control) operation to automatically load sequential 16 state dither pattern into the PWM duty cycle register setting. Takes about 8 CPU/System clock cycles per DTC transfer, with no CPU operation needed.

(3) 10bit ADC conversions at 1638.4HZ rate (every 610.4 uSEC), using fSUB = 32768HZ clock with ADC Hardware Trigger Wait mode from 12-bit Interval Timer.

(4) Optional UART1 output to transmit live 12-bit averages of filtered PWM dithering DC value.
3.2 MCU CPU processing

Since the PWM output is being dithered, some CPU processing overhead is required:

1. DTC updates every 16uSEC; DTC uses 8 CPU cycles out of every 512 cycles when using 32MHZ CPU clock rate. The update rate could be adjusted for faster or slower updates if desired, as long as the RC low-pass filter time constant is adjusted accordingly.

2. DTC state reload interrupts, r_tau0_channel0_interrupt(), every 16 DTC cycles, at 256uSEC rate.

3. 10-bit ADC conversion completion interrupt processing every 610.4 uSEC (1638.4HZ rate). 10-bit ADC conversions occur at 1638.4HZ rate using fSUB = 32768HZ clock in ADC Hardware trigger wait mode. However, the ADC HW triggered conversions themselves can operate in parallel with Software operation. ADC conversions are an optional method to monitor RC low-pass filter output from PWM dithering pattern, and correct the DC value by modifying the dither patter.

4. Processing sum of 16 consecutive ADC conversion every 9.677mSEC (102.4HZ rate)

5. Optional UART1 interrupts, processing at 86.81uSEC per ASCII Character at 115.2Kbaud. This facilitates real-time monitoring of 16 consecutive averaged 10-bit ADC conversions of filter PWM dithered output, in a testing mode.

4. Software Environment

<table>
<thead>
<tr>
<th>IDE</th>
<th>RL78 Compiler</th>
<th>Compiler Versions</th>
</tr>
</thead>
<tbody>
<tr>
<td>Renesas e2studio v5.4.0.018</td>
<td>CC-RL</td>
<td>v1.05</td>
</tr>
</tbody>
</table>

Table 1: Sample Software project environment
5. PWM Dithering (High-level Flowchart and Interrupt processing)

Start:
- Power-ON, MCU RESET Boot Start (@ 0x00000)
- Initialize MCU, RAM, Clock Generator & Peripheral Functions (Ports, UART, 10-bit ADC, TA0 PWM, 12bit Interval Timer, DTC)
- Set up TA0 Ch0/Ch1 for 8-bit PWM Output Duty cycle start value
- Set up DTC target 16Word Dithering Table
- Start 16bit TAU0 timer Ch0 constant 16USEC interrupt
- Start continuous ADC conversions by Interval Timer trigger

Main Application

- 16 ADC Readings (ADC_Convert16_flag = 12?)
- Yes
- Clear ADC_Convert16_flag
- Store consecutive sums of 16 ADC Conversions each
- Have 16 ADC sums (total of 256 ADC samples) been stored?
- Calc. sum of 256 ADC conversion values (18bit result) scaled down to 12bit value
- Compare measured average of 256 ADC (scaled to 12bit) Result to current Dither PWM target value (12-bit) \[\text{result} = \text{Target PWM12_value - adc_256sum_avg}\]
- Result Avg. < Target DC Value (Dither Increase)
- Change DTC PWM 16Word Table to next higher values, Call Function pwm_dithering_increase()
- Result Avg. > Target DC Value (Dither Decrease)
- Change DTC PWM 16Word Table to next lower values, Call Function pwm_dithering_decrease()

Result comparison?

Dithering
PWM
“Bang-bang” Control Loop

---

**r_cg_adc_user.c:**

- r_adc_interrupt()
  - 10-bit ADC completion interrupt
  - Add current ADC value to 16bit sum
  - Increment ADC conversion count
  - Count > 15?
  - Yes: Set ADC_Convert16_flag
  - No: RTI

**r_cg_timer_user.c:**

- r_tau0_channel0_interrupt()
  - Constant 256USEC Interrupt, end of 16 DTC transfers (TA0 Ch0 Interval Timer ISR)

**r_cg_serial_user.c:**

- r_uart1_interrupt_send()
  - UART1 Send Interrupt
  - Load next char until done
  - RTI

---

**DTC hardware processing:**

- 16bit TA0 Ch0 timer Interval Interrupt Trigger
- DTC transfer of next PWM dithering word (N = 0 to 15)
- Resume program flow

- Constant 16USEC Interrupt for DTC trigger (no ISR)

---

Constant ADC interrupts @1638.4HZ (610.4uSEC) HW trigger with Wait mode

86.81uSEC per ASCII Character at 115.2Kbaud.
6. PWM dithering method details

6.1 PWM Dither Adder Sequence table

This PWM dither adder sequence table was designed to distribute the zeroes and ones pattern for highest repetition frequency, although PWM dither pattern is not so critical, since frequency components are similar for adjacent duty cycles (for example 128/256, and 129/256 duty cycles have almost the same harmonic content values). A zero means the base PWM duty cycle value is used and a one means the base PWM duty cycle + 1 value is used. The Dither factor is the total duty cycle of N/16, where N = 0 to 15.

<table>
<thead>
<tr>
<th>DTC State</th>
<th>Dither sequence (Dither factor)</th>
</tr>
</thead>
<tbody>
<tr>
<td>0</td>
<td>0 1 1 1 1 1 1 1 1 0 0 0 0 0 0 0</td>
</tr>
<tr>
<td>1</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1</td>
</tr>
<tr>
<td>2</td>
<td>0 0 0 0 0 0 0 0 1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>3</td>
<td>0 0 0 0 0 0 1 1 1 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>4</td>
<td>0 0 0 0 0 1 0 0 0 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>5</td>
<td>0 0 0 0 1 0 0 1 1 0 1 1 0 1 1 1</td>
</tr>
<tr>
<td>6</td>
<td>0 0 0 1 0 0 1 0 0 1 1 0 1 1 0 1</td>
</tr>
<tr>
<td>7</td>
<td>0 0 0 1 0 1 0 1 1 0 1 0 1 1 0 1</td>
</tr>
<tr>
<td>8</td>
<td>0 0 0 1 1 0 1 1 1 0 1 0 1 1 1 1</td>
</tr>
<tr>
<td>9</td>
<td>0 0 1 0 1 0 1 1 1 0 1 1 0 1 1 1</td>
</tr>
<tr>
<td>10</td>
<td>0 0 0 0 0 1 0 1 0 0 1 0 1 1 1 1</td>
</tr>
<tr>
<td>11</td>
<td>0 0 0 0 1 0 1 0 1 1 0 1 1 0 1 1</td>
</tr>
<tr>
<td>12</td>
<td>0 0 0 0 0 0 0 0 1 0 0 1 1 1 1 1</td>
</tr>
<tr>
<td>13</td>
<td>0 0 0 0 1 1 0 1 1 0 0 1 1 1 1 1</td>
</tr>
<tr>
<td>14</td>
<td>0 0 0 0 0 0 0 0 1 1 0 0 1 1 1 1</td>
</tr>
<tr>
<td>15</td>
<td>0 0 0 0 0 0 0 0 0 1 1 1 1 1 1 1</td>
</tr>
<tr>
<td>16</td>
<td>0 0 0 0 0 0 0 0 0 0 0 0 0 0 0 1</td>
</tr>
</tbody>
</table>

Table 2: Dithering adder sequence table

Each vertical set of 16 adder values is for creating a new DTC sequence by adding to the base PWM value.

Examples:
- DTC Adder Sequence 0 has all zeroes (no dithering)
- DTC Adder Sequence 7 has 9 zeroes and 7 ones (7/16 dithering)
- DTC Adder Sequence 15 has one zero and 15 ones (15/16 dithering)

6.2 DTC PWM Dithering adder example

Example to create new DTC Dithering values:
If base PWM value is 0x0080, and adder is for 7/16 dithering, use DTC Adder Table 7
6.3 Tradeoffs for PWM dither update rate versus CPU overhead

When implementing the PWM dithering method shown in this app note, it may be desirable to change the dithering rate, which may also require modifying the low-pass filter RC time constant. The tradeoff is that a slow dithering update rate, and longer RC filter time constant, will have a longer response time when changing the target PWM dithered 12-bit effective resolution value, especially when the target DC output value delta change is large. For example, changing from 10% to 90% of the analog full scale reference will take a settling time that is proportional to the RC low pass filter time constant (approximately 2.5 to 3 RC time constants for 10% to 90% slew rate). However, a faster PWM dither rate will require more CPU/System clock cycles for DTC operation and higher CPU processing overhead. Therefore, the user will need to determine a balance between adequate DC Slew rate performance versus System/CPU processing overhead. The sample software project uses 16uSEC DTC update rates based on a 16MHZ TAU timer clock rate, so at 32MHZ system clock the DTC operation uses 8clocks out of every 512 System clocks.

6.4 Measuring PWM dithering ripple at RC low-pass filter output

The app note software project implements a 16uSEC PWM dither update rate that repeats every 16 periods (256uSEC total period) to create close to 12-bit effective resolution. The RC low pass filter should be designed to limit ripple to less than 1LSB at 12-bit effective resolution. This app note sample project uses 5.6K series resistor and 5.6uF capacitor for a 31.4mSEC RC time constant. Using the 31.4mSEC RC time constant achieves about 0.5-0.6 LSB typical ripple amplitude (relative to 12-bit effective resolution) when the duty cycle is 50%, which is worst case.

It is difficult to measure the dithering ripple amplitude after RC filtering for these reasons:

1. The ripple amplitude for 12-bit effective resolution from RC filtered PWM is typically less than 0.75mV-1.25mV (or lower) depending on VDD value. In Table 2 example below, VDD values of 3.072 Volts and 5.12 Volts (similar to typical 3Volt and 5Volt power supplies) are shown to make the steps easy to represent. At these 0.75-1.25millivolts levels (or less) the System/MCU noise levels may be as high the PWM dithering ripple value.

<table>
<thead>
<tr>
<th>Using RL78:</th>
<th>Resolution</th>
<th>Each LSB step, when AVREFP = VDD =</th>
</tr>
</thead>
<tbody>
<tr>
<td>ADC</td>
<td>10-bit</td>
<td>3.072 Volts</td>
</tr>
<tr>
<td>RC-filtered PWM Dithering</td>
<td>12-bit (effective)</td>
<td>0.75mV</td>
</tr>
</tbody>
</table>

Table 4: ADC/PWM Dithering resolutions
Although an RC filter series resistance of 5.6kΩ was used for app note sample project, almost any instrument loading on the RC filter will still affect the 12-bit effective DC level accuracy somewhat, especially when loaded with a 1MΩ probe. In open-loop mode, the DC value will drop by about 23 LSB (12-bit resolution) if loaded by 1MΩ impedance. In closed-loop mode the PWM dither algorithm will try to compensate and bring the RC-filtered output back to the target 12-bit effective DC value. The compensation will work for most of the 12-bit DC voltage target range unless the unloaded target DC value was at the upper PWM duty cycle range, and no more compensation “head-room” is left.

<table>
<thead>
<tr>
<th>Scope/meter Probe Loading on RC filter output (5.6Kohm series resistor)</th>
<th>Lowered DC amplitude due to Probe loading</th>
<th>Loading Error, One part in:</th>
<th>Equivalent LSB error @12bit resolution:</th>
</tr>
</thead>
<tbody>
<tr>
<td>1 Megohm</td>
<td>0.99443</td>
<td>179.6</td>
<td>22.8</td>
</tr>
<tr>
<td>10 Megohm</td>
<td>0.99944</td>
<td>1788</td>
<td>2.3</td>
</tr>
</tbody>
</table>

**Figure 3: Measurement errors due to instrument loading**

### 6.5 Typical PWM dithering ripple amplitude from RC low filter

For a variable duty cycle PWM waveform filtered by RC filter, the maximum ripple is at 50% duty cycle (duty factor). If the maximum ripple at 50% duty factor is normalized to 1.0, the relative RC-filter PWM ripple is shown by equation:

\[
\text{RC-Filtered PWM ripple} = 4^*(DF - (DF)^2);
\]

where \(DF= \text{Duty Factor} = N/256 \text{ for } N = 0 \text{ to } 256\)

**Figure 4. Relative PWM ripple amplitude after simple Low Pass RC Filtering**

The RC-filtered PWM ripple amplitude is symmetrical around 50% duty cycle. For example the filtered ripple amplitude for duty factor = 64/256 is the same as for duty factor 192/256, just inverted. As the Duty factor approaches 0% and 100%, the PWM output harmonic content increases and is more highly attenuated by the RC filter. Since dithering is performed by alternating between 2 adjacent PWM duty cycles (for example, 128/256 versus 129/256 duty cycle), there is almost no difference in ripple amplitude between different dither factors using the same base PWM duty cycle value.

### 6.6 Understanding PWM DC offset errors due to VOL and VOH offsets

When the PWM dithering is in open-loop mode the main DC errors are from DC offsets in the port pin P16/TO01 output due to VOL (when PWM output is at low state) and VOH (when PWM output is at high state). Most often the P-channel transistor driving the port pin high is weaker than the N-channel transistor, so that the VDD-VOH difference offset is typically larger than the VOL-VSS difference offset. That means the range of RC filtered DC value over PWM values of duty cycle of 0x00 to 0xFF will be less than VDD-VSS (AVREFP-AVREFM) full scale analog voltage reference. It could also mean in some PWM value cases there can also be a lowered skew of DC value. For example, if
VDD – VOH = 50mV and VOL – VSS = 20mV, then a 50% PWM duty cycle will generate a DC value that is about 37.5mV lower than (VDD-VSS)/2, the DC value halfway between VDD-VSS (AVREFP-AVREFM) full scale analog voltage. Typically, the DC offset error won’t be this large though.

In Figure 7, the PWM pin VOL vs IOL and VOH vs IOH curves can be used to evaluate typical PWM DC offsets. **Note:** these curves are typical, not guaranteed specifications.
For PWM Dithering in closed loop mode, the feedback loop will attempt to compensate for DC offset errors if possible. However, due to DC offset issues at low and high PWM values, it is recommend to operate the PWM dithering in a narrower range than full 100% of 0x000 to 0xFF0 dithered, 12-bit effective DC values. For example, a 5%-95% range or 10%-90% operation range is more likely to achieve accurate results.

7. Limitation of Dynamic range using PWM Dithering method

There are 256 possible output values of the 8-bit PWM, but the dithering requires toggling between 2 adjacent PWM output values. Using a 16 state dithering sequence there are only 15 different dithering sequences between any 2 PWM output states. As can be seen, the Dither adder sequence 0 (in Table 2.) is all zeroes which means no dithering is done. Otherwise, dithering can only be applied on 255 combinations of 2 adjacent PWM codes, so there are only 4081 possible values:

\[
\text{Maximum range of Dithered \text{“12-bit” output values}} = \\
256 (\text{PWM codes 0x00 to 0xFF, no dithering}) + 255 \times 15 \text{ dithering sequences} \\
= 4081 \text{ values,} \\
0-4080 \text{ decimal (0x000 to 0xFF0)}
\]

So when using the PWM Dithering method, the effective 12-bit resolution target setting the max value is limited to the 12-bit code of 0xFF0, which is the same maximum of the 8-bit PWM output codes. Note: Although the PWM dithering output setting is limited to a max target value of 0xFF0, it is possible that ADC conversion values of 0xFF1 to 0xFFF may still occur, due to DC offsets/errors from ADC conversions.

It would be possible to dither between a duty cycle of 255/256 and constant output state = 1, but the app note SW project limits the max PWM duty cycle to 255/256 (0x00FF), to avoid any PWM timer start/stop issues.

8. Typical monitoring results of PWM dithering Output

The app note Software Project includes an optional UART1 output (provided on RSKRL78G14 board DB-9 connector) to provide real-time monitoring of the PWM dithering output, both before and after RC filtering. UART1 is set for 115.2Kbps, and each 10bit character takes about 86.8uSEC. Each hex value of 3 ASCII characters (plus comma or LF character) in section 8.1 and 8.2 is output at 102.4HZ (9.77mSEC) rate and takes about 347uSEC for 4characters. The UART1 print function was intended for troubleshooting and accuracy measurement, but is not needed to implement the PWM dithering open-loop or closed-loop functions.

8.1 UART output for RC filtered PWM dithering, open-loop mode

When variables enable_print = 1 and g_closed_loop = 0 in r_main.c, UART1 will output the sum of 16 consecutive ADC conversion, scaled down to a 12bit Hex value, with no correction on the PWM dithering. The first (single) hex value is the target 12-bit effective dithered PWM DC value. Each line thereafter represents 16 averaged/scaled RC filtered output values (each value is sum of 16 ADC 10-bit conversions). So each line occurs at 64HZ rate (16384HZ sample rate/256 total samples). In this example output, target_pwm12_value = 0xD1B. After about 16mSEC startup time, the dithered PWM RC filtered output settles to 0xD19, which is an offset of about -2 steps below the target 0xD1B value in 12bit effective PWM resolution.

<table>
<thead>
<tr>
<th>D1B</th>
</tr>
</thead>
<tbody>
<tr>
<td>0xD1F, 0xD1F, 0xF75, 0xF75, 0xF75, 0xF75, 0xF75, 0xF74, 0xF74, 0xF74, 0xF74, 0xF74, 0xF74, 0xF74, 0xF74, 0xF74, 0xF74</td>
</tr>
<tr>
<td>0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19</td>
</tr>
<tr>
<td>0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19, 0xD19</td>
</tr>
</tbody>
</table>

(…continues indefinitely)

Figure 8.: UART1 print monitoring in Open-loop mode

8.2 UART output for RC filtered PWM dithering, closed-loop mode

When variables enable_print = 1 and g_closed_loop = 1 in r_main.c, UART1 will output the sum of 16 consecutive ADC conversion, scaled down to a 12bit Hex value, with the PWM Dithering value corrected once on each line (156.25mSEC correction rate). The data output is the same format as described in section 8.1 above. In this example, again the target_pwm12_value = 0xD1B. However due to the closed-loop ADC measurement and correction, the
dithered PWM RC filtered output settles to the target 0xD1B value in 12-bit effective resolution but takes about 3-4 periods of 156.25mSEC correction to achieve stable output. However, due to system noise, the ADC occasionally sees averaged 12-bit DC values at 0xD1A and 0xD1C, even if no dithering correction is applied.

8.3 UART output for measuring PWM output offset errors

When `g_pwmout_test_flag = 1` in `r_main.c`, and function `pwmout_test_to_adc_input()` is run, the 10bit ADC measures each of 8-bit PWM codes 0x00 to 0xFF, without dithering, for 256 consecutive ADC conversions per PWM output code at the RC filter output (ANI10). Each line evaluates a single 8-bit PWM output code, starting with 0x00 and ending with 0xFF. Each 4 character value corresponds to the sum of 16 consecutive 10-bit ADC conversions, so each value can contain up to 14bit results, not scaled down. Possible output range is 0x0000 to 0x3FFC max (0 to 16380 decimal).

From this example below, it is seen the 8-bit PWM code of 0xFF, when measured 256 times has a 14bit average value of 0x3FBB, or about 1019.68 decimal (or 0x3FC) at 10-bit resolution. This Figure 10. Data is representative but will vary from one RL78/G14 MCU device to another.

```
003C,0040,0040,0048,0048,004E,004F,0050,004E,004F,004E,0050,004E,004F,0050,004E
0071,007B,0080,0080,0080,0080,0081,0081,0086,0084,0086,0089,0089,0087,0089
00B4,00C0,00C0,00C1,00C1,00C0,00C0,00C4,00C9,00CB,00CB,00CA,00CB,00CA,00C7
3EF0,3EF2,3EFC,3EF3,3EF7,3EF7,3EF9,3EF9,3EF9,3EFB,3EF7,3EFC,3EF9,3EFB,3EF7,3EFE
3F37,3F32,3F3B,3F38,3F3A,3F3A,3F3F,3F3C,3F3B,3F3A,3F3F,3F3C,3F3B,3F3A,3F3F,3F3D
3F6F,3F71,3F72,3F72,3F7B,3F78,3F7F,3F7C,3F7F,3F7D,3F7A,3F7F,3F7A,3F7B,3F79,3F7D
3FB4,3FBB,3FBB,3FBB,3FB9,3FBC,3FBB,3FBB,3FBF,3FBB,3FBB,3FB8,3FBB,3FBD,3FC2,3FC0
(completes after 256 total lines)
```

By taking the above data from `pwmout_test_to_adc_input()` UART1 data output averaging and scaling down to 10-bit results equivalent resolution, the average RC-filtered PWM DC output error can be visualized. The errors tend to be larger toward the middle ranges of PWM duty cycle. This is probably because the RC filter charge and discharge currents are larger in the middle ranges (50%/50%) of PWM, and therefore has larger VOH and VOL offsets.

**Note:** Data in Figure 11 is typical, not guaranteed.
9. PWM Dithering increase/decrease, closed-loop algorithm

In the PWM Dithering close-loop mode, the sum of the last 256 ADC conversions (10bits x 256 = 18bit result) is scaled down and rounded off to a 12bit effective result every 156.25mSEC. Then the 12bit actual (averaged) result is compared to the User settable 12-bit target_pwm12_value. If target and measured values are equal, then no PWM dithering correction is made. If the actual measured value is less than the target value, the dithering factor is increased by one bit value in 12-bit resolution. If the actual measured value is greater than the target value, the dithering factor is decreased by one bit value (12-bit resolution). Care is taken not to produce a Dithering base value and factor that is out of range.

Depending on the previous PWM output Base Value, either the Base Value, the Dithering factor, or both values will need to be updated into the 16word RAM table transferred to TAU timer channel1 (duty cycle compare register (TDR01) by DTC data transfers.

9.1 PWM Dithering Increase

For Dithering increases, a special case occurs when the previous PWM Dithering value is 0xFF0, and no increase is allowed, since Dithering can only occur between PWM output codes 0xFE and 0xFF to produce 12bit PWM effective codes of 0xFE0 to 0xFEF. A constant PWM output code of 0xFF represents 0xFF0 in 12-bit resolution and no further increase is allowed. Of course, there could be some DC offset due to VOH output level being lower than VDD = AVREFP, when PWM output is 0xFF code, resulting in the 12bit effective DC value slightly less than 0xFF0.

9.2 PWM Dithering Decrease

For Dithering decreases, a special case occurs when the previous PWM Dithering value is 0x000, and no decrease is possible, since Dithering can only occur between PWM output codes 0x00 and 0x01 to produce 12bit PWM effective codes of 0x000 to 0x00F. A constant PWM output code of 0x00 represents 0x000 in 12-bit resolution and no further decrease is possible.

10. HW implementation for Sample SW project

The PWM dithering application note Sample SW project was developed on an RSKRL78G14 board, populated with 100pin RL78/G14 (device R5F104PJ). This board layout was designed to maximize access to all the MCU pins, and provide a preliminary prototyping platform for customer RL78/G14 designs. However, the printed circuit board layout may not be optimum for lowest Analog noise riding on the RL78 power supply and ground lines. RSKRL78G14 board wiring for the Sample SW project is shown in Figure 12 and Figure 13.

In a customer-designed board, care should be taken to minimize ground loops and power supply line impedance to the Analog voltage reference pins. For the RSKRL78G14 board, connector J4 is the shortest, most convenient place to wire up the ADC lines and analog reference pins on RL78/G14 MCU ports P2 and P15. ADC analog reference pins AVREFP and AVREFM are connected to VDD and VSS/Ground respectively, by connecting to connector J12.
In wiring diagram Figure 13, ANI10 ADC input is used for checking/correcting the PWM dithering Low-pass filtered output value.

**Figure 13: Recommended wiring for PWM dithering Sample SW project using RSKRL78G14 board**

### 11. Documents for Reference

**User’s Manual:**
RL78/G14 User’s Manual: Hardware Rev.3.30 (R01UH0200EJ0330)
RL78 Family User’s Manual: Software Rev.2.00 (R01US0015EJ0200)
RL78 Family DAC Dithering Rev. 1.00 (R01AN3795EJ100)

(The latest versions of the documents are available on the Renesas Electronics Website.)

**Technical Updates/Technical Brochures**
(The latest versions of the documents are available on the Renesas Electronics Website.)
Website and Support

Renesas Electronics Website

http://www.renesas.com/

Inquiries

http://www.renesas.com/contact/

All trademarks and registered trademarks are the property of their respective owners.
# Revision History

<table>
<thead>
<tr>
<th>Rev.</th>
<th>Date</th>
<th>Page</th>
<th>Summary</th>
</tr>
</thead>
<tbody>
<tr>
<td>1.00</td>
<td>16Jun2017</td>
<td></td>
<td>First edition</td>
</tr>
</tbody>
</table>
General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Handling of Unused Pins
   Handle unused pins in accordance with the directions given under Handling of Unused Pins in the manual.
   - The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible. Unused pins should be handled as described under Handling of Unused Pins in the manual.

2. Processing at Power-on
   The state of the product is undefined at the moment when power is supplied.
   - The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the moment when power is supplied.
   In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the moment when power is supplied until the reset process is completed.
   In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the moment when power is supplied until the power reaches the level at which resetting has been specified.

3. Prohibition of Access to Reserved Addresses
   Access to reserved addresses is prohibited.
   - The reserved addresses are provided for the possible future expansion of functions. Do not access these addresses; the correct operation of LSI is not guaranteed if they are accessed.

4. Clock Signals
   After applying a reset, only release the reset line after the operating clock signal has become stable. When switching the clock signal during program execution, wait until the target clock signal has stabilized.
   - When the clock signal is generated with an external resonator (or from an external oscillator) during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Moreover, when switching to a clock signal produced with an external resonator (or by an external oscillator) while program execution is in progress, wait until the target clock signal is stable.

5. Differences between Products
   Before changing from one product to another, i.e. to a product with a different part number, confirm that the change will not lead to problems.
   - The characteristics of Microprocessing unit or Microcontroller unit products in the same group but having a different part number may differ in terms of the internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.
Notice

1. Descriptions of circuits, software and other related information in this document are provided only to illustrate the operation of semiconductor products and application examples. You are fully responsible for the incorporation or any other use of the circuits, software, and information in the design of your product or system. Renesas Electronics disclaims any and all liability for any losses and damages incurred by you or third parties arising from the use of these circuits, software, or information.

2. Renesas Electronics hereby expressly disclaims any warranties against and liability for infringement or any other disputes involving patents, copyrights, or other intellectual property rights of third parties, by or arising from the use of Renesas Electronics products or information described in this document, including but not limited to, the product data, drawing, chart, program, algorithm, application examples.

3. No license, express, implied or otherwise, is granted hereby under any patents, copyrights or other intellectual property rights of Renesas Electronics or others.

4. You shall not alter, modify, copy or otherwise misappropriate any Renesas Electronics product, whether in whole or in part. Renesas Electronics disclaims any and all liability for any losses or damages incurred by you or third parties arising from such alteration, modification, copy or otherwise misappropriation of Renesas Electronics products.

5. Renesas Electronics products are classified according to the following two quality grades: "Standard" and "High Quality". The intended applications for each Renesas Electronics product depends on the product's quality grade, as indicated below.

   - "Standard": Computers, office equipment, communications equipment, test and measurement equipment, audio and visual equipment, home electronic appliances, machine tools, personal electronic equipment, and industrial robots etc.
   - "High Quality": Transportation equipment (automobiles, trains, ships, etc.), traffic control (traffic lights), large-scale communication equipment, key financial terminal systems, safety control equipment, etc.

Renesas Electronics products are neither intended nor authorized for use in products or systems that may pose a direct threat to human life or bodily injury (artificial life support devices or systems, surgical implantations etc.), or may cause serious property damages (space and underwater repeaters, nuclear power control systems, aircraft control systems, key plant systems, military equipment, etc.). Renesas Electronics disclaims any and all liability for any damages or losses incurred by you or third parties arising from the use of any Renesas Electronics product for which the product is not intended by Renesas Electronics.

6. When using the Renesas Electronics products, refer to the latest product information (data sheets, user's manuals, application notes, "General Notes for Handling and Using Semiconductor Devices" in the reliability handbook, etc.), and ensure that usage conditions are within the ranges specified by Renesas Electronics with respect to maximum ratings, operating power supply voltage range, heat radiation characteristics, installation, etc. Renesas Electronics disclaims any and all liability for any malfunctions or failure or accident arising out of the use of Renesas Electronics products beyond such specified ranges.

7. Although Renesas Electronics endeavors to improve the quality and reliability of Renesas Electronics products, semiconductor products have specific characteristics such as the occurrence of failure at a certain rate and malfunctions under certain use conditions. Further, Renesas Electronics products are not subject to radiation resistance design. Please ensure to implement safety measures to guard them against the possibility of bodily injury, injury or damage caused by fire, and social damage in the event of failure or malfunction of Renesas Electronics products, such as safety design for hardware and software including but not limited to redundancy, fire control and malfunction prevention, appropriate treatment for aging degradation or any other appropriate measures by your own responsibility as warranty for your product/system. Because the evaluation of microcomputer software alone is very difficult and not practical, please evaluate the safety of the final products or systems manufactured by you.

8. Please contact a Renesas Electronics sales office for details as to environmental matters such as the environmental compatibility of each Renesas Electronics product. Please investigate applicable laws and regulations that regulate the inclusion or use of controlled substances, including but not limited to, the EU RoHS Directive carefully and sufficiently and use Renesas Electronics products in compliance with all applicable laws and regulations.

9. Renesas Electronics products and technologies shall not be used for or incorporated into any products or systems whose manufacture, use, or sale is prohibited under any applicable domestic or foreign laws or regulations. You shall not use Renesas Electronics products or technologies for any purpose relating to the development, design, manufacture, use, stockpiling, etc., of weapons of mass destruction, such as nuclear weapons, chemical weapons, or biological weapons, or missiles (including unmanned aerial vehicles (UAVs)) for delivering such weapons, (2) any purpose relating to the development, design, manufacture, or use of conventional weapons, or (3) any other purpose of disturbing international peace and security, and you shall not sell, export, lease, transfer, or release Renesas Electronics products or technologies to any third party whether directly or indirectly with knowledge or reason to know that such third party will engage in the activities described above. When exporting, selling, transferring, etc., Renesas Electronics products or technologies, you shall comply with any applicable export control laws and regulations promulgated and administered by the governments of the countries asserting jurisdiction over the parties or transactions.

10. Please acknowledge and agree that you shall bear all the losses and damages which are incurred from the misuse or violation of the terms and conditions described in this document, including this notice, and hold Renesas Electronics harmless, if such misuse or violation results from your resale or making Renesas Electronics products available any third party.

11. This document shall not be reproduced, reproduced or duplicated in any form, in whole or in part, without prior written consent of Renesas Electronics.

12. Please contact a Renesas Electronics sales office if you have any questions regarding the information contained in this document or Renesas Electronics products.

(Note 1) "Renesas Electronics" as used in this document means Renesas Electronics Corporation and also includes its majority-owned subsidiaries.

(Note 2) "Renesas Electronics products" means any product developed or manufactured by or for Renesas Electronics.

(Rev. 3.0-1 November 2016)