Low-Latency, Low-Power, Precision Analog-to-Digital Converters

Joao Marques, Senior Design Centre Manager, Industrial ASIC BU

Abstract

The ADC is a key element in any Analog Front End. In this paper we examine how choosing the right converters for each application determines how efficient those systems will be. Over-specifying converter's parameters will increase the costs and the complexity. Under-specification will reduce the performance and limit the scope of applications. Choosing the right ADC architecture is critical for an optimized solution. This paper focuses on the Low-Latency, Low-Power Precision ADCs targeting the expanding IoT market, but also other markets including automotive, medical and consumer.

Contents

Abstract **1**

Introduction **2**

Latency, Power, Precision **3**

Latency 3

Power 3

Precision 4

Dynamic Performance 4

Static Performance 5

Analog to Digital Converter Architectures **6**

Flash ADC 6

Delta Sigma ADC 7

Pipeline ADC 8

Successive Approximation Register (SAR) ADC 9

DIAS ADCs: Low-Latency, Low-Power, Precision Converters **10**

Multiplexed Input Channels 10

Input Signal Range 11

Input Common-Mode Range 11

Input Signal Type 11

Small Input Capacitance 11

Adjustable Tracking Period 11

Wide Range Sampling Rate with Scaling Power Dissipation 12

Supply Noise Immunity 12

Operating Modes 12

Digital Output Format 12

Programmable Resolution 13

Low Power and Calibration 14

Conclusions **15**

Revision History **16**

Introduction

Industry 4.0 and the Industrial Internet of Things (IIoT) is changing the industry as we know it and there is a movement towards industrial systems now becoming connected, intelligent devices.

Figure 1: Industry Revolutions

In this industrial new world, factories are operated by self-driving vehicles and robots, each one with many sensors wirelessly connected to a central system that can make decisions on its own and that can optimize the process based on continuously receiving accurate data.

In such an industrial environment, factories can increase the efficiency, lower the costs, and improve the productivity.

Industrial IoT is expected to be one of the fastest growing segments of IoT with tens of billion connected devices expected in a few years.

In these factories, there are three critical requirements:

1. Large bandwidth communication channels
2. Fast Data processing
3. Accurate decision intelligence (at the edge)

The large bandwidth communication channels are required for the broadband communication between the multiple devices (edge) and the central system, either a cloud or a server. The new 5G wireless protocol is helping enable this communication. New advancements in AI (Artificial Intelligence) and Big Data provide the tools to process the data.

The decision intelligence at the device level, also called processing at the edge or edge computing, is important in an industrial environment, when fast decisions are required, and delays related to the communication latency with the central system are not acceptable.

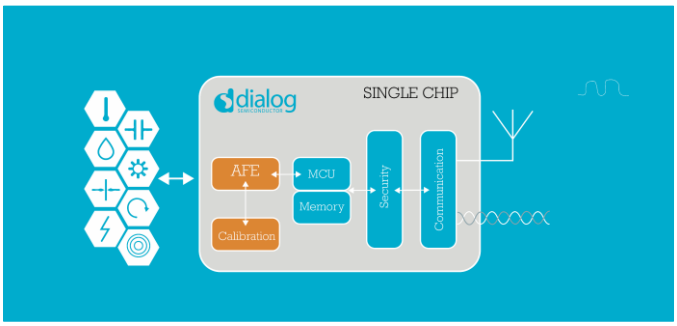


Figure 2: SmartEdge™ Platform

Our SmartEdge™ system (Fig. 2) represents such an edge device and the main components required for the edge operations. Processing at the edge optimizes system responsiveness, communication overhead and security.

A key block in any edge device is the Analog-to-Digital Converter (ADC), included in the Analog Front-End (AFE). The ADC is the block responsible to convert the analog signals acquired by the sensors to the digital world to be processed by the local processor and/or sent to the central system through a wireless or wired interface.

The main requirements for these ADCs are:

- **Low Latency**: these ADCs are often present in precision control loops, in which minimum latency is required for a fast action based on a decision resulting from the acquired data.
- **Low Power**: many industrial devices are operated by batteries or energy harvesting and low power is crucial to extend the device lifetime. Replacing batteries on nodes can be extremely costly and, in some cases, it may be very difficult or even impossible.
- **High Precision/High Accuracy**: accurate digital representation of the analog signal optimizes the system responsiveness and the overall efficiency.

Latency, Power, Precision

Latency

ADC Latency can be defined as the time difference between acquiring the analog input signal and having its representative digital word available at the output.

Latency L, is usually a multiple of clock-cycles or half clock-cycles

$$L = K*T_{CLK}/2$$

Where TCLK is the clock period and K depends on the ADC architecture (which will be reviewed in more detail later in this paper). A smaller K corresponds to a smaller latency.

A higher clock frequency $f_{CLK} = 1/T_{CLK}$ corresponds to a smaller latency. Maximum f_{CLK} also depends on the ADC architecture, as well as the technology process node and supply voltage.

Fig. 3 represents an ADC timing diagram, including its latency.

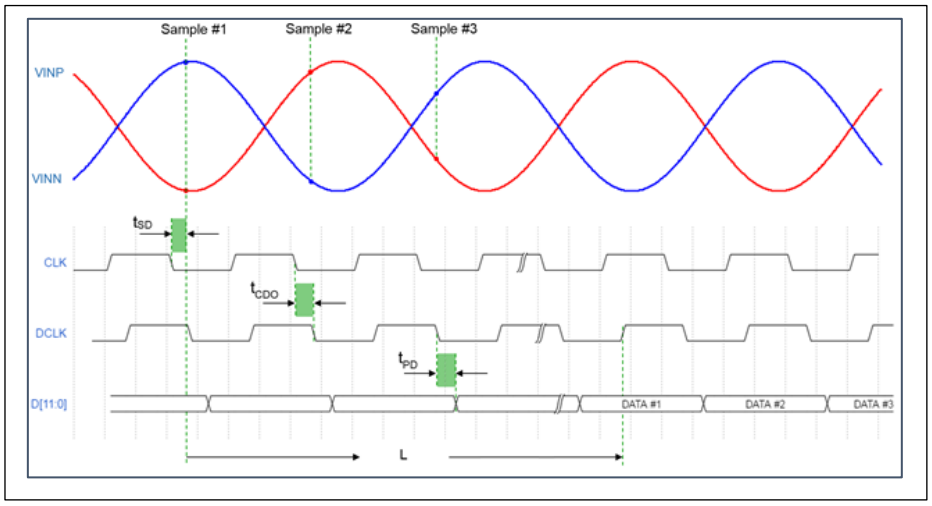


Figure 3: ADC Timing Diagram

Power

Power dissipation is among the highest concern in ADC design for mobile, battery-operated, applications.

The power dissipation measures the energy dissipated per unit of time, which indicates the lifetime of a battery-operated device. Explained by the Joule effect, the dissipated energy generates heat which will, in an IC component, limit the operating frequency, the performance and add constraints to the package selection.

The digital and analog sections of the ADCs have different power dissipation profiles.

Power dissipation on a digital CMOS gate, P_{dig}, is primarily related to the dynamic power given by:

$$P_{dig} = f_{SW} \times VDD_D^2 \times C_L$$

where:

f_{SW} is the switching frequency, which is a fraction of the clock frequency related to the switching activity of that gate during a period of time.

VDD_D is the digital supply voltage.

C_L is the capacitive load of the gate, which is the inherent capacitance of its PMOS/NMOS devices and the load at the output of the gate.

Reducing the power dissipation of a high-speed digital block requires reducing its supply voltage and/or the devices size.

Smaller process geometries have thinner devices and the supply voltage also reduces with the process. Therefore, the demand for lower power solutions on fast processing digital chips is one of the drivers of the technology shrink.

Static power dissipation of an analog circuit, P_{ana}, is given by:

$$P_{ana} = I_{BIAS} \times VDD_A$$

where

I_{BIAS} is the analog circuit biasing current.

VDD_A is the analog supply voltage.

Static biasing current depends on the circuit function and performance requirements. Depending if the goal is low noise, high gain or low distortion, the biasing current specifications will change. But, in general, the current increases for higher frequency circuits operation and higher precision circuits.

Precision

Precision and Accuracy are two important parameters, sometimes used with the same meaning, although they refer to different things.

Precision reflects how repetitive a measurement is. Accuracy reflects how close a measurement is to its true value.

When a Precision ADC is required, it usually means that the error after conversion needs to be extremely small and the digital output word is a faithful representation of the analog input signal.

The performance specification of an ADC can be split into Dynamic Performance and Static Performance.

Dynamic Performance

Several parameters are defined and can be used to specify the dynamic performance of an ADC:

Spurious Free Dynamic Range (SFDR): measures the difference between the rms value of the input signal and the rms value of the largest spurious component.

Total Harmonic Distortion (THD): measures the ratio of the rms sum of the harmonic components to the rms value of the input signal.

Signal to Noise Ratio (SNR): measures the ratio of the rms value of the input signal to the rms sum of all other spectral components in the Nyquist bandwidth, excluding harmonic components.

A plot of a digitized signal spectrum can help understanding these parameters (Fig. 4)

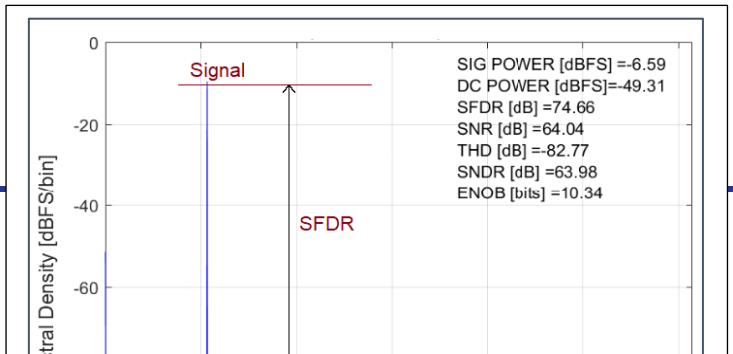


Figure 4: ADC Dynamic Performance

Static Performance

Static performance is particularly relevant when high accuracy measurements of DC signals are required. When accurate, precision measurements are important, all the errors need to be included in the total deviation between the real value and the measured value.

TUE (Total Unadjusted Error) is a static error specification representing the maximum deviation between real and measured values and it includes Offset, DC Gain Error and Integral Non-Linearity (INL).

Offset Error: the difference between the real and the ideal offset points. It corresponds to the mid-step value when the digital output is zero. (Fig. 5a).

Gain Error: the difference between the real and the ideal slope of the ADC output. It corresponds to the mid-step value when the digital output is full-scale. (Fig. 5b).

Offset error must be corrected before measuring the gain error.

Integral Non-Linearity: the maximum deviation of the output value to a straight-line characteristic (Fig. 5c).

Offset and Gain error are usually removed before measuring the INL.

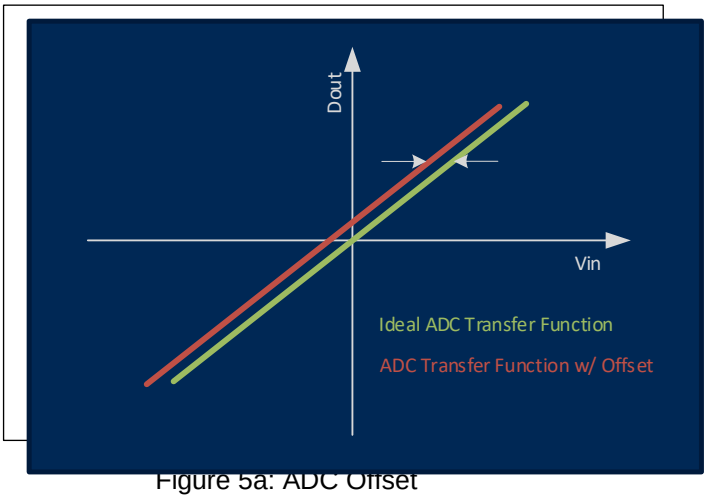


Figure 5a: ADC Offset

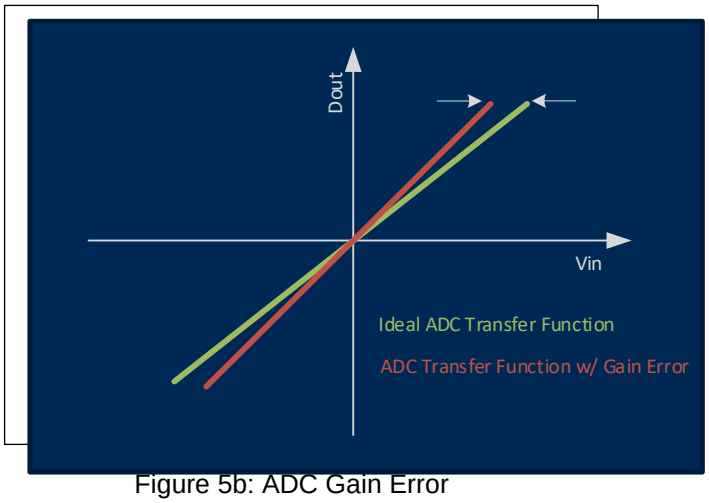
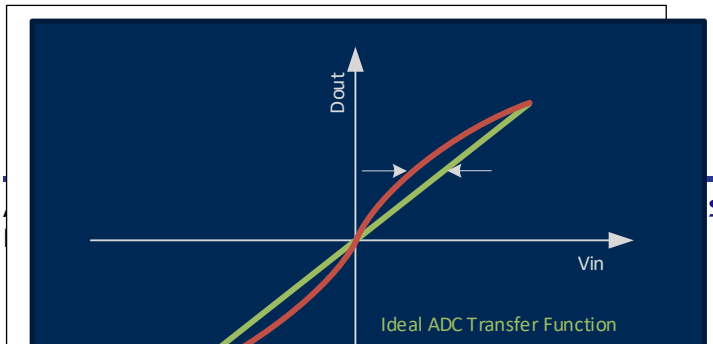


Figure 5b: ADC Gain Error



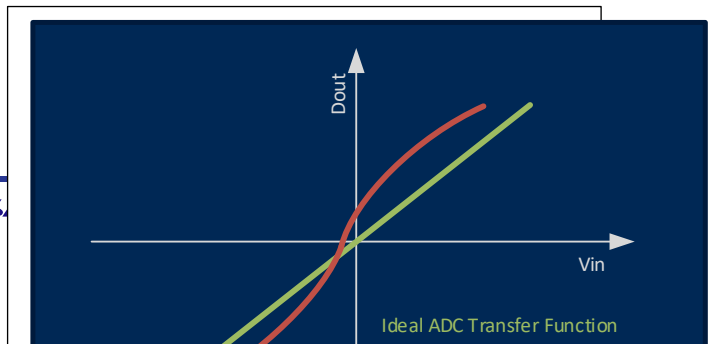


Figure 5c: ADC INL

Figure 5d: ADC Offset + Gain Error + INL

All these parameters contribute to the total inaccuracy and TUE (Total Unadjusted Error) is a useful specification to measure that deviation.

These errors being uncorrelated, can be expressed by the equation below:

$$TUE = \sqrt{Offset^2 + GainError^2 + INL^2}$$

Analog to Digital Converter Architectures

There are many architecture types, and each has its advantages and disadvantages.

Parallel type ADCs are extremely fast converters. Noise-shaping modulators allow the highest resolution converters.

Low latency requires high sampling rates, which means high power dissipation. Precision measurements require larger currents which means higher power dissipation. Low power requires low conversion rates.

So, what is the right architecture for Low-Latency, Low-Power, Precision ADCs?

Flash ADC

Flash ADCs, or Parallel ADCs, are the fastest converters. For an N-bit resolution ADC, a resistive ladder generates 2N-1 voltage references and 2N-1 comparators, that compare in parallel the references voltages to the input signal. The outputs of those comparators are combined to generate a digital output word.

As the comparators work in parallel, using high-speed comparators allows the achievement of very high-speed conversion rates and very low latencies.

This is however, at the cost of high-power consumption and large area. The number of comparators increases exponentially with the ADC resolution. The same is valid for the resistors and logic.

As the resolution increases, the area, power and complexity increase significantly, making these converters not very attractive for high resolution, precision converters.

The increase in the number of comparators also increases the input capacitance of the ADC, requiring much higher power dissipation buffers to drive the ADC.

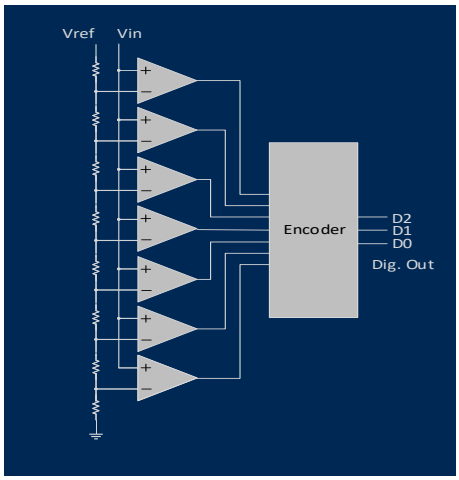
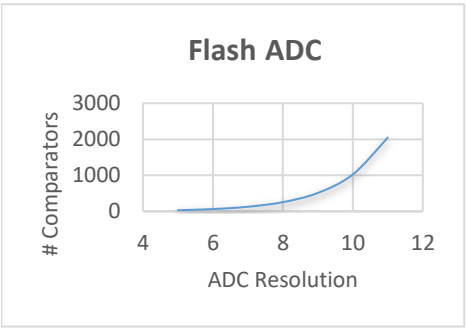


Figure 6: Flash ADC Block Diagram



Delta Sigma ADC

Delta-Sigma ADCs are oversampled converters implemented with a Modulator and a Decimation Filter.

The Delta-Sigma modulation shapes the quantization noise, pushing it into higher frequencies.

Digital filtering of that high frequency noise, results in large SNR performances, suitable for precision conversions.

Fig. 9 shows the Noise Spectral Density for a Nyquist Convert, an Oversampled Converter and an Oversampled Converter with Noise-Shaping. Oversampling a signal, spreads the total noise power in a larger bandwidth, reducing the Noise Spectral Density within the signal bandwidth. Shaping the noise with a High-Pass filtering transfer function further reduces the Noise Spectral Density in the signal bandwidth. Low-Pass filtering the Modulator output bitstream signal before Decimation, removes all the out-of-band noise and avoids noise folding back to the signal bandwidth.

The Delta-Sigma modulation order determines the High-Pass filter transfer function for the quantization noise. A first-order modulator shapes the quantization noise at 20dB/dec; a second-order modulator shapes the noise at 40dB/dec, etc.

With a higher order modulation and a large oversampling ratio (i.e. the ratio between the oversampled and the Nyquist rates) it is possible to achieve very high performance.

The digital output word is obtained after filtering and decimating the high frequency bitstream. Implementing the digital filters as FIR (Finite

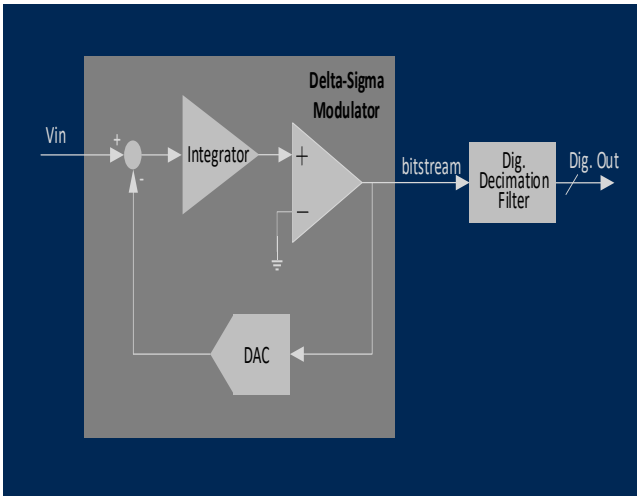


Figure 8: Delta-Sigma ADC Block Diagram

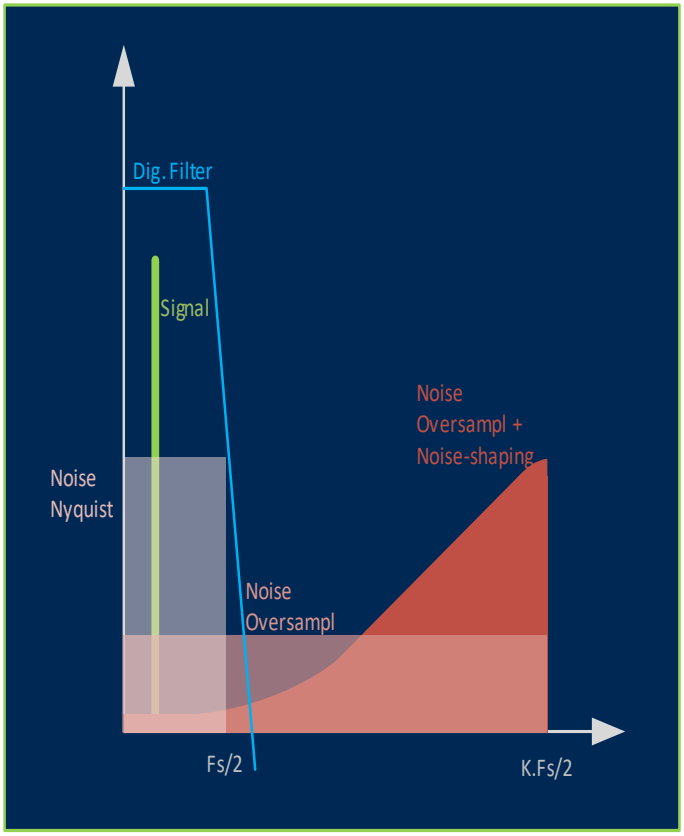


Figure 9: Oversampling and Noise-Shaping

Impulse Response) or IIR (Infinite Impulse Response) depends on several factors: phase distortion, efficiency, stability, etc. But the digital filter group delay will contribute to increase the overall ADC latency. Its settling time is also a limitation for applications requiring multiple channels time-multiplexed conversion.

As such, Delta-Sigma ADC architecture is not the best option for converters required for low-latency applications.

Pipeline ADC

This ADC is implemented as a pipeline of stages, each one with a number of bits smaller than the overall ADC resolution.

Each stage samples and holds (S&H) the input signal and quantizes it to the stage output resolution. This digital word is then converted back to analog by the DAC and subtracted to the held signal, generating a residue. This residue is then amplified and sampled by the next stage S&H.

Once the following stage samples the signal, the present stage can start sampling the next input sample. Due to the signal pipelining, a timing alignment is required at the output to recover the output digital code.

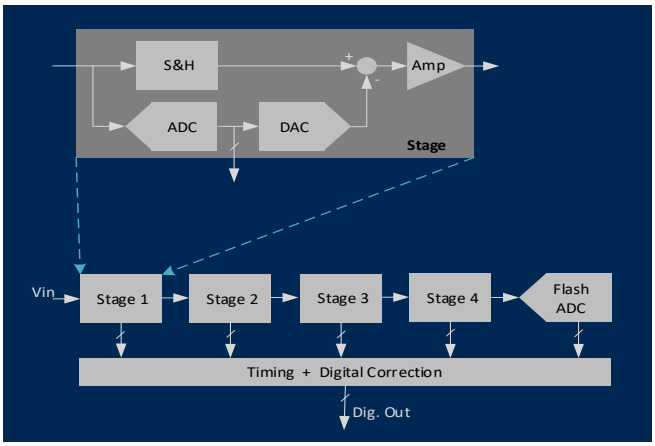


Figure 10: Pipeline ADC Block Diagram

While the pipeline signal processing achieves faster sampling rates, it also increases the latency. Every analog input sample must go through all the pipeline stages before a digital output word can be made available. A higher number of stages corresponds to a larger latency.

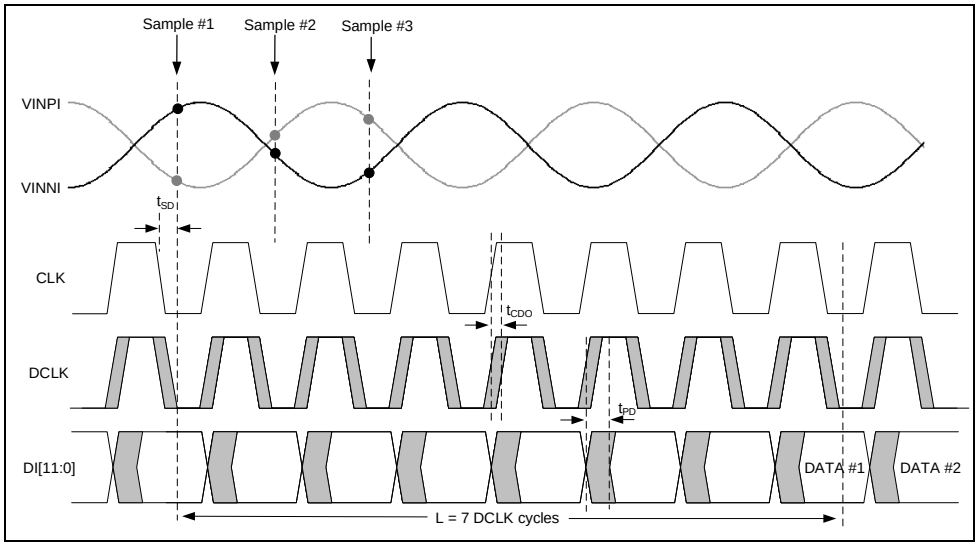


Fig.11: Pipeline ADC Timing Diagram. Example with 7 clock cycles latency.

Despite the reasonably low power dissipation figures of pipeline ADCs, the larger latency is a disadvantage for applications requiring low latency.

Successive Approximation Register (SAR) ADC

In a simple implementation of a SAR ADC, the input signal is sampled and held, and it is then compared to successive reference voltages by a single comparator working at a higher frequency than the sampling rate.

The Successive Approximation Register (SAR) name is related to the binary search algorithm used to find the digital output code representative of the input signal.

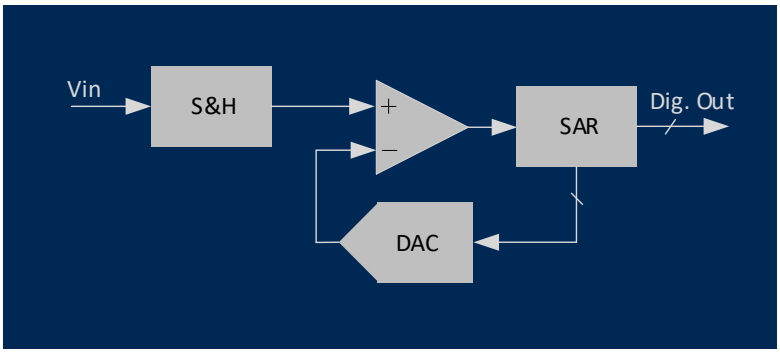


Fig.12: SAR ADC Block Diagram

Fig. 13 represents the steps in time of a 3-bit SAR ADC. After the signal is held, the comparator compares that signal to mid-scale of the input range, i.e. VREF/2. As the signal voltage level is higher than mid-scale, the comparator outputs “1”. This is the first comparator decision which corresponds to the MSB (Most Significant Bit). Based on this decision, the SAR digital block reconfigures the DAC for the next decision to be VREF/2 + VREF/4.

The next comparator decision is “0” (the input held signal is lower than VDAC), indicating that the DAC voltage must be reduced. For the next decision, the SAR digital block reconfigures the DAC to VREF/2 + VREF/4 - VREF/8.

The last decision is still “0”, as the input signal is still lower than VDAC. This is the LSB (Least Significant Bit).

The resulting output digital word is D[2:0] = “100”.

The SAR ADC is then ready for sampling a new input signal sample to be converted.

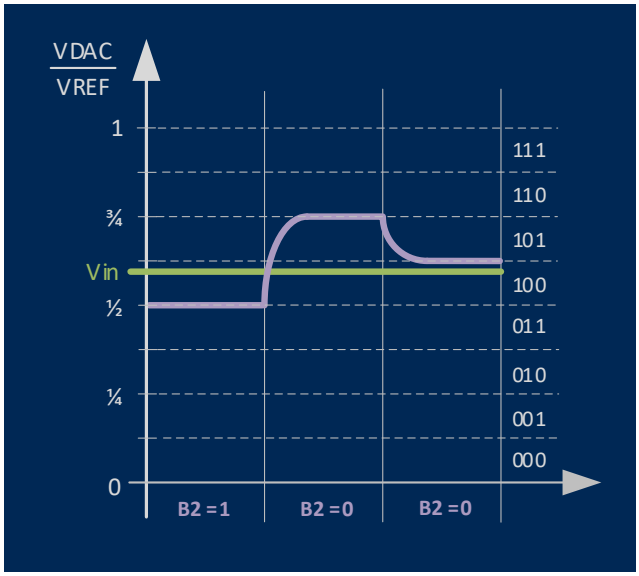


Figure 13: Successive Approximation Register: example for a 3-bit ADC

This architecture is used since the 1970s. It was used mostly for applications requiring only moderate resolution and speeds due to the limitations on the technology and the speed of the digital logic and the comparator.

But with technology scaling there is a significant increase in the speed and reduction in the digital power dissipation.

It also made it possible to integrate reasonably complex calibration algorithms with only a small area increase. Such calibrations overcome the technology limitations for higher resolutions and helped optimize the converters area and power efficiency.

The SAR ADC has become an extremely power-efficient architecture, achieving high sampling rates as well as high resolution. With an SNR > 60dB, SAR ADCs can work at tens or hundreds MSps while keeping very competitive power dissipation figures.

As the SAR ADC comparator works at a frequency higher than the sampling clock, the digital output is available just after the sampling period or delayed only by any latency from calibration. This makes the SAR ADC the lowest latency architecture available.

With all these features, the SAR ADC is the best architecture for Low-Latency, Low-Power Analog-to-Digital Converters. Renesas, formerly Dialog's DIAS Family SAR-ADCs were designed to meet these requirements.

DIAS ADCs: Low-Latency, Low-Power, Precision Converters

Renesas, formerly Dialog has a large number of silicon-proven ADCs in its DIAS Family, available in multiple processes and geometries. These ADCs were designed to fit the challenging requirements of the Industrial IoT market. They are extremely flexible and also suitable for other markets including communications, automotive and consumer.

Besides Low-Latency and Low-Power, the DIAS ADCs have several other features very important in an industrial environment. Some of these characteristics are reviewed in this section.

S3ADS40M12BT40ULPB is a 12-bit resolution SAR ADC designed in 40nm Ultra Low-Power Embedded-Flash process.

With a sampling rate of 40MSps, it has a Latency of 25ns and a total supply current of 2.2mA.

With 0.08mm^2 area, the Dynamic Performance includes 65.4dB SNR and Total Harmonic Distortion below -75.0dB. It also has a high Static Performance with no missing codes and including < +/-1% Gain Error and < 8mV Input Referred Offset.

The low-latency, low-power and high-performance, makes this ADC a perfect solution for instrumentation and control systems, industrial motor controls, and precision control loops.

Several other built in features and parameters are worth mentioning.

Multiplexed Input Channels

This ADC has up-to 16 individual input channels that can be connected to different signals. The ADC can be continuously converting a single channel, or it can be configured to convert multiple channels in a time-multiplex scheme.

In an industrial environment, there are usually multiple sensors and having a multiplexed analog input bus is an important feature for an ADC.

The channel selection can be changed on-the-fly during conversion.

Input Signal Range

The input signal voltage range goes from 0V to 3.63V. Such large signal range is a valuable feature in a multi-sensor environment. In a single solution, different sensors can be measuring battery voltage levels, temperature, pressure, humidity, or leakage current. And this results in voltage levels from a few mV to several Volts.

Without a large input signal voltage range ADC, many of these channels would require a gain amplifier, increasing the power dissipation and adding cost and complexity to the solution.

Input Common-Mode Range

Within the input signal range, there are no limitations with respect to the common-mode voltage. The ADC has a high common-mode rejection ratio, and it will convert the input differential signal, independently of its common-mode voltage.

Input Signal Type

Another important feature of this ADC is its compatibility with multiple input signal types:

- Pseudo-Differential Unipolar
- Pseudo-Differential Bipolar
- Fully-Differential

Figures 15a to 15c represent each signal type.

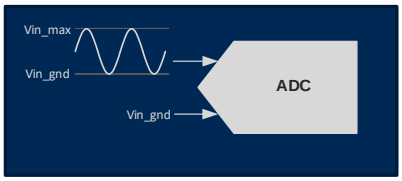


Fig.15a: Pseudo-Diff.

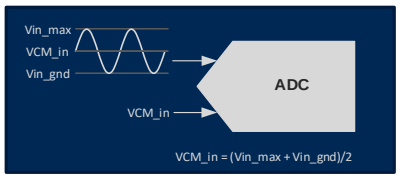


Fig.15b: Pseudo-Diff. Bipolar

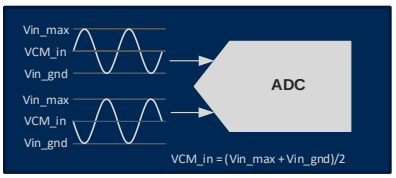


Fig.15c: Fully-Differential

Small Input Capacitance

Despite the high dynamic performance of 65.4dB SNR, the input capacitance of this switched-cap ADC is only 1.0pF.

This low input capacitance strongly relaxes the specification requirements and the power dissipation of the amplifier driving the ADC.

Adjustable Tracking Period

Another feature that helps relaxing the specification requirements of the circuit driving the ADC is the Adjustable Tracking Period.

By controlling the time window allowed to charge the ADC input capacitance, the same ADC can be used to convert signals from both large and small output driving current amplifiers.

Fig. 16 shows an example of an extended track phase timing diagram.

By setting TRACK = ‘1’ during 2 clock periods, the tracking time increases from ½ clock cycle to ½+2 clock periods.

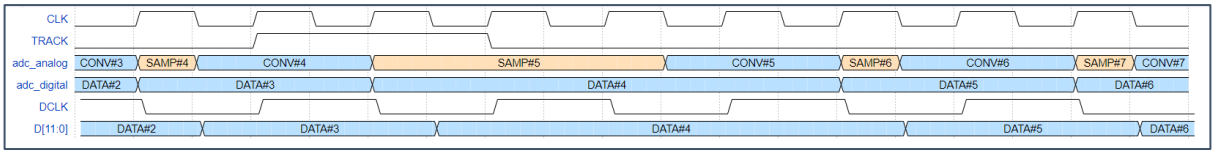


Fig.16: Extended track phase timing diagram

Wide Range Sampling Rate with Scaling Power Dissipation

The minimum latency is obtained with the 40MSps sampling rate. But for applications where lower power is more important than lower latency, the sampling rate can be reduced to any other rate just by reducing the clock frequency. The S3ADS40M12BT40ULPB is designed such that the power dissipation will scale down reasonably linearly with the sampling rate.

This makes this ADC extremely flexible to be used for multiple different applications.

Supply Noise Immunity

An industrial environment can be quite noisy, and the ADC has to be robust enough to convert accurately despite the noisy environment. For that reason, a Reference Buffer is included in the IP to buffer the VREF voltage needed for the ADC but also to filter that reference voltage.

With the purpose of having the gain error referred to the supply voltage, S3ADS40M12BT40ULPB reference voltage is the same as AVDDIO. But otherwise it can be replaced by a Bandgap voltage reference.

Operating Modes

This ADC has 3 operating modes:

- Power-Down Mode
- Standby Mode
- Active Mode

In Power-Down mode, all the blocks are powered-down and there is no power dissipation.

In Standby mode, the ADC core is powered down, but the Reference Buffer is enabled.

In Active mode, all the blocks are enabled.

During Standby mode, the power dissipation is less than 1/10 of Active Mode. And Wake-up time from Standby mode is about 4 times faster than Wake-up time from Power-Down mode.

As such, Standby mode is an interesting option to save power during idle periods, when a fast wake-up time is required.

Digital Output Format

For digital interface flexibility, two digital formats are available: straight binary and 2’s complement. Fig. 18 shows an example, using a fully differential input signal.

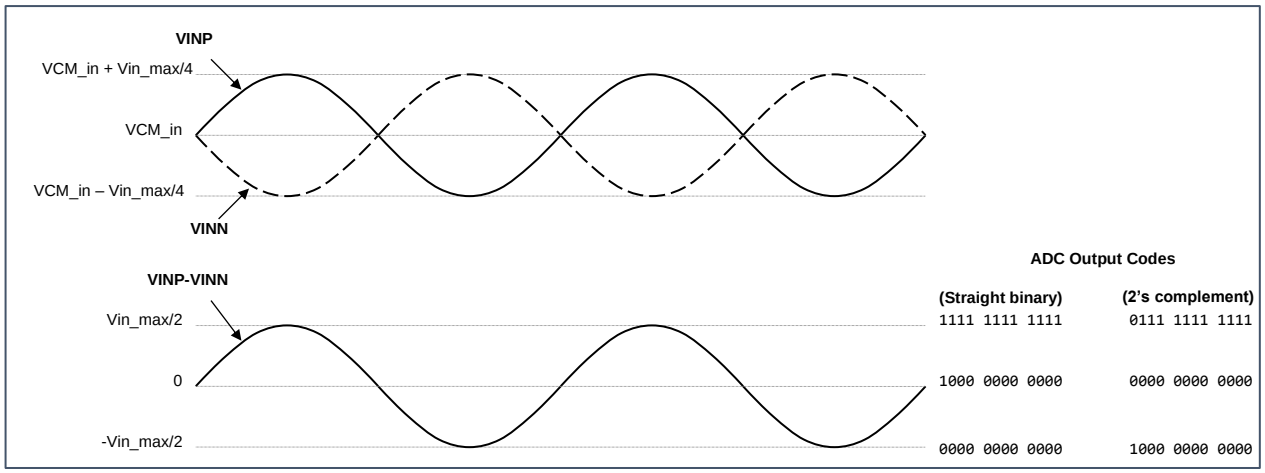


Fig.17: ADC digital output formats

S3ADS1M14BT40ULPB is another interesting IP. This ADC has a few additional features that makes it very flexible and attractive.

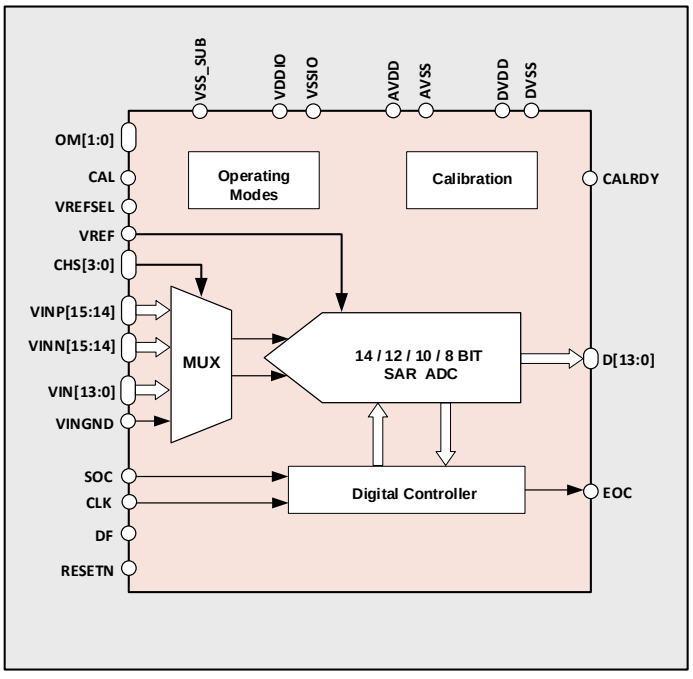


Fig.19: S3ADS1M14BT40ULPB Block Diagram

Programmable Resolution

The S3ADS1M14BT40ULPB ADC resolution can be controlled by the user as 14-bit, 12-bit, 10-bit or 8-bit. The 14-bit resolution mode has an Effective Number of Bits ENOB = 12-bit. The 8-bit resolution mode has an ENOB = 7.5-bit.

For those systems requiring less precision, a lower resolution mode can be selected, reducing the power dissipation.

Low Power and Calibration

With a die area of 0.055mm^2, the S3ADS1M14BT40ULPB low-power and high precision is obtained with built-in calibration. This calibration needs to be run only once, and the ADC performance remains valid despite variations in the Supply Voltages or any temperature changes from -40degC to 125deC. The calibration process does not require any input signal and all calibration reference signals are generated internally.

When the ADC is powered down, the calibration coefficients are kept on internal memory elements. After resuming activity, the ADC continues to use the calibration coefficients previously saved. For longer powered-down periods and to minimize the power dissipation through current leakage, the analog supplies may be removed, and only the digital domain DVDD remains available to supply the memory elements. In this mode, the power dissipation is around 10nW.

Once calibrated, the ADC can resume instantaneously from power-down to active, making it similarly efficient for single-conversion or continuous conversion. Assuming a conversion activity (duty-cycle) around 10%, the integrated supply current is below 15□A, when the ADC is converting at 14-bit resolution and 1.2MSps sampling rate.

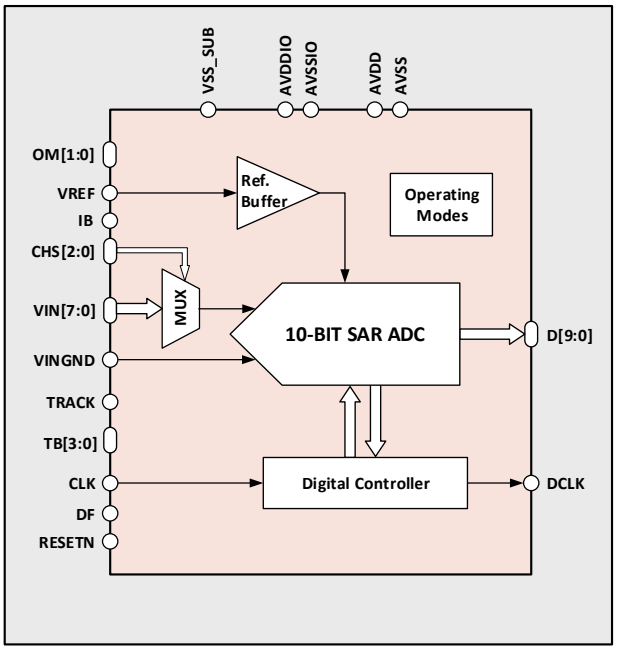


Fig.20: S3ADS1M14BT40ULPD Block Diagram

S3ADS1M10BT40ULPD is an ADC IP designed for ultra-low power applications.

With 10-bit resolution and a die area of 0.025mm^2 including the Reference Buffer, this ADC has an ENOB of 8.8-bit.

With no missing codes over the full PVT range, this ADC does not require any calibration. That allows the ADC to go from power-down (or even no-supplies) to active, fully on-spec, in less than 15us.

For long idle periods, the ADC can be powered down and the supplies can be removed to avoid any leakage currents.

While in continuous conversion, the total supply current is 17□A.

Conclusions

The ADC is a key element in any Analog Front End. In an era in which every device is connected to any other nearby device and connected to remote systems through servers or clouds, the converters have a critical role in the systems' operation.

Every system has its own requirements and choosing the right converters for each application determines how efficient those systems will be. Over-specifying converter's parameters will increase the costs and the complexity. Under-specification will reduce the performance and limit the scope of applications. Choosing the right ADC architecture is critical for an optimized solution.

This article focused on the Low-Latency, Low-Power Precision ADCs targeting the expanding IoT market, but also other markets including automotive, medical and consumer.

The DIAS Family SAR-ADCs were designed for these applications and they offer the best in-class converters available in the market.

Several IPs were mentioned in this Article as examples to describe the multiple features available in these ADCs which make them unique optimized solutions for any system.

Revision History

Revision	Date	Description
1.0	Aug 01, 2019	Initial release.
1.1	Dec 22, 2021	Rebrand