[Notes]

e² studio Code Generator Plug-in

Outline

When using the products in the title, note the following point:

1. Saving linker option settings

1. Saving Linker Option Settings

1.1 Applicable Products

➢ Renesas CC-RL C Executable Project of e² studio V6.2.0 (Code Generator Plug-in V2.10.0) or later

1.2 Applicable MCUs

➢ RL78 family:

RL78/D1A, RL78/F12, RL78/F13, RL78/F14, RL78/F15, RL78/F1E(*),
RL78/G10, RL78/G11, RL78/G12, RL78/G13, RL78/G14, RL78/G1A, RL78/G1C, RL78/G1D,
RL78/G1E, RL78/G1F, RL78/G1G, RL78/G1H,
RL78/H1D, RL78/I1A, RL78/I1B, RL78/I1C, RL78/I1D, RL78/I1E,
RL78/L12, RL78/L13, RL78/L1A, and RL78/L1C groups

(*): Supported by e² studio V7.0.0 or later

1.3 Details

If you perform settings for any of the following peripheral functions in a Renesas CC-RL C executable project, the settings are reflected in linker options during code generation. However, the reflected linker option settings are not saved with the project. Therefore, if you reload the project and rebuild it without generating code, an intended object file will not be created because the linker option settings are incorrect.

➢ Peripheral function settings:

• Clock generator→ Clock settings (*)

• Clock generator→ On-chip debugging settings

• Clock generator → Data flash

• Watchdog timer

• Voltage detector

(*): "→" indicates an item to be selected on the tab for the clock generator.

➢ Linker option settings (Operation: Settings after selecting [Linker] → [Device])

• Security ID value

• Reserve working memory for RRM/DMM function → Start address area

• Secure memory area of OCD monitor → Memory area

• Set user option byte → User option byte value

• Set enable/disable on-chip debug by link option → On-chip debugging control value

• RAM area without section

➢ Linker Option Setting Window Example (Properties for RL78/G14)
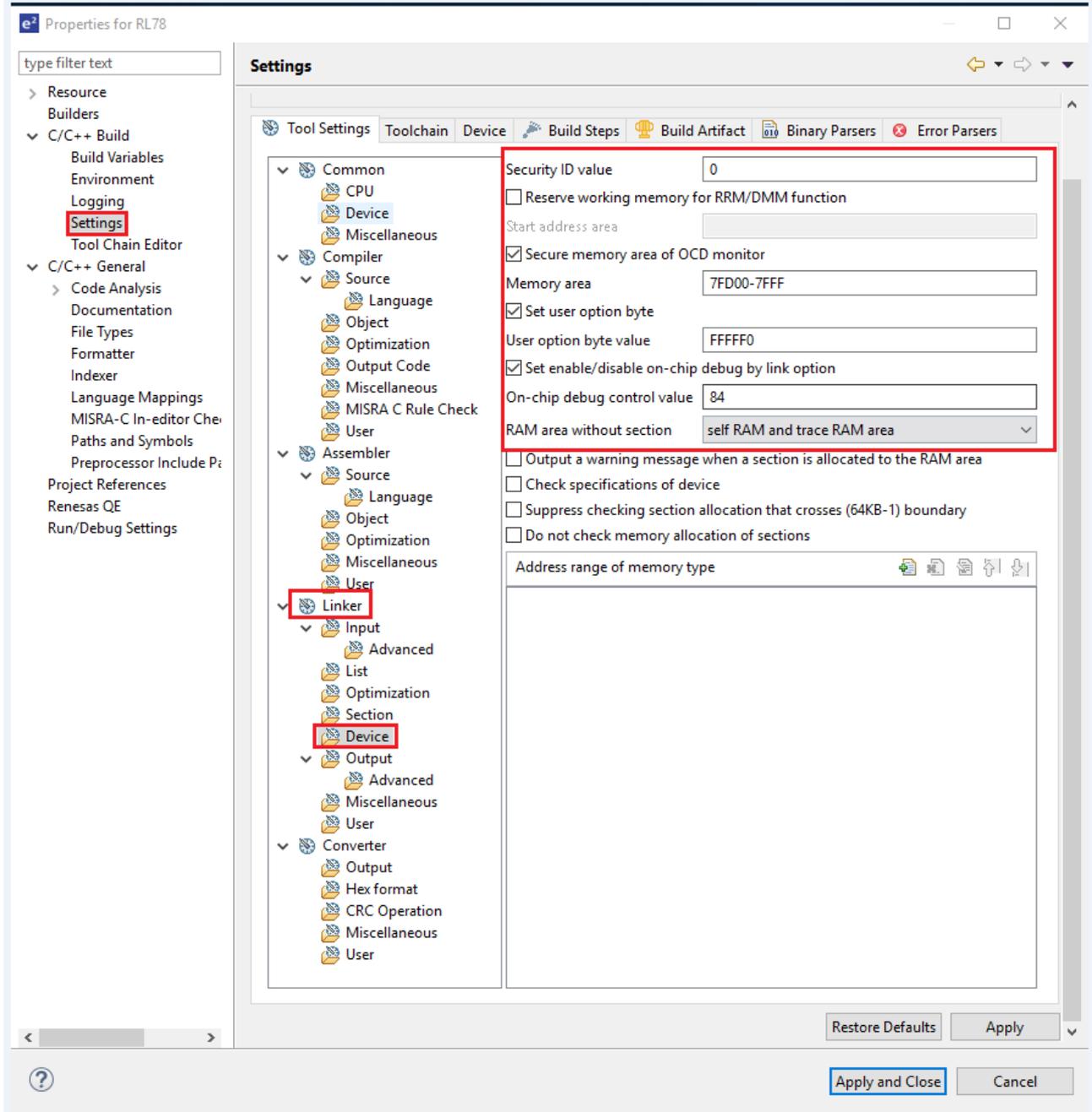
1.4   Workaround

To save the linker option settings reflected during code generation, select [Apply] → [Apply and Close] in the window shown below before closing the project.
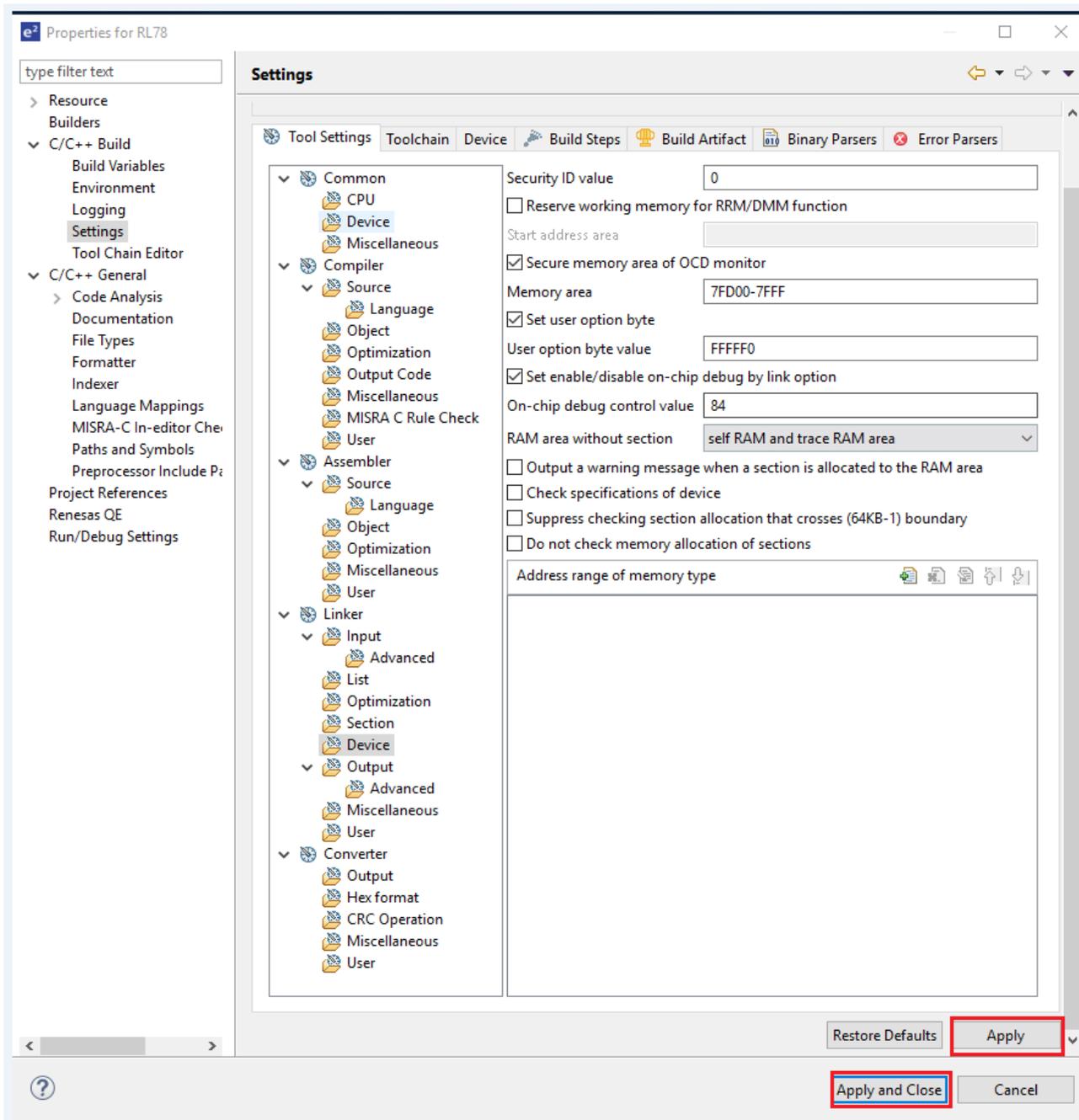
1.5   Schedule for Fixing the Problem

This problem will be fixed in a later version. (Scheduled to be released in July 2019.)

Revision History

Rev.	Date	Description	
		Page	**Summary**
1.00	Mar.16.19	-	First edition issued

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit: www.renesas.com/contact/.