

RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-SY*-A0037B/E	Rev.	2.0
Title	The restriction at switching a clock source		Information Category	Technical Notification		
Applicable Product	Renesas Synergy™ S7G2 MCU Group Renesas Synergy™ S5D9 MCU Group Renesas Synergy™ S5D5 MCU Group Renesas Synergy™ S5D3 MCU Group Renesas Synergy™ S3A7 MCU Group Renesas Synergy™ S3A6 MCU Group Renesas Synergy™ S3A3 MCU Group Renesas Synergy™ S3A1 MCU Group Renesas Synergy™ S124 MCU Group Renesas Synergy™ S128 MCU Group Renesas Synergy™ S1JA MCU Group	Lot No.	Reference Document	S7G2 Microcontroller Group User's Manual Rev.1.40 S5D9 Microcontroller Group User's Manual Rev.1.20 S5D5 Microcontroller Group User's Manual Rev.1.10 S5D3 Microcontroller Group User's Manual Rev.1.00 S3A7 Microcontroller Group User's Manual Rev.1.40 S3A6 Microcontroller Group User's Manual Rev.1.10 S3A3 Microcontroller Group User's Manual Rev.1.10 S3A1 Microcontroller Group User's Manual Rev.1.20 S124 Microcontroller Group User's Manual Rev.1.30 S128 Microcontroller Group User's Manual Rev.1.10 S1JA Microcontroller Group User's Manual Rev.1.30		
		All				

Renesas added a restriction at switching a clock source due to non-response from some interruptions which are RTC periodic interrupt, RTC periodic event output, internal asynchronous (AGT) interrupt and the external pin interrupt.

1. Restriction

When switching a clock source by changing SCKSCR.CKSEL[2:0] which is shown in Figure 1, clock output from the selector stops for 4 cycles of the switched clock as shown in Figure 2. Please follow the conditions below due to avoid not to accept the interrupt requests.

- 1) When using RTC periodical interrupt, RTC periodical event output or internal asynchronous interrupt, the clock source must be switched at a point in time when the interrupt or the event is not issued.
- 2) When using external interrupt, the pulse width must be added 4 clock cycles of switched source.

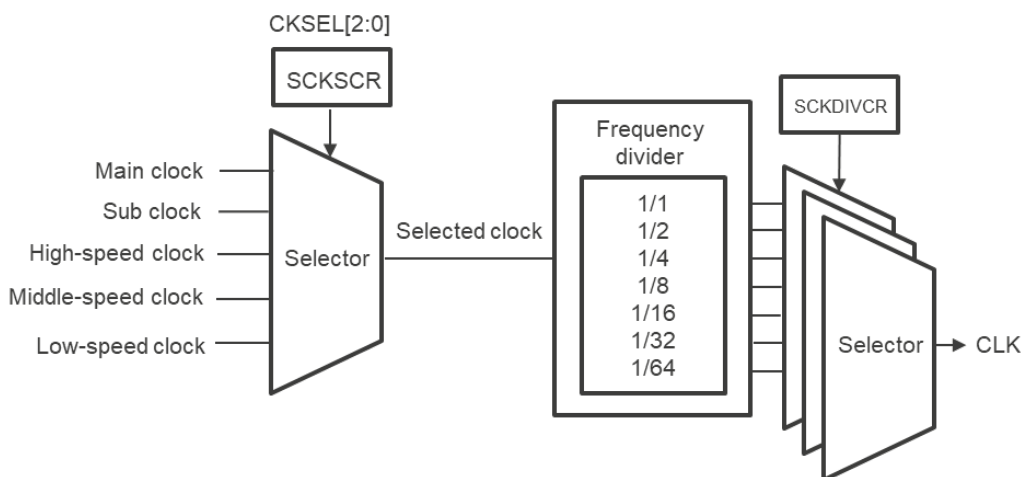


Figure1 Block diagram of clock source selector

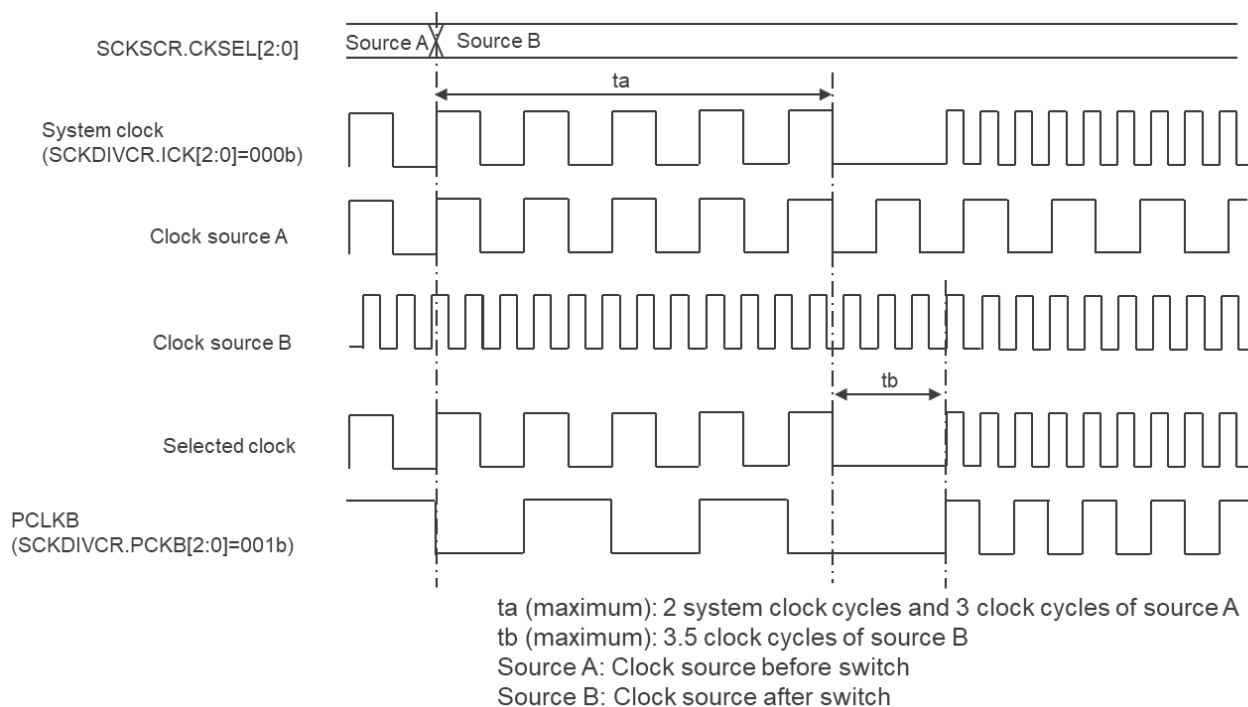


Figure2 Timing of clock source switching