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RENESAS TECHNICAL UPDATE

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Product Category	MPU/MCU		Document No.	TN-RA*-A0055A/E	Rev.	1.00
Title	RA6M4 Group, RA6M5 Group, RA4M3 Group, RA6E1 Group, correction of note on Cache specifications		Information Category	Technical Notification		
Applicable Product	RA6M4 Group RA6M5 Group RA4M3 Group RA6E1 Group	Lot No. All	Reference Document	RA6M4 Group User's Manual Hardware Rev.1.10 RA6M5 Group User's Manual Hardware Rev.1.10 RA4M3 Group User's Manual Hardware Rev.1.20 RA6E1 Group User's Manual Hardware Rev.1.10		

The note on Cache specifications is corrected.

[Before]

Table 14.9 Cache specifications

Parameter	C-cache	S-cache
Capacity	2 KB	2 KB
Way	2-way set associative	2-way set associative
Line size	32/64 bytes	32/64 bytes
Number of entry	32/16 entry/way	32/16 entry/way
Write way	No write	Write-through, non-write allocate
Replace way	2-way: LRU (least recently used)	2-way: LRU (least recently used)
Cache support area	0x0000_0000 to 0x1FFF_FFFF	0x20000000 – 0xDFFFFFFF*1 except Standby SRAM area (0x2800_0000 to 0x2FFFF_FFFF)

Note 1. Peripheral area 0x4000_0000 to 0x5FFF_FFFF must not have the cacheable attribution in the Arm MPU.

[After]

Table 14.9 Cache specifications

Parameter	C-cache	S-cache
Capacity	2 KB	2 KB
Way	2-way set associative	2-way set associative
Line size	32/64 bytes	32/64 bytes
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Write way	No write	Write-through, non-write allocate
Replace way	2-way: LRU (least recently used)	2-way: LRU (least recently used)
Cache support area	0x0000_0000 to 0x1FFF_FFFF	0x20000000 – 0xDFFFFFFF*1 except Standby SRAM area (0x2800_0000 to 0x2FFFF_FFFF)

Note 1. Peripheral area 0x4000_0000 to 0x5FFF_FFFF and QSPI I/O register area 0x6400_0000 to 0x67FF_FFFF must not have the cacheable attribution in the Arm MPU.