# RL78/G13, 78K0/Kx2

## Migration Guide from 78K0 to RL78: 8-Bit Timer/Event Counters 50 and 51 to Timer Array Unit

### Introduction

This application note describes how to migrate the 8-bit timer/event counters 50 and 51 of the 78K0/Kx2 to the timer array unit (TAU) of the RL78/G13.

### Target Device

RL78/G13, 78K0/Kx2

When using this application note with other Renesas MCUs, careful evaluation is recommended after making modifications to comply with the alternate MCU.

## Contents

# 1. Functions of 8-Bit Timer/Event Counters 50 and 51 and Timer Array Unit

Table 1.1 shows the functions of the 8-bit timer/event counters 50 and 51, and Table 1.2 shows the functions of the timer array unit (TAU).

Table 1.1 Functions of 8-Bit Timer/Event Counters 50 and 51

| Function | Explanation |
|---|---|
| Interval timer | 8-bit timer/event counters 50 and 51 generate an interrupt request at the preset time interval. |
| External event counter | 8-bit timer/event counters 50 and 51 can measure the number of pulses of an externally input signal. |
| Square-wave output | 8-bit timer/event counters 50 and 51 can output a square wave with any selected frequency. |
| PWM output | 8-bit timer/event counters 50 and 51 can output a rectangular wave whose output pulse width can be set freely. |

Table 1.2 Functions of Timer Array Unit

| Function | Explanation |
|---|---|
| Interval timer | Each timer of a unit can be used as a reference timer that generates an interrupt (INTTMmn) at fixed intervals. |
| Square wave output | A toggle operation is performed each time INTTMmn interrupt is generated and a square wave with a duty factor of 50% is output from a timer output pin (TOmn). |
| External event counter | Each timer of a unit can be used as an event counter that generates an interrupt when the number of the valid edges of a signal input to the timer input pin (TImn) has reached a specific value. |
| Divider | A clock input from a timer input pin (TI00) is divided and output from an output pin (TO00). |
| Input pulse interval measurement | Counting is started by the valid edge of a pulse signal input to a timer input pin (TImn). The count value of the timer is captured at the valid edge of the next pulse. In this way, the interval of the input pulse can be measured. |
| Measurement of high-/low-level width of input signal | Counting is started by a single edge of the signal input to the timer input pin (TImn), and the count value is captured at the other edge. In this way, the high-level or low-level width of the input signal can be measured. |
| Delay counter | Counting is started at the valid edge of the signal input to the timer input pin (TImn), and an interrupt is generated after any delay period. |
| One-shot pulse output | Two channels are used as a set to generate a one-shot pulse with a specified output timing and a specified pulse width. |
| PWM output | Two channels are used as a set to generate a pulse with a specified period and a specified duty factor. |
| Multiple PWM output | By extending the PWM function and using one master channel and two or more slave channels, up to seven types of PWM signals that have a specific period and a specified duty factor can be generated. |

Remark. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Each of the 8-bit timer/event counters 50 and 51 incorporated in the 78K0/Kx2 has one timer capture/compare register per timer counter register, one input pin, and one output pin.

The timer array unit (TAU) incorporated in the RL78/G13 has eight 16-bit timers. Each 16-bit timer is called a channel and can be used as an independent timer. In addition, two or more channels can be combined to serve as a higher-accuracy timer.

Each channel has one timer counter register, one timer data register, one input pin, and one output pin.

Table 1.3 shows the TAU functions corresponding to the 8-bit timer/event counters 50 and 51.

With the TAU, independent channels (single channel) or combined multiple channels can provide the functions equivalent to the 8-bit timer/event counters 50 and 51.

Table 1.3 Correspondence between Functions

| 78K0/Kx2<br>8-bit timer/event counters 50 and 51 | RL78/G13<br>Timer Array Unit (TAU) | |
|---|---|---|
| | Operation function | Channel operation |
| Interval timer | Interval timer | Independent |
| External event counter | External event counter | Independent |
| Square-wave output | Square wave output | Independent |
| PWM output | PWM output | Simultaneous |

The interval timers of the 8-bit timer/event counters 50 and 51 correspond to the interval timer function of the TAU.

The external event counters of the 8-bit timer/event counters 50 and 51 correspond to the external event counter function of the TAU.

The square-wave output function of the 8-bit timer/event counters 50 and 51 corresponds to the square-wave output function of the TAU.

The PWM output function of the 8-bit timer/event counters 50 and 51 corresponds to the PWM function of the TAU.

# 2. Differences between 8-bit timer/event counters 50 and 51 and Timer Array Unit

## 2.1 Summary of Differences between Functions

Table 2.1 summarizes the differences between the functions of the 8-bit timer/event counters 50 and 51 and TAU.

Table 2.1 Summary of Differences between Functions

| Item | 78K0/Kx2<br>8-bit timer/event counters 50 and 51 | RL78/G13<br>Timer Array Unit (TAU) |
|---|---|---|
| Configuration | 8-bit timer | 16-bit timer (Note1) |
| Count clock | $f_{PRS}$, $f_{PRS}/2$, $f_{PRS}/2^2$, $f_{PRS}/2^4$, $f_{PRS}/2^6$, $f_{PRS}/2^8$, $f_{PRS}/2^{12}$, $f_{PRS}/2^{13}$ | $f_{TCLK}$ ($f_{CLK}$ to $f_{CLK}/2^{15}$), $f_{SUB}$, $f_{IL}$ |
| Counter | TM5n register | TCRmn register |
| Count setting value | CR5n register | TDRmn register |
| Count Mode | Count up | Count up, Count down (Note3) |
| Operation Mode | • Interval timer<br>• External event counter<br>• Square-wave output<br>• PWM output | • Interval timer<br>• Square wave output<br>• External event counter<br>• Frequency divider (channel 0 of unit 0 only)<br>• Input pulse interval measurement<br>• Input signal high-/low-level width measurement<br>• Delay counter<br>• One-shot pulse output function (Note2)<br>• PWM output (Note2)<br>• Multiple PWM output (Note2) |
| Simultaneous channel operation function | Not applicable | Applicable (Note2) |
| Timer input | TI5n | TI00-TI07, TI10-TI17 |
| Timer output | TO5n, Output controller | TO00-TO07, TO10-TO17, Output controller |

Note 1. Channels 1 and 3 can be each used in 2-channel 8-bit timer configuration.

Note 2. Realized by combining master and slave channels.

Note 3. Depends on the mode.

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

## 2.2 Differences between Interval Timers

The interval timers of the 8-bit timer/event counters 50 and 51 of the 78K0/Kx2 correspond to the interval timer of the TAU of the RL78/G13.

Table 2.2 shows the differences between the interval timers.

Table 2.2 Differences between Interval Timers

| Item | 78K0/Kx2<br>8-bit timer/event counters 50 and 51 | RL78/G13<br>Timer Array Unit (TAU) |
|---|---|---|
| Count clock | $f_{PRS}$, $f_{PRS}/2$, $f_{PRS}/2^2$, $f_{PRS}/2^4$, $f_{PRS}/2^6$, $f_{PRS}/2^8$, $f_{PRS}/2^{12}$, $f_{PRS}/2^{13}$ | $f_{TCLK}$ ($f_{CLK}$ ~ $f_{CLK}/2^{15}$), $f_{SUB}$(Note), $f_{IL}$(Note) |
| Enable supplying the clock to the timer array unit | None | Setting the TAUmEN bit in the PER0 register to 1 |
| Count mode | Count up | Count down |
| Generation period of interrupt | (Set value of CR5n +1) ×Period of count clock | (Set value of TDRmn +1) ×Period of count clock |
| Interrupt occur timing | When the TM5n register value matches the CR5n register value and then the next count clock pulse (selected by the TCL5n register) is generated | - When TCRmn reaches 0000H and then the next count clock pulse (fMCK) is generated<br>- When count operation starts (only if MDmn0 bit in the TMRmn register is set to 1) |
| Starts count operation | Setting the TCE5n bit in the TMC5n register to 1 | Setting the TSmn bit in the TSm register to 1 |
| Stops count operation | Setting the TCE5n bit in the TMC5n register to 0 | Setting the TTmn bit in the TTm register to 1 |
| Counter value initialization timing | - When an interrupt occurs<br>- When count operation stops | - When count operation starts<br>- When an interrupt occurs |
| Acquires timer counter value | Reading the TM5n register | Reading the TCRmn register |

Note. Channel 5 only

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

## 2.3 Differences between External Event Counters

The external event counters of the 8-bit timer/event counters 50 and 51 of the 78K0/Kx2 correspond to the external event counter of the TAU of the RL78/G13.

Table 2.3 shows the differences between the external event counters.

Table 2.3 Differences between External Event Counters

| Item | 78K0/Kx2<br>8-bit timer/event counters 50 and 51 | RL78/G13<br>Timer Array Unit (TAU) |
|---|---|---|
| Enable supplying the clock to the timer array unit | None | Setting the TAUmEN bit in the PER0 register to 1 |
| Count mode | Count up | Count down |
| Setting for number of times of detection of external event input | CR5n register | TDRmn register |
| Interrupt occur timing | When the valid edge on the TI5n pin is detected for the times indicated by (set value of CR5n register + 1) | When the valid edge on the TImn pin is detected for the times indicated by (set value of TDRmn register + 1) |
| Detects valid edge | Level detection: Match 1 time (asynchronous edge detection) | When TNFENmn = 1,<br>Sampling clock: $f_{MCK}$<br>Level detection: Match 2 times in a row<br>When TNFENmn = 0,<br>Sampling clock: $f_{MCK}$<br>Level detection: Match 1 time (synchronized with $f_{MCK}$) |
| Starts count operation | Setting the TCE5n bit in the TMC5n register to 1 | Setting the TSmn bit in the TSm register to 1 |
| Stops count operation | Setting the TCE5n bit in the TMC5n register to 0 | Setting the TTmn bit in the TTm register to 1 |
| Counter value initialization timing | - When an interrupt occurs<br>- When count operation stops | - When count operation starts<br>- When an interrupt occurs |
| Acquires timer counter value | Reading the TM5n register | Reading the TCRmn register |
| Input pin | TI5n pin | TImn pin |

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

## 2.4 Differences between Square-Wave output

The square-wave output function of the 8-bit timer/event counters 50 and 51 of the 78K0/Kx2 corresponds to the square-wave output function of the TAU of the RL78/G13.

Table 2.4 shows the differences between the square-wave output functions.

Table 2.4 Differences between Square-Wave Output Functions

| Item | 78K0/Kx2<br>8-bit timer/event counters 50 and 51 | RL78/G13<br>Timer Array Unit (TAU) |
|---|---|---|
| Count clock | $f_{PRS}$, $f_{PRS}/2$, $f_{PRS}/2^2$, $f_{PRS}/2^4$, $f_{PRS}/2^6$, $f_{PRS}/2^8$, $f_{PRS}/2^{12}$, $f_{PRS}/2^{13}$ | $f_{TCLK}$ ($f_{CLK}$ to $f_{CLK}/2^{15}$), $f_{SUB}$(Note1), $f_{IL}$(Note1) |
| Enable supplying the clock to the timer array unit | None | Setting the TAUmEN bit in the PER0 register to 1 |
| Count mode | Count up | Count down |
| Square wave frequency | Frequency of count clock / {(Set value of CR5n + 1) × 2} | Frequency of count clock / { (Set value of TDRmn＋1) x 2 } |
| Interrupt occur timing | When the TM5n register value matches the CR5n register value and then the next count clock pulse (selected by the TCL5n register) is generated | - When TCRmn reaches 0000H and then the next count clock pulse ($f_{MCK}$) is generated<br>- When count operation starts (only if MDmn0 bit in TMRmn register is set to 1) |
| Starts count operation | Setting the TCE5n bit in the TMC5n register to 1 | Setting the TSmn bit in the TSm register to 1 |
| Stops count operation | Setting the TCE5n bit in the TMC5n register to 0 | Setting the TTmn bit in the TTm register to 1 |
| Counter value initialization timing | - When an interrupt occurs<br>- When count operation stops | - When count operation starts<br>- When an interrupt occurs |
| Acquires timer counter value | Reading the TM5n register | Reading the TCRmn register |
| Output level when timer output is disabled | Fixed to low (TOE5n = 0).<br>Can also be fixed to high by setting 1 to the port latch of the multiplexed pin. Set 0 to the above latch at the start of timer output. | TOmn bit setting in the TOm register<br>Valid only when TOEmn = 0. |
| Output level when timer operation starts | LVS5n and LVR5n bit setting in the TMC5n register.<br>Output level is inverted upon match between the TM5n register value and CR5n register value.<br>Valid only when PM17 = P17 = 0, and PM33 = P33 = 0. | TOmn bit setting in the TOm register after port output is enabled.<br>When MDmn0 = 1, output level is inverted after timer operation starts.<br>When MDmn0 = 0, output level is not inverted after timer operation starts.<br>Valid only when PMxx = Pxx =0, and PMCxx = 0. (Note2) |
| Output pin | TO5n pin | TOmn pin |

Note1. Channel 5 only

Note2. Refer to tables, Setting Examples of Registers and Output Latches When Using Alternate Function, in the RL78/G13 User's Manual: Hardware.

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0 to 7)

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

## 2.5 Differences from PWM output

The PWM output of the 8-bit timer/event counters 50 and 51 of the 78K0/Kx2 corresponds to the PWM function of the TAU of the RL78/G13.

Table 2.5 and Table 2.6 shows the differences between the PWM output.

Table 2.5 Differences between PWM output (1/2)

| Item | 78K0/Kx2<br>8-bit timer/event counters 50 and 51 | RL78/G13<br>Timer Array Unit (TAU) |
|---|---|---|
| Count clock | $f_{PRS}$, $f_{PRS}/2$, $f_{PRS}/2^2$, $f_{PRS}/2^4$, $f_{PRS}/2^6$, $f_{PRS}/2^8$, $f_{PRS}/2^{12}$, $f_{PRS}/2^{13}$ | $f_{TCLK}$ ($f_{CLK}$ to $f_{CLK}/2^{15}$), $f_{SUB}$(Note1), $f_{IL}$(Note1) |
| Enable supplying the clock to the timer array unit | None | Setting the TAUmEN bit in the PER0 register to 1 |
| Count mode | Count up | Count down |
| Period of output waveform | Period of count clock × 256 | Period of count clock ×<br>{Set value of TDRmn (Master) + 1} |
| High-level width of output waveform (Note2) | - When TMC5n1 = 0 (active high)<br>Period of count clock ×<br>(set value of CR5n register + 1)<br>- When TMC5n1 = 1 (active low)<br>Period of count clock ×<br>{256 - (set value of CR5n register + 1)} | - When TOLm = 0 (active high)<br>Period of count clock ×<br>{Set value of TDRmp (Slave)}<br>- When TOLm = 1 (active low)<br>Period of count clock ×<br>[ {Set value of TDRmn (Master) + 1} -<br>{Set value of TDRmp (Slave) }] |
| Interrupt occur timing | When the TM5n register value matches the CR5n register value and then the next count clock pulse (selected by the TCL5n register) is generated | - When count operation starts (master)<br>- When TCRmn reaches 0000H and then the next count clock pulse ($f_{MCK}$) is generated (master)<br>- When TCRmp reaches 0000H and then the next count clock pulse ($f_{MCK}$) is generated (slave) |
| Compare register update timing (software) | When INTTM5n is generated. After updating of CR5n, there must be an interval of at least three count clock cycles before the next updating operation. | When INTTMmn is generated by master channel |
| Compare register setting | CR5n setting is changed only when the active-level width is to be changed. | - TDRmn (master) setting is changed only when the period is to be changed.<br>- TDRmp (slave) setting is changed only when the high-level width (TOLm = 0) or low-level width (TOLm = 1) is to be changed. |

Note1. Channel 5 only

Note2. The 78K0/Kx2 outputs an inactive level after counting begins and until an overflow occurs.

Note3. Refer to tables, Setting Examples of Registers and Output Latches When Using Alternate Function, in the RL78/G13 User's Manual: Hardware.

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

Table 2.6 Differences between PWM output (2/2)

| | | |
|---|---|---|
| Starts count operation | Setting the TCE5n bit in the TMC5n register to 1 | Setting the TSmn bit in the TSm register to 1 |
| Stops count operation | Setting the TCE5n bit in the TMC5n register to 0 | Setting the TTmn bit in the TTm register to 1 |
| Acquires timer counter value | Reading the TM5n register | Reading the TCRmn register<br>Reading the TCRmp register |
| Output level when timer output is disabled | Fixed to low (TOE5n = 0).<br>Can also be fixed to high by setting 1 to the port latch of the multiplexed pin. Set 0 to the above latch at the start of timer output. | TOmn bit setting in the TOm register<br>Valid only when TOEmn = 0. |
| Output level when timer operation starts | TMC5n1 bit setting in the TMC5n register.<br>TMC5n1 = 0 : High level<br>TMC5n1 = 1 : Low level<br>Valid only when PM17 = P17 = 0, and PM33 = P33 = 0. | TOmp bit setting in the TOm register after port output is enabled.<br>Output level after timer operation starts is:<br>when TOLmp = 0, high level<br>when TOLmp = 1, low level.<br>However, valid only when PMxx = Pxx =0 and PMCxx = 0. (Note3) |
| Output pin | TO5n pin | TOmp pin |

Note1. Channel 5 only

Note2. The 78K0/Kx2 outputs an inactive level after counting begins and until an overflow occurs.

Note3. Refer to tables, Setting Examples of Registers and Output Latches When Using Alternate Function, in the RL78/G13 User's Manual: Hardware.

Remarks1. For 78K0/Kx2, n = 0, 1
For RL78/G13, m: Unit number (m = 0, 1), n: Channel number (n = 0, 2, 4, 6)
p: Slave channel number (n < p ≤ 7)

Remarks2. Different products are provided with different functions. For details, refer to the appropriate user's manuals (hardware).

## 3. Sample Code for Timer Array Unit

The sample code for the timer array unit is explained in the following application notes.

- RL78/G13 Timer Array Unit (Interval Timer) CC-RL (R01AN2576)
- RL78/G13 Timer Array Unit (PWM Output) CC-RL (R01AN2589)

## 4. Documents for Reference

User's Manual:

- RL78/G13 User's Manual: Hardware (R01UH0146)
- 78K0/Kx2 User's Manual: Hardware (R01UH0008)

  The latest versions can be downloaded from the Renesas Electronics website.

Technical Update/Technical News:

The latest information can be downloaded from the Renesas Electronics website.

## Revision History

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# General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)
   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on
   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state
   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins
   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals
   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin
   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between $V_{IL}$ (Max.) and $V_{IH}$ (Min.).
7. Prohibition of access to reserved addresses
   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products
   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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