RX660 Group, RX65N/651 Group

Differences Between the RX660 Group and the RX65N/651 Group

Introduction

This application note is intended as a reference to points of difference between the peripheral functions, I/O registers, and pin functions of the RX660 Group and RX65N/RX651 Group, as well as a guide to key points to consider when migrating between the two groups.

Unless specifically otherwise noted, the information in this application note applies to the 144-pin package version of the RX660 Group and the 177-pin package version of the RX65N/RX651 Group as the maximum specifications. To confirm details of differences in the specifications of the electrical characteristics, usage notes, and setting procedures, refer to the User's Manual: Hardware of the products in question.

Target Devices

RX660 Group and RX65N/RX651 Group

Contents

1. Comparison of Built-In Functions of RX660 Group and RX65N/RX651 Group

A comparison of the built-in functions of the RX660 Group and RX65N Group is provided below. For details of the functions, see section 2, Comparative Overview of Specifications and section 5, Reference Documents.

Table 1.1 is a Comparison of Built-In Functions of RX660 Group and RX65N Group.

Table 1.1 Comparison of Built-In Functions of RX660 Group and RX65N Group

Function	RX65N	RX660
CPU	▲	
Operating modes	■/▲	
Address space	▲	
Resets	○	
Option-setting memory (OFSM)	●/▲	
Voltage detection circuit (LVDA)	▲	
Clock generation circuit	▲	
Clock frequency accuracy measurement circuit (CAC)	○	
Low power consumption	▲	
Battery backup function	○	×
Register write protection function	▲	
Exception Handling	○	
Interrupt controller (ICUB for RX65N, and ICUF for RX660)	▲	
Buses	■/▲	
Memory-protection unit (MPU)	○	
DMA controller (DMACAa)	○	
EXDMA controller (EXDMACa)	○	×
Data transfer controller (DTCb)	○	
Event link controller (ELC)	▲	
I/O ports	▲	
Multi-function pin controller (MPC)	●/■	
Multi-function timer pulse unit 3 (MTU3a)	○	
Port output enable 3 (POE3a)	▲	
16-bit timer pulse unit (TPUa)	○	×
Programmable pulse generator (PPG)	○	×
8-bit timer (TMR for RX65N, and TMRb for RX660)	●	
Compare match timer (CMT)	○	
Compare match timer W (CMTW)	▲	
Realtime clock (RTCd for RX65N, and RTCC for RX660)	▲	
Watchdog timer (WDTA)	○	
Independent watchdog timer (IWDTa)	○	
Ethernet controller (ETHERC)	○	×
DMA controller for Ethernet controller (EDMACa)	○	×
USB2.0FS host or function module (USBb)	○	×
Serial communications interface (SCIg, SCIi, and SCIh for RX65N) (SCIk, SCIm, SCIh for RX660)	▲	

Function	RX65N	RX660
Serial communications interface (RSCI)	×	○
I²C bus interface (RIICa)	■	
CAN module (CAN): RX65N CANFD module (CANFD-Lite): RX660	●/▲	
Serial peripheral interface (RSPIc for RX65N, and RSPId for RX660)	▲	
Quad serial peripheral interface (QSPI)	○	×
CRC calculator (CRCA)	○	
SD host interface (SDHI)	○	×
SD slave interface (SDSI)	○	×
MultiMediaCard interface (MMCIF)	○	×
Parallel data capture unit (PDC)	○	×
Graphic LCD controller (GLCDC)	○	×
2D drawing engine (DRW2D)	○	×
Boundary scan	○	×
AESa	○	×
RNG	○	×
Remote control signal receiver (REMCa)	×	○
Trigonometric function calculator (TFU)	×	○
Trusted Secure IP (TSIP)	○	×
12-bit A/D converter (S12ADFa for RX65N, and S12ADH for RX660)	▲	
12-bit D/A converter (R12DAa for RX65N, and R12DAb for RX660)	▲	
Temperature sensor (TEMPS)	■/▲	
Comparator C (CMPC)	×	○
Data operation circuit (DOC for RX65N, and DOCA for RX660)	●/▲	
Standby RAM	○	×
RAM	■/▲	
Flash memory (FLASH)	●/▲	
Packages	▲	

○: Available, ×: Unavailable, ●: Differs due to added functionality, ▲: Differs due to change in functionality, ■: Differs due to removed functionality.

2. Comparative Overview of Specifications

This section presents a comparative overview of specifications, including registers.

In the comparative overview, red text indicates functions which are included only in one of the MCU groups and also functions for which the specifications differ between the two groups.

In the register comparison, red text indicates differences in specifications for registers that are included in both groups and black text indicates registers which are included only in one of the MCU groups. Differences in register specifications are not listed.

2.1 CPU

Table 2.1 is Comparative Overview of CPU.

Table 2.1 Comparative Overview of CPU

Item	RX65N	RX660
CPU	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv2) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers Basic instructions: 75 Floating point instructions: 11 DSP instructions: 23 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 × 64 bits • On-chip divider: 32 / 32 × 32 bits • Barrel shifter: 32 bits	• Maximum operating frequency: 120 MHz • 32-bit RX CPU (RXv3) • Minimum instruction execution time: One instruction per clock cycle • Address space: 4 GB, linear • Register set of the CPU — General purpose: Sixteen 32-bit registers — Control: Ten 32-bit registers — Accumulator: Two 72-bit registers • 113 instructions — Standard provided instructions: 111 — Basic instructions: 77 — Single-precision floating point instructions: 11 — DSP instructions: 23 — Instructions for register bank save function: 2 • Addressing modes: 11 • Data arrangement — Instructions: Little endian — Data: Selectable between little endian and big endian • On-chip 32-bit multiplier: 32 × 32 × 64 bits • On-chip divider: 32 / 32 × 32 bits • Barrel shifter: 32 bits
FPU	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard	• Single-precision floating-point (32 bits) • Data types and floating-point exceptions conform to IEEE 754 standard
Register bank save function	—	• Fast collective saving and restoration of the values of CPU registers • 16 save register banks

2.2 Operating Modes

Table 2.2 is Comparative Overview of Operating Modes, and Table 2.3 is Comparison of Operating Mode Registers.

Table 2.2 Comparative Overview of Operating Modes

Item	RX65N	RX660
Operating modes specified by mode setting pins	Single-chip mode	Single-chip mode
	Boot mode (SCI interface) Boot mode (USB interface) Boot mode (FINE interface)	Boot mode (SCI interface) User boot mode Boot mode (FINE interface)
Operating modes selected by register settings	Single-chip mode and user boot mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode	Single-chip mode and user boot mode On-chip ROM disabled extended mode On-chip ROM enabled extended mode

Table 2.3 Comparison of Operating Mode Registers

Register	Bit	RX65N	RX660
MDSR	—	—	Mode status register
SYSCR1	SBYRAME	Standby RAM enable bit	—
VOLSR	—	—	Voltage level setting register

2.3 Address Space

Figure 2.1 is a Comparative Memory Map of Single-Chip Mode.

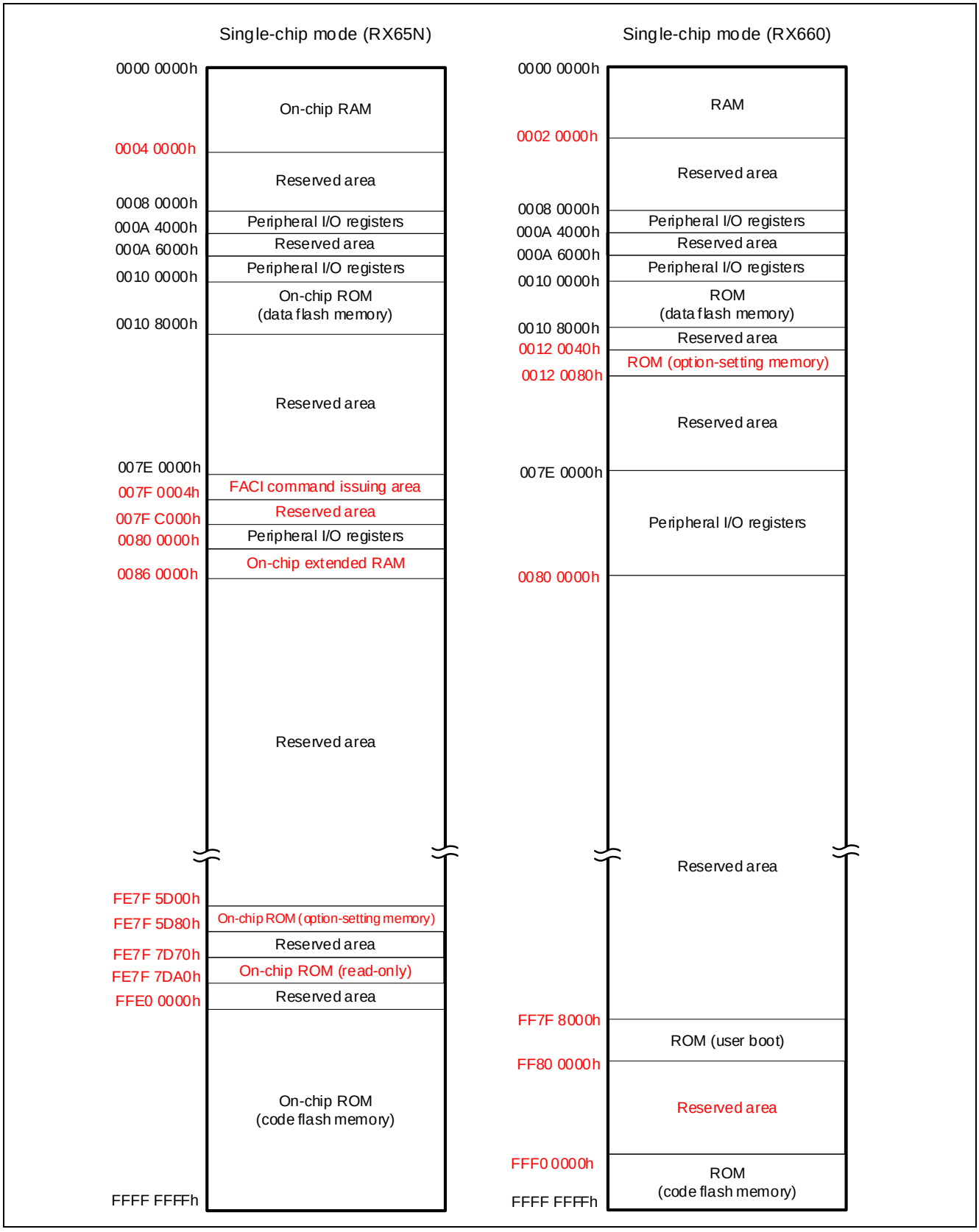

Figure 2.1 Comparative Memory Map of Single-Chip Mode

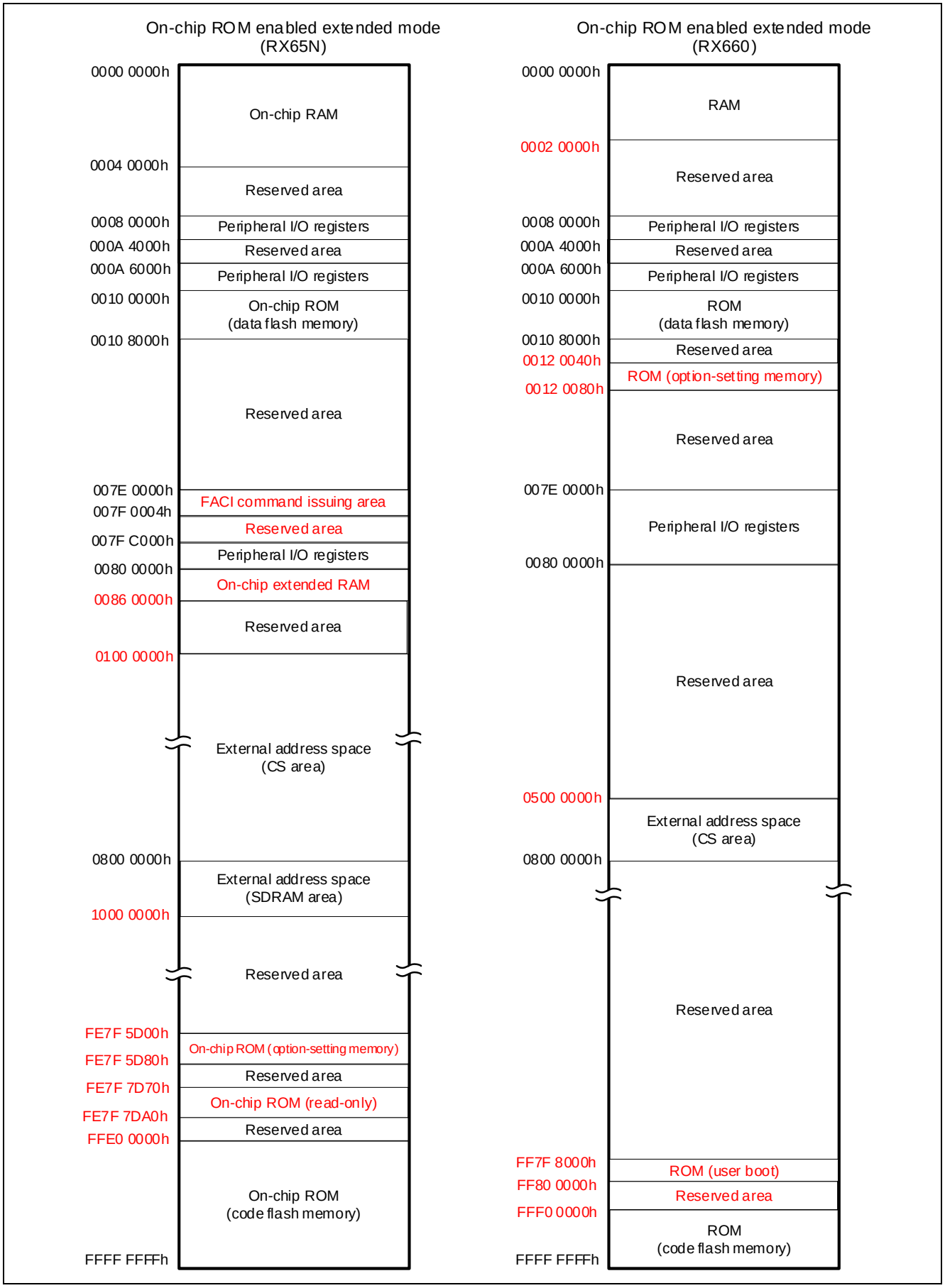

Figure 2.2 Comparative Memory Map of On-chip ROM Enabled Extended Mode

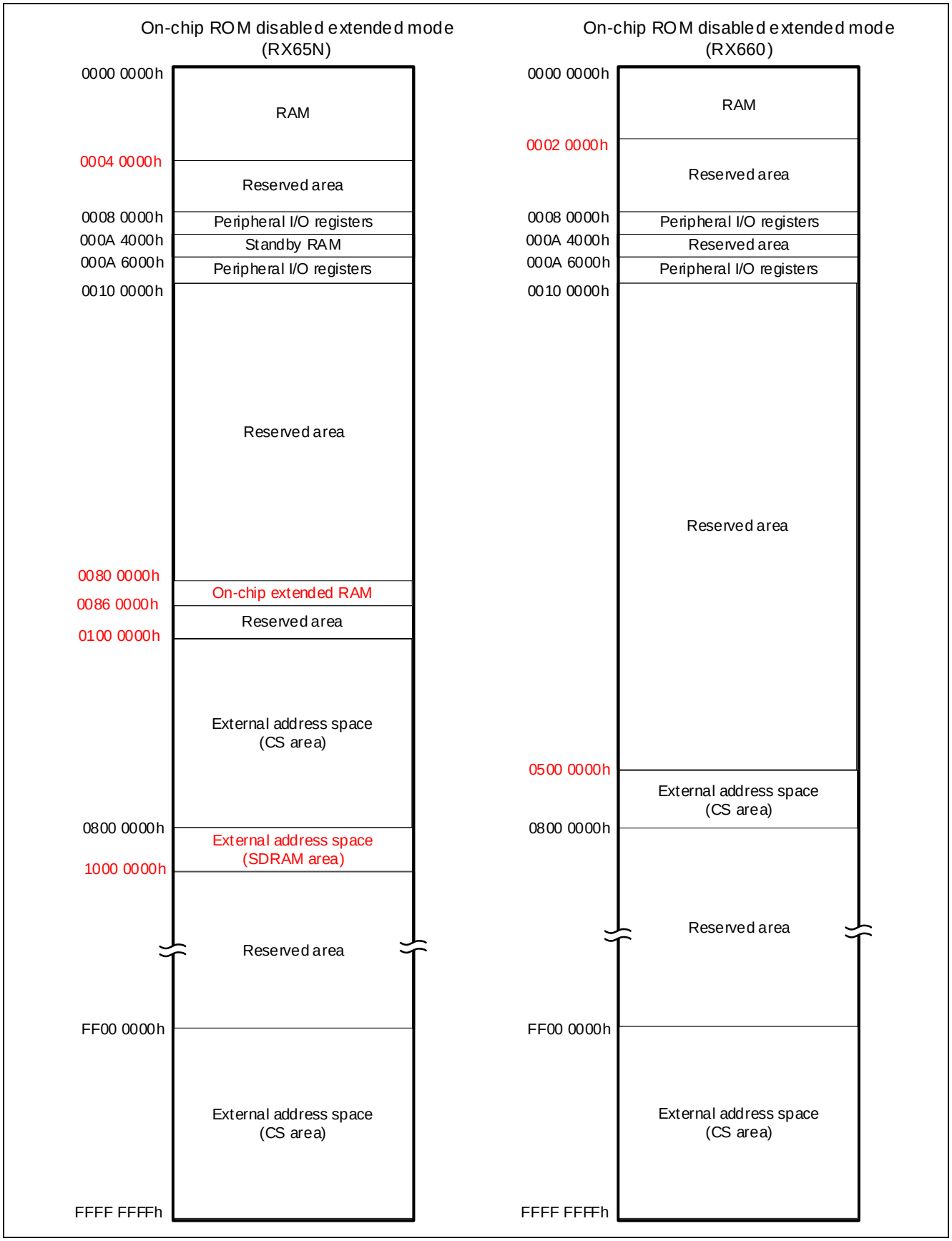

Figure 2.3 Comparative Memory Map of On-chip ROM Disabled Extended Mode

2.4 Option-Setting Memory

Figure 2.4 is a Comparison of Option-Setting Memory Areas, and Table 2.4 is a Comparison of Option-Setting Memory Registers.

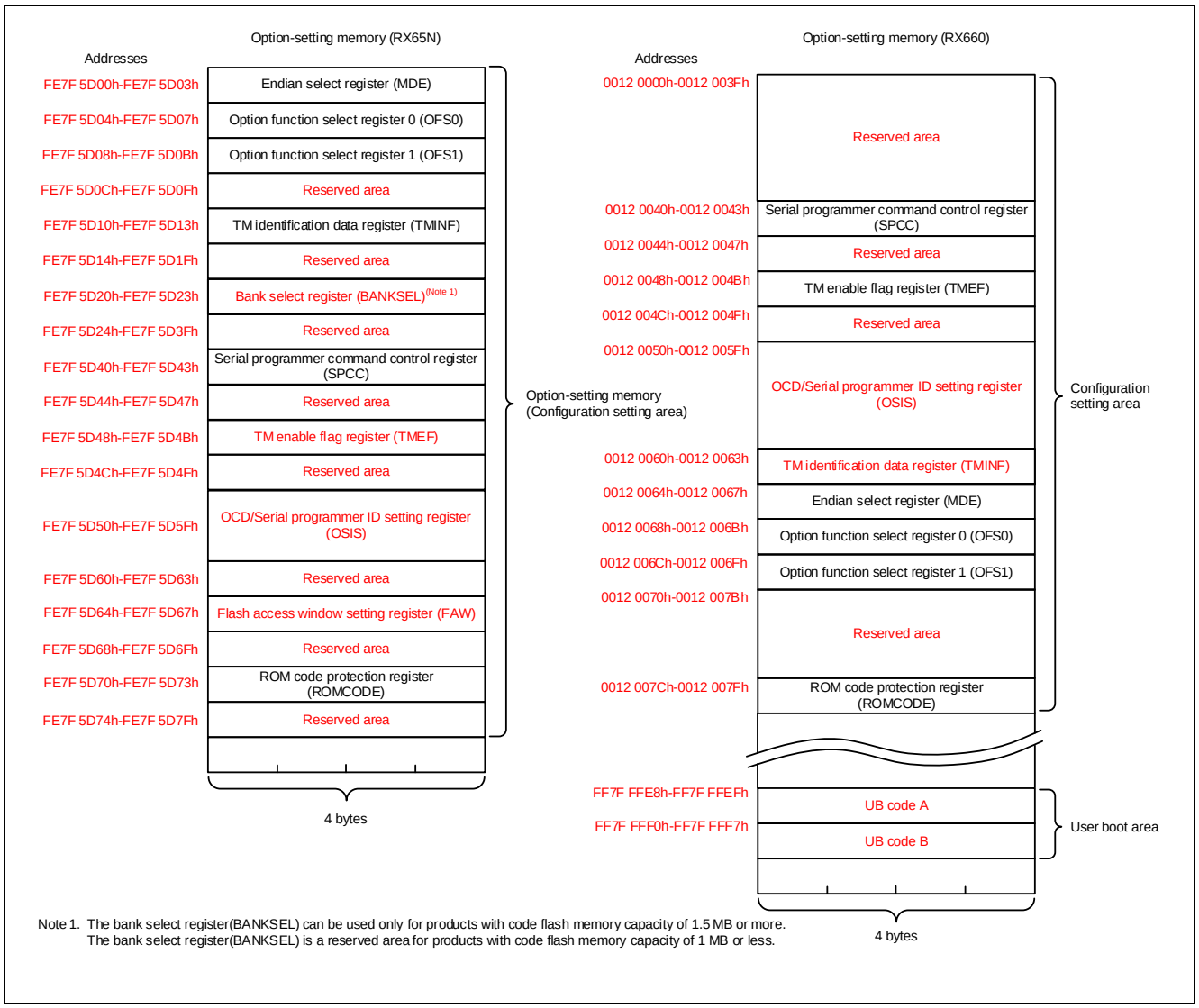

Figure 2.4 Comparison of Option-Setting Memory Areas

Table 2.4 Comparison of Option-Setting Memory Registers

Register	Bit	RX65N (OFSM)	RX660 (OFSM)
SPCC	OCDE	—	On-chip debugger connection enable bit
	IDE	—	ID code protection enable bit
	SEPR	—	Block erasure command protect bit
	WRPR	—	Programming command protect bit
	RDPR	—	Read command protect bit
OFS1	VDSEL	Voltage detection 0 level select bit b1 b0 0 0: Reserved 0 1: 2.94 V is selected. 1 0: 2.87 V is selected. 1 1: 2.80 V is selected.	Voltage detection 0 level select bit b1 b0 0 0: Reserved 0 1: Reserved 1 0: 2.83 V is selected. 1 1: 4.22 V is selected.
MDE	BANKMD[2:0]	Bank mode select bit	—
TMEF	TMEFDB[2:0]	Dual bank TM enable bit(Note 1)	—
BANKSEL	—	Bank select register	—
FAW	—	Flash access window setting register	—

Note 1. These bits are reserved for products with code flash memory of 1 MB or less. When read, these bits return the written value. The write value should be 111b.

2.5 Voltage Detection Circuit

Table 2.5 is a Comparative Overview of Voltage Detection Circuits, and Table 2.6 is a Comparison of Voltage Detection Circuit Registers.

Table 2.5 Comparative Overview of Voltage Detection Circuits

Item		RX65N (LVDA)			RX660 (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
VCC monitoring	Monitored voltage	Vdet0	Vdet1	Vdet2	Vdet0	Vdet1	Vdet2
	Detection target	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2	When voltage drops below Vdet0	When voltage rises above or drops past Vdet1	When voltage rises above or drops past Vdet2
	Detection voltage	Selectable from 3 levels using OFS1.VDSEL [1:0] bits.	Selectable from 3 levels using LVDLVLR.LVD1 LVL[3:0] bits	Selectable from 3 levels using LVDLVLR.LVD2 LVL[3:0] bits	Selectable from 2 levels using OFS1.VDSEL [1:0] bits.	Selectable from 5 levels using LVDLVLR.LVD1 LVL[3:0] bits	Selectable from 5 levels using LVDLVLR.LVD2 LVL[3:0] bits
	Monitoring flags	—	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2	—	LVD1SR. LVD1MON flag: Monitors whether voltage is higher or lower than Vdet1	LVD2SR. LVD2MON flag: Monitors whether voltage is higher or lower than Vdet2
			LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection		LVD1SR. LVD1DET flag: Vdet1 passage detection	LVD2SR. LVD2DET flag: Vdet2 passage detection

Item		RX65N (LVDA)			RX660 (LVDA)		
		Voltage Monitoring 0	**Voltage Monitoring 1**	**Voltage Monitoring 2**	**Voltage Monitoring 0**	**Voltage Monitoring 1**	**Voltage Monitoring 2**
Voltage detection processing	Reset	Voltage Monitoring 0 Reset	Voltage Monitoring 1 reset	Voltage Monitoring 2 reset	Voltage Monitoring 0 Reset	Voltage Monitoring 1 reset	Voltage Monitoring 2 reset
		Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet2 or Vdet2 > VCC	Reset when Vdet0 > VCC: CPU restart timing after specified time with VCC > Vdet0	Reset when Vdet1 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet1 or Vdet1 > VCC	Reset when Vdet2 > VCC: CPU restart timing selectable between after specified time with VCC > Vdet2 or Vdet2 > VCC
	Interrupts	—	Voltage Monitoring 1 interrupt	Voltage Monitoring 2 interrupt	—	Voltage Monitoring 1 interrupt	Voltage Monitoring 2 interrupt
			Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt		Selectable between non-maskable or maskable interrupt	Selectable between non-maskable or maskable interrupt
			Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC, VCC > Vdet2, or both		Interrupt request issued when Vdet1 > VCC, VCC > Vdet1, or both	Interrupt request issued when Vdet2 > VCC, VCC > Vdet2, or both
Digital filter	Enable/ disable switching	No digital filter function	Available:	Available:	No digital filter function	Available:	Available:
	Sampling time	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	—	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)	1/n LOCO frequency × 2 (n: 2, 4, 8, 16)
Event link function		—	Available: Event output at Vdet passage detection	Available: Event output at Vdet passage detection	—	Available: Event output at Vdet1 passage detection	Available: Event output at Vdet2 passage detection

Table 2.6 Comparison of Voltage Detection Circuit Registers

Register	Bit	RX65N (LVDA)	RX660 (LVDA)
LVDLVLR	LVD1LVL[3:0]	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 1 0 0 1: 2.99 V (Vdet1_1) 1 0 1 0: 2.92 V (Vdet1_2) 1 0 1 1: 2.85 V (Vdet1_3) Settings other than the above are prohibited.	Voltage detection 1 level select bits (Standard voltage during drop in voltage) b3 b0 0 1 0 0: 4.57 V (Vdet1_0) 0 1 0 1: 4.47 V (Vdet1_1) 0 1 1 0: 4.32 V (Vdet1_2) 1 0 1 0: 2.93 V (Vdet1_3) 1 0 1 1: 2.88 V (Vdet1_4) Settings other than the above are prohibited.
	LVD2LVL[3:0]	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 1 0 0 1: 2.99 V (Vdet2_1) 1 0 1 0: 2.92 V (Vdet2_2) 1 0 1 1: 2.85 V (Vdet2_3) Settings other than the above are prohibited.	Voltage detection 2 level select bits (Standard voltage during drop in voltage) b7 b4 0 1 0 0: 4.57 V (Vdet2_0) 0 1 0 1: 4.47 V (Vdet2_1) 0 1 1 0: 4.32 V (Vdet2_2) 1 0 1 0: 2.93 V (Vdet2_3) 1 0 1 1: 2.88 V (Vdet2_4) Settings other than the above are prohibited.

2.6 Clock Generation Circuit

Table 2.7 is a Comparative Overview of Clock Generation Circuits, and Table 2.8 is a Comparison of Clock Generation Circuit Registers.

Table 2.7 Comparative Overview of Clock Generation Circuits

Item	RX65N	RX660
Use	• Generates the system clock (ICLK) to be supplied to the CPU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the ETHERC, EDMAC, RSPI, SCIi, MTU3, AES, GLCDC, and DRW2D • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module clock (for analog conversion) (PCLKC: unit 0, PCLKD: unit 1) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the external bus clock (SDCLK) to be supplied to the SDRAM • Generates the USB clock (UCLK) to be supplied to the USBb. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CAN clock (CANMCLK) to be supplied to the CAN. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the RTC main clock (RTCMCLK) to be supplied to the RTC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT. • Generates the JTAG clock (JTAGTCK) to be supplied to the JTAG.	• Generates the system clock (ICLK) to be supplied to the CPU, TFU, DMAC, DTC, code flash memory, and RAM. • Generates the peripheral module clock (PCLKA) to be supplied to the RSPI, SCIm, RSCI, MTU, and CANFD. • Generates the peripheral module clock (PCLKB) supplied to the peripheral modules. • Generates the peripheral module clock (for analog conversion) (PCLKD) to be supplied to the S12AD. • Generates the FlashIF clock (FCLK) to be supplied to the FlashIF. • Generates the external bus clock (BCLK) to be supplied to the external bus. • Generates the CAC clock (CACCLK) to be supplied to the CAC. • Generates the CANFD clock (CANFDCLK) to be supplied to the CANFD. • Generates the CANFD main clock (CANFDMCLK) to be supplied to the CANFD. • Generates the RTC sub-clock (RTCSCLK) to be supplied to the RTC. • Generates the REMC sub-clock (REMSCLK) to be supplied to the REMC. • Generates the IWDT-dedicated clock (IWDTCLK) to be supplied to the IWDT.

Item	RX65N	RX660
Operating frequency	• ICLK: 120 MHz (max) • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKC: 60 MHz (max) • PCLKD: 60 MHz (max) • FCLK: — 4 MHz to 60 MHz (during programming or erasing of code flash memory and data flash memory) — 60 MHz (max) (during reading of data flash memory) • BCLK: 120 MHz (max) • BCLK pin output: 60 MHz (max.) • SDCLK pin output: 60 MHz (max.) • UCLK: 48 MHz (max) • CACCLK: Same as clock from respective oscillators • CANMCLK: 24 MHz (max) • RTCSCLK: 32.768 kHz • RTCMCLK: 8 MHz to 16 MHz • IWDTCLK: 120 kHz • JTAGTCK: 10 MHz (max)	• ICLK: 120 MHz (max) • PCLKA: 120 MHz (max) • PCLKB: 60 MHz (max) • PCLKD: 8 MHz to 60 MHz (when 12-bit A/D converter is operating) • FCLK: — 4 MHz to 60 MHz (during programming or erasing of code flash memory or data flash memory) — 60 MHz (max) (for reading from the data flash) • BCLK: 60 MHz (max) • BCLK pin output: 40 MHz (max.) • CACCLK:Same as clock from respective oscillators • CANFDCLK: 60 MHz (max) • CANFDMCLK: 24 MHz (max) • RTCSCLK: 32.768 kHz • REMCLK: 32.768 kH • IWDTCLK: 120 kHz
Main clock oscillator	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU3 pin can be forcedly driven to high-impedance.	• Resonator frequency: 8 MHz to 24 MHz • External clock input frequency: 24 MHz (max) • Connectable resonator or additional circuit: Ceramic resonator, crystal • Connection pins: EXTAL and XTAL • Oscillation stop detection function: When a main clock oscillation stop is detected, the system clock source is switched to LOCO and MTU pin can be forcedly driven to high-impedance.
Sub-clock oscillator	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN and XCOUT	• Resonator frequency: 32.768 kHz • Connectable resonator or additional circuit: Crystal • Connection pins: XCIN and XCOUT

Item	RX65N	RX660
PLL frequency synthesizer	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Oscillation frequency: 120 MHz to 240 MHz	• Input clock source: Main clock, HOCO • Input pulse frequency division ratio: Selectable from 1, 2, and 3 • Input frequency: 8 MHz to 24 MHz • Frequency multiplication ratio: Selectable from 10 to 30 • Output clock frequency of PLL frequency synthesizer: 120 MHz to 240 MHz
High-speed on-chip oscillator (HOCO)	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control	• Oscillation frequency: Selectable from 16 MHz, 18 MHz, and 20 MHz • HOCO power supply control • FLL function (Not available on products without a sub-clock oscillator.)
Low-speed on-chip oscillator (LOCO)	Oscillation frequency: 240 kHz	Oscillation frequency: 240 kHz
IWDT-dedicated on-chip oscillator	Oscillation frequency: 120 kHz	Oscillation frequency: 120 kHz
JTAG external clock input (TCK)	Input clock frequency: 10 MHz (max)	—
BCLK pin output control function	• Selectable between BCLK clock output or high-level output. • Output clock selectable between BCLK or BCLK/2.	• Selectable between BCLK clock output or high-level output. • Output clock selectable between BCLK or BCLK/2.
SDCLK pin output control function	• Selectable between SDCLK clock output or high-level output.	—
Event link function (output)	Detection of stopping of the main clock oscillator	Detection of stopping of the main clock oscillator
Event link function (input)	Switching of the clock source to the low-speed on-chip oscillator	Switching of the clock source to the low-speed on-chip oscillator

Table 2.8 Comparison of Clock Generation Circuit Registers

Register	Bit	RX65N	RX660
SCKCR	PCKC[3:0]	Peripheral module clock (PCLKC) select bit b7 b4 0 0 0 0: x1/1 0 0 0 1: x1/2 0 0 1 0: x1/4 0 0 1 1: x1/8 0 0 0 0: x1/16 0 1 0 1: x1/32 0 1 1 0: x1/64 Settings other than the above are prohibited.	The PCLKC is not implemented on this MCU. These bits should be set to 0001b.
	PSTOP0	SDCLK pin output control bit	—
ROMWT	—	ROM wait cycle setting register	—
SCKCR2	UCK[3:0]	USB clock (UCLK) select bit	—
	CFDCK[3:0]	—	CANFD clock (CANFDCLK) select bit
SOSCCR	SOSTP	Sub-clock oscillator stop bit	Sub-clock oscillator stop bit This bit is not initialized by reset sources other than a power-on reset.
		Initial value after a reset differs.	
FLLCR1	—	—	FLL control register 1
FLLCR2	—	—	FLL control register 2
SOFCR	—	—	Sub-clock oscillator forced oscillation control register
MOFCR	MOFXIN	Main clock oscillator forced oscillation bit	—

2.7 Low Power Consumption

Table 2.9 is Comparative Overview of Low Power Consumption Functions, Table 2.10 is Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode, and Table 2.11 is Comparison of Low Power Consumption Registers.

Table 2.9 Comparative Overview of Low Power Consumption Functions

Item	RX65N	RX660
Reducing power consumption by switching clock signals	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, PCLKC, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).	The frequency division ratio can be set independently for the system clock (ICLK), peripheral module clocks (PCLKA, PCLKB, and PCLKD), external bus clock (BCLK), and flash interface clock (FCLK).
BCLK output control function	Selectable from BCLK output and high-level output	Selectable from BCLK output and high-level output
SDCLK output control function	Selectable from SDCLK output and high-level output	—
Module stop function	Each peripheral module can be stopped independently by the module stop control register.	Each peripheral module can be stopped independently by the module stop control register.
Function for transition to low power consumption mode	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.	Transition to a low power consumption mode in which the CPU, peripheral modules, or oscillators are stopped is enabled.
Low power consumption modes	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode	• Sleep mode • All-module clock stop mode • Software standby mode • Deep software standby mode
Function for lower operating power consumption	• Power consumption can be reduced in normal operation, sleep mode, and all-module clock stop mode by selecting an appropriate operating power control mode according to the operating frequency and operating voltage. • Three operating power control modes are available — High-speed operating mode — Low-speed operating mode 1 — Low-speed operating mode 2 When the same conditions (frequency and voltage) are set, there is no difference in power consumption between low-speed operating modes1 and 2.	—

Table 2.10 Comparison of Procedures for Entering and Exiting Low Power Consumption Modes and Operating States in Each Mode

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX65N	RX660
Sleep mode	Transition method	Control register + instruction	Control register + instruction
	Method of release other than reset	Interrupts	Interrupts
	State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM, Extended RAM (RX65N)	Operation possible (retained)	Operation possible (retained)
	Standby RAM	Operation possible (retained)	—
	Flash memory	Operation	Operation
	USBFS host or function module (USBb)	Operation possible	—
	Watchdog timer (WDTA, WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVDA, LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Operation possible	Operation possible
	I/O ports	Operation	Operation
All-module clock stop mode	Transition method	Control register + instruction	Control register + instruction
	Method of release other than reset	Interrupts	Interrupts
	State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Operation possible
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Operation possible	Operation possible
	Low-speed on-chip oscillator	Operation possible	Operation possible
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Operation possible	Operation possible
	CPU	Stopped (retained)	Stopped (retained)
	RAM, Extended RAM (RX65N)	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	—
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS host or function module (USBb)	Stopped	—

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX65N	RX660
All-module clock stop mode	Watchdog timer (WDTA, WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	Operation possible	Operation possible
	Remote control signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0, unit1) (TMR)	Operation possible	Operation possible
	Voltage detection circuit (LVDA, LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of release other than reset	Interrupts	Interrupts
	State after release	Program execution state (interrupt processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Operation possible	Operation possible
	PLL	Stopped	Stopped
	CPU	Stopped (retained)	Stopped (retained)
	RAM, Extended RAM (RX65N)	Stopped (retained)	Stopped (retained)
	Standby RAM	Stopped (retained)	—
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS host or function module (USBb)	Stopped	—
	Watchdog timer (WDT)	Stopped (retained)	Stopped (retained)
	Independent watchdog timer (IWDT)	Operation possible	Operation possible
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	Stopped (retained)	Stopped (retained)
	Remote control signal receiver (REMC)	—	Operation possible
	8-bit timer (unit 0 and unit1) (TMR)	Stopped (retained)	Stopped (retained)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (retained)	Stopped (retained)
	I/O ports	Retained	Retained
Deep software standby mode	Transition method	Control register + instruction	Control register + instruction
	Method of release other than reset	Interrupts	Interrupts
	State after release	Program execution state (reset processing)	Program execution state (interrupt processing)
	Main clock oscillator	Operation possible	Stopped
	Sub-clock oscillator	Operation possible	Operation possible
	High-speed on-chip oscillator	Stopped	Stopped
	Low-speed on-chip oscillator	Stopped	Stopped
	IWDT-dedicated on-chip oscillator	Stopped (undefined)	Stopped (undefined)

Mode	Entering and Exiting Low Power Consumption Modes and Operating States	RX65N	RX660
Deep software standby mode	PLL	Stopped	Stopped
	CPU	Stopped (undefined)	Stopped (undefined)
	RAM, Extended RAM (RX65N)	Stopped (undefined)	Stopped (undefined)
	Standby RAM	Stopped (retained/undefined)	—
	Flash memory	Stopped (retained)	Stopped (retained)
	USBFS host or function module (USBb)	Stopped (retained/undefined)	—
	Watchdog timer (WDT)	Stopped (undefined)	Stopped (undefined)
	Independent watchdog timer (IWDT)	Stopped (undefined)	Stopped (undefined)
	Realtime clock (RTC)	Operation possible	Operation possible
	Port output enable (POE)	Stopped (undefined)	Stopped (undefined)
	Remote control signal receiver (REMC)	—	Stopped (undefined)
	8-bit timer (unit 0 and unit1) (TMR)	Stopped (undefined)	Stopped (undefined)
	Voltage detection circuit (LVD)	Operation possible	Operation possible
	Power-on reset circuit	Operation	Operation
	Peripheral modules	Stopped (undefined)	Stopped (undefined)
	I/O ports	Retained	Retained

“Operation possible” means that whether the state is operating or stopped is controlled by the control register setting.

“Stopped (retained)” means that internal register values are retained and internal operations are suspended.

“Stopped (undefined)” means that internal register values are undefined and power is not supplied to the internal circuit.

Table 2.11 Comparison of Low Power Consumption Registers

Register	Bit	RX65N	RX660
MSTPCRA	MSTPA10	Programmable pulse generator (unit 1) module stop bit	—
	MSTPA11	Programmable pulse generator (unit 0) module stop bit	—
	MSTPA13	16-bit timer pulse unit 0 (unit 0) module stop bit	—
	MSTPA16	12-bit A/D converter (unit 1) module stop bit	—
	MSTPA29	EXDMA controller module stop bit	Module stop A29 bit
MSTPCRB	MSTPB0	CAN module 0 module stop bit	—
	MSTPB1	CAN module 1 module stop bit	—
	MSTPB8	Temperature sensor module stop bit	—
	MSTPB10	—	Comparator C module stop bit
	MSTPB15	Ethernet controller and Ethernet controller DMA controller (channel 0) modules stop bit	—
	MSTPB16	Serial peripheral interface 1 module stop bit	—
	MSTPB19	Universal serial bus 2.0 FS interface module stop bit	—
	MSTPB20	I^2C bus interface 1 module stop bit	—
	MSTPB22	Parallel data capture unit module stop bit	—
MSTPCRC	MSTPC2	Extended RAM module stop bit	—
	MSTPC7	Standby RAM module stop bit	—
	MSTPC22	Serial peripheral interface 2 module stop bit	—
	MSTPC23	Quad serial peripheral interface module stop bit	—
	MSTPC28	2D drawing engine module stop bit	—
	MSTPC29	Graphic LCD controller module stop bit	—
MSTPCRD	MSTPD0	Module stop D0 setting bit	—
	MSTPD1	Module stop D1 setting bit	—
	MSTPD2	Module stop D2 bit	Serial communications interface 11 module stop bit
	MSTPD3	Module stop D3 bit	Serial communications interface 10 module stop bit
	MSTPD4	Module stop D4 setting bit	—
	MSTPD5	Module stop D5 setting bit	—
	MSTPD6	Module stop D6 setting bit	—
	MSTPD7	Module stop D7 setting bit	Remote control signal receiver module stop bit
	MSTPD10	—	CANFD module stop bit
	MSTPD13	SD slave interface module stop bit	—
	MSTPD19	SD host interface module stop bit	—
	MSTPD21	MMC host interface module stop bit	—
	MSTPD27	Trusted Secure IP module stop bit	—
OPCCR	—	Operating power control register	—

Register	Bit	RX65N	RX660
DPSBYCR	DEEPCUT [1:0]	Deep cut bit	—
DPSIER2	DRIICDIE	SDA2-DS deep-standby release signal enable bit	—
	DRIICCIE	SCL2-DS deep-standby release signal enable bit	—
	DUSBIE	USB suspend/resume deep-standby release signal enable bit	—
DPSIER3	—	Deep standby interrupt enable register 3	—
DPSIFR2	DRIICDIF	SDA2-DS deep-standby release flag	—
	DRIICCIF	SCL2-DS deep-standby release flag	—
	DUSBIF	USB suspend/resume deep-standby release flag	—
DPSIFR3	—	Deep standby interrupt flag register 3	—
DPSIEGR2	DRIICDEG	SDA2-DS edge select bit	—
	DRIICCEG	SCL2-DS edge select bit	—
DPSIEGR3	—	Deep standby interrupt edge register 3	—

2.8 Register Write Protection Function

Table 2.12 is a Comparative Overview of Register Write Protection Functions.

Table 2.12 Comparative Overview of Register Write Protection Functions

Item	RX65N	RX660
PRC0 bit	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, OSTDCR, OSTDSR	• Registers related to the clock generation circuit: SCKCR, SCKCR2, SCKCR3, PLLCR, PLLCR2, BCKCR, MOSCCR, SOSCCR, LOCOCR, ILOCOCR, HOCOCR, HOCOCR2, FLLCR1, FLLCR2, OSTDCR, OSTDSR
PRC1 bit	• Registers related to the operating modes: SYSCR0, SYSCR1, • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, OPCCR, RSTCKCR, DPSBYCR, DPSIER0 to 3, DPSIFR0 to 3, DPSIEGR0 to 3 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, HOCOPCR • Software reset register: SWRR	• Registers related to the operating modes: SYSCR0, SYSCR1, VOLSR • Registers related to the low power consumption functions: SBYCR, MSTPCRA, MSTPCRB, MSTPCRC, MSTPCRD, RSTCKCR, DPSBYCR, DPSIER0 to 2, DPSIFR0 to 2, DPSIEGR0 to 2 • Registers related to the clock generation circuit: MOSCWTCR, SOSCWTCR, MOFCR, SOFCR, HOCOPCR • Software reset register: SWRR
PRC3 bit	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR	• Registers related to LVD: LVCMPCR, LVDLVLR, LVD1CR0, LVD1CR1, LVD1SR, LVD2CR0, LVD2CR1, LVD2SR

2.9 Interrupt Controller

Table 2.13 is a Comparative Overview of Interrupt Controllers, and Table 2.14 is a Comparison of Interrupt Controller Registers.

Table 2.13 Comparative Overview of Interrupt Controllers

Item		RX65N (ICUB)	RX660 (ICUF)
Interrupts	Peripheral function interrupts	Interrupts from peripheral modules • Interrupt detection method: Edge detection or level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.	Interrupts from peripheral modules • Interrupt detection method: Edge detection or level detection (fixed for each interrupt source) • Group interrupt: Multiple interrupt sources are grouped together and treated as a single interrupt source. — Group IE0 interrupt: Interrupt sources of coprocessors that use CLK as the operating clock (edge detection) — Group BE0 interrupt: Interrupt sources of peripheral modules that use PCLKB as the operating clock (edge detection) — Group BL0/BL1/BL2 interrupt: PCLKB as the operating clock Interrupt sources of peripheral modules (level detection) — Group AL0/AL1 interrupt: Interrupt sources of peripheral modules that use PCLKA as the operating clock (level detection) • Software configurable interrupt B: Any of the interrupt sources for peripheral modules that use PCLKB as the operating clock can be assigned to interrupt vector numbers 128 to 207. • Software configurable interrupt A: Any of the interrupt sources for peripheral modules that use PCLKA as the operating clock can be assigned to interrupt vector numbers 208 to 255.

Item		RX65N (ICUB)	RX660 (ICUF)
Interrupts	External pin interrupts	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • A digital filter can be used to remove noise.	Interrupts by input signals on IRQi pins (i = 0 to 15) • Interrupt detection: Detection of low level, falling edge, rising edge, or rising and falling edges can be set for each detection source. • A digital filter can be used to remove noise.
	Software interrupts	• An interrupt request can be generated by writing to a register. • Number of sources: 2	• An interrupt request can be generated by writing to a register. • Number of sources: 2
	Interrupt priority level	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).	The priority level is set with the interrupt source priority register r (IPRr) (r = 000 to 255).
	Fast interrupt function	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.	It is possible to reduce the CPU's interrupt response time. This setting can be used for one interrupt source only.
	DTC and DMAC control	The DTC and DMAC can be activated by an interrupt source.	The DTC and DMAC can be activated by an interrupt source.
	EXDMAC control	• Software configurable interrupt B source select register 144 or software configurable interrupt A source select register • Interrupt selected by 208 can be used to start EXDMAC0. • Software configurable interrupt B source select register 145 or software configurable interrupt A source select register • Interrupt selected by 209 can be used to start EXDMAC1.	—
Non-maskable interrupts	NMI pin interrupt	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • A digital filter can be used to remove noise.	Interrupt by the input signal on the NMI pin • Interrupt detection: Falling edge or rising edge • A digital filter can be used to remove noise.
	Oscillation stop detection Interrupts	Interrupt at detection of main clock oscillation stop	Interrupt at detection of main clock oscillation stop
	WDT underflow/ refresh error interrupt	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the watchdog timer underflows or a refresh error occurs.
	IWDT underflow/ refresh error interrupt	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.	Interrupt occurs when the independent watchdog timer underflows or a refresh error occurs.
	Voltage monitoring 1 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 1 (LVD1) Interrupts	Interrupt from voltage detection circuit 1 (LVD1)

Item		RX65N (ICUB)	RX660 (ICUF)
Non-maskable interrupts	Voltage monitoring 2 interrupt	Voltage monitoring interrupt of voltage monitoring circuit 2 (LVD2) Interrupts	Interrupt from voltage detection circuit 2 (LVD2)
	RAM error interrupt	Interrupt occurs when a parity check error is detected in the RAM (including the extended RAM).	Interrupt occurs when a parity check error is detected in the RAM.
Return from low power consumption state	Sleep mode	Exit sleep mode by any interrupt source.	Exit sleep mode by any interrupt source.
	All-module clock stop mode	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, USB resume, RTC alarm, RTC period, IWDT, or software configurable interrupt 146 to 157).	Exit all-module clock stop mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, oscillation stop detection interrupt, RTC alarm, RTC period, IWDT, REMC interrupt, or software configurable interrupt 146 to 157).
	Software standby mode	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, RTC period, or IWDT).	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, RTC period, IWDT, or REMC interrupt).
	Deep software standby mode	Exit software standby mode by NMI pin interrupt, external pin interrupt, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, USB resume, RTC alarm, or RTC period).	Exit deep software standby mode by NMI pin interrupt, any among a subset of external pin interrupts, or peripheral interrupt (voltage monitoring 1, voltage monitoring 2, RTC alarm, or RTC period).

Table 2.14 Comparison of Interrupt Controller Registers

Register	Bit	RX65N (ICUB)	RX660 (ICUF)
GRPBE0	—	Group BE0 interrupt request register	—
GRPAL1	—	Group AL1 interrupt request register	
GENBE0	—	Group BE0 interrupt request enable register	—
GENAL1	—	Group AL1 interrupt request enable register	
GCRBE0	—	Group BE0 interrupt clear register	—
PIBRk	—	Software configurable interrupt B request register k (k = 0h to Bh)	Software configurable interrupt B request register k (k = 0h, 1h, 5h, 6h, 8h to Ah, Ch, Dh)
PIARk	—	Software configurable interrupt A request register k (k = 0h to 5h, Bh)	Software configurable interrupt A request register k (k = 0h to 5h, Bh, Ch)
SELEXDR	—	EXDMAC start interrupt select register	—

2.10 Buses

Table 2.15 is a Comparative Overview of Buses, and Table 2.16 is a Comparison of Bus Registers.

Table 2.15 Comparative Overview of Buses

Item		RX65N	RX660
CPU buses	Instruction bus	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, extended RAM, or code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for instructions) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
	Operand bus	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, extended RAM, or code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the CPU (for operands) • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Memory buses	Memory bus 1	Connected to RAM	Connected to RAM
	Memory bus 2	Connected to ROM	Connected to code flash memory
	Memory bus 3	Connected to extended RAM	—
Internal main buses	Internal main bus 1	• Connected to CPU • Operates in synchronization with the system clock (ICLK)	• Connected to CPU • Operates in synchronization with the system clock (ICLK)
	Internal main bus 2	• Connected to DTC, DMAC, and extended bus master • Connected to on-chip memory (RAM, extended RAM, or code flash memory) • Operates in synchronization with the system clock (ICLK)	• Connected to the DTC and DMAC • Connected to on-chip memory (RAM, code flash memory) • Operates in synchronization with the system clock (ICLK)
Internal peripheral buses	Internal peripheral bus 1	• Connected to peripheral modules (DTC, DMAC, EXDMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK) (EXDMAC operates in synchronization with BCLK)	• Connected to peripheral modules (TFU, DTC, DMAC, interrupt controller, and bus error monitoring section) • Operates in synchronization with the system clock (ICLK)
	Internal peripheral bus 2	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (peripheral functions other than those connected to internal peripheral buses 1, 3, 4, and 5) • Operates in synchronization with the peripheral-module clock (PCLKB)

Item		RX65N	RX660
Internal peripheral buses	Internal peripheral bus 3	• Connected to peripheral modules (USBb, PDC, and standby RAM) • Operates in synchronization with the peripheral-module clock (PCLKB)	• Connected to peripheral modules (DOC, REMC, CANFD, CMPC) • Operates in synchronization with the peripheral-module clock (PCLKB)
	Internal peripheral bus 4	• Connected to peripheral modules (EDMAC, ETHERC, MTU3, SCIi, RSPI, and AES(Note 2)) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (MTU, RSPI, SCIi) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 5	• Connected to peripheral modules (GLCDC and DRW2D)(Note 1) • Operates in synchronization with the peripheral-module clock (PCLKA)	• Connected to peripheral modules (RSCI, CANFD) • Operates in synchronization with the peripheral-module clock (PCLKA)
	Internal peripheral bus 6	• Connected to code flash memory (in P/E) and data flash memory(Note 1) • Operates in synchronization with the FlashIF clock (FCLK)	• Connected to code flash memory (in P/E) and data flash • Operates in synchronization with the FlashIF clock (FCLK)
External bus	CS area	• Connected to an external device • Operates in synchronization with the external bus clock (BCLK)	• Connected to an external device • Operates in synchronization with the external bus clock (BCLK)
	SDRAM area	• Connected to SDRAM • Operates in synchronization with the SDRAM clock (SDCLK)	—

Note 1. Only available for products with code flash memory capacity of 1.5 MB or more.
Note 2. Only available for products with code flash memory capacity of 1 MB or less.

Table 2.16 Comparison of Bus Registers

Register	Bit	RX65N	RX660
CSnREC	—	Software interrupt 2 generation register (n = 0 to 7)	Software interrupt 2 generation register (n = 0 to 3)
CSnMOD	—	CSn mode register (n = 0 to 7)	CSn mode register (n = 0 to 3)
CSnWCR1	—	CSn wait control register 1 (n = 0 to 7)	CSn wait control register 1 (n = 0 to 3)
CSnWCR2	—	CSn wait control register 2 (n = 0 to 7)	CSn wait control register 2 (n = 0 to 3)
SDCCR	—	SDC control register	—
SDCMOD	—	SDC mode register	—
SDAMOD	—	SDRAM access mode register	—
SDSELF	—	SDRAM self-refreshing control register	—
SDRFCR	—	SDRAM refreshing control register	—

Register	Bit	RX65N	RX660
SDRFEN	—	SDRAM auto-refresh control register	—
SDICR	—	SDRAM initialization sequence control register	—
SDIR	—	SDRAM initialization register	—
SDADR	—	SDRAM address register	—
SDTR	—	SDRAM timing register	—
SDMOD	—	SDRAM mode register	—
SDSR	—	SDRAM status register	—
BERSR1	MST[2:0]	Bus master code bits b6 b4 0 0: CPU 0 0: Reserved 0 1: Reserved 0 1: DTC/DMAC 1 0: Reserved 1 0: Reserved 1 1: Extended bus master 1 1: EXDMAC	Bus master code bits b6 b4 0 0: CPU 0 0: Reserved 0 1: Reserved 0 1: DTC/DMAC 1 0: Reserved 1 0: Reserved 1 1: Reserved 1 1: Reserved
BUSPRI	BPRA[1:0]	Memory bus 1, 3 (RAM/extended RAM) priority control bits	Memory bus 1 (RAM) priority control bits
EBMAPCR	—	Extended bus master priority control register	—

2.11 Event Link Controller

Table 2.17 is Comparative Overview of Event Link Controllers, Table 2.18 is Comparison of Event Link Controller Registers, Table 2.19 is Correspondence between ELSRn Registers and Peripheral Modules, and Table 2.20 is Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers.

Table 2.17 Comparative Overview of Event Link Controllers

Item	RX65N (ELC)	RX660 (ELC)
Event link function	• 82 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event input is selectable. • Event link operation is possible for port B and port E. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.	• 83 types of event signals can be directly connected to peripheral modules. • The operation of peripheral timer modules at event input is selectable. • Event link operation is possible for port B and port E. — Single port: Event link operation can be enabled for a single specified port. — Port group: Event link operation can be enabled for multiple specified ports within a group of up to eight ports.
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Table 2.18 Comparison of Event Link Controller Registers

Register	Bit	RX65N (ELC)	RX660 (ELC)
ELSRn	—	Event link setting register n (n=0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 33, 35 to 38, or 45) 00h: Event signal output to the corresponding peripheral module is disabled. 01h to BDh: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.	Event link setting register n (n=0, 3, 4, 7, 10 to 13, 15, 16, 18 to 28, 30, 31, 32, or 56) 00h: Event signal output to the corresponding peripheral module is disabled. 01h to F1h: Specifies the number of the event signal to be linked. Settings other than the above are prohibited.
ELOPE	—	—	Event link option setting register E
ELOPF	—	Event link option setting register F	—
ELOPH	—	Event link option setting register H	—

Table 2.19 Correspondence between ELSRn Registers and Peripheral Modules

Register	RX65N (ELC)	RX660 (ELC)
ELSR0	MTU0	MTU0
ELSR3	MTU3	MTU3
ELSR4	MTU4	MTU4
ELSR7	CMT1	CMT1
ELSR10	TMR0	TMR0
ELSR11	TMR1	TMR1
ELSR12	TMR2	TMR2
ELSR13	TMR3	TMR3
ELSR15	S12AD	S12AD (ELCTRG00N)
ELSR16	DA0	DA0
ELSR18	ICU (interrupt 1)	ICU (interrupt 1)
ELSR19	ICU (interrupt 2)	ICU (interrupt 2)
ELSR20	Output port group 1	Output port group 1
ELSR21	Output port group 2	Output port group 2
ELSR22	Input port group 1	Input port group 1
ELSR23	Input port group 2	Input port group 2
ELSR24	Single port 0	Single port 0
ELSR25	Single port 1	Single port 1
ELSR26	Single port 2	Single port 2
ELSR27	Single port 3	Single port 3
ELSR28	Clock source switching to LOCO	Clock source switching to LOCO
ELSR30	—	MTU6
ELSR31	—	MTU7
ELSR32	—	MTU8
ELSR33	CMTW0	—
ELSR35	TPU0	—
ELSR36	TPU1	—
ELSR37	TPU2	—
ELSR38	TPU3	—
ELSR45	S12AD1	—
ELSR56	—	S12AD (ELCTRG01N)

Table 2.20 Correspondence between Values Set in ELSRn.ELS[7:0] Bits and Event Signal Names and Numbers

ELS[7:0] Value of Bits	Peripheral modules (RX65N)	RX65N (ELC)	Peripheral modules (RX660)	RX660 (ELC)
01h	Multi-function timer pulse unit 3	MTU0 compare match 0A	Multi-function timer pulse unit 3	MTU0 compare match 0A
02h		MTU0 compare match 0B		MTU0 compare match 0B
03h		MTU0 compare match 0C		MTU0 compare match 0C
04h		MTU0 compare match 0D		MTU0 compare match 0D
05h		MTU0 compare match 0E		MTU0 compare match 0E
06h		MTU0 compare match 0F		MTU0 compare match 0F
07h		MTU0 overflow		MTU0 overflow
10h		MTU3 compare match 3A		MTU3 compare match 3A
11h		MTU3 compare match 3B		MTU3 compare match 3B
12h		MTU3 compare match 3C		MTU3 compare match 3C
13h		MTU3 compare match 3D		MTU3 compare match 3D
14h		MTU3 overflow		MTU3 overflow
15h		MTU4 compare match 4A		MTU4 compare match 4A
16h		MTU4 compare match 4B		MTU4 compare match 4B
17h		MTU4 compare match 4C		MTU4 compare match 4C
18h		MTU4 compare match 4D		MTU4 compare match 4D
19h		MTU4 overflow		MTU4 overflow
1Ah		MTU4 underflow		MTU4 underflow
1Eh	Compare match timer	CMT1 compare match 1		MTU6 compare match 6A
1Fh	—	—		MTU6 compare match 6B
20h	—	—		MTU6 compare match 6C
21h	—	—		MTU6 compare match 6D
22h	8-bit timer	TMR0 compare match A0		MTU6 overflow
23h		TMR0 compare match B0		MTU7 compare match 7A
24h		TMR0 overflow		MTU7 compare match 7B
25h		TMR1 compare match A1		MTU7 compare match 7C
26h		TMR1 compare match B1		MTU7 compare match 7D
27h		TMR1 overflow		MTU7 overflow
28h		TMR2 compare match A2		MTU7 underflow
29h		TMR2 compare match B2		MTU8 compare match 8A
2Ah		TMR2 overflow		MTU8 compare match 8B
2Bh		TMR3 compare match A3		MTU8 compare match 8C
2Ch		TMR3 compare match B3		MTU8 compare match 8D
2Dh		TMR3 overflow		MTU8 overflow
2Eh	Realtime clock	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)	—	—
31h	Independent watchdog timer	IWDT underflow or refresh error	—	—
37h	—	—	Compare match timer	CMT1 compare match 1
3Ah	Serial communications interface	SCI5 error (receive error or error signal detection)	—	—

ELS[7:0] Value of Bits	Peripheral modules (RX65N)	RX65N (ELC)	Peripheral modules (RX660)	RX660 (ELC)
3Bh	Serial communications interface	SCI5 receive data full	—	—
3Ch		SCI5 transmit data empty	8-bit timer	TMR0 compare match A0
3Dh		SCI5 transmit end		TMR0 compare match B0
3Eh	—	—		TMR0 overflow
3Fh	—	—		TMR1 compare match A1
40h	—	—		TMR1 compare match B1
41h	—	—		TMR1 overflow
42h	—	—		TMR2 compare match A2
43h	—	—		TMR2 compare match B2
44h	—	—		TMR2 overflow
45h	—	—		TMR3 compare match A3
46h	—	—		TMR3 compare match B3
47h	—	—		TMR3 overflow
4Eh	I^2C bus interface	RIIC0 communication error or event generation	—	—
4Fh		RIIC0 receive data full	—	—
50h		RIIC0 transmit data empty	—	—
51h		RIIC0 transmit end	—	—
52h	Serial peripheral interface	RSPI0 error (mode fault, overrun, underrun, or parity error)	—	—
53h		RSPI0 idle	—	—
54h		RSPI0 receive data full	—	—
55h		RSPI0 transmit data empty	—	—
56h		RSPI0 transmit end	—	—
58h	12-bit A/D converter	S12AD A/D conversion end	—	—
5Bh	Voltage Detection Circuit	LVD1 voltage detection	—	—
5Ch		LVD2 voltage detection	—	—
5Dh	DMA controller	DMAC0 transfer end	—	—
5Eh		DMAC1 transfer end	—	—
5Fh		DMAC2 transfer end	—	—
60h		DMAC3 transfer end	—	—
61h	Data transfer controller	DTC transfer end	—	—
62h	Clock Generation Circuit	Oscillation stop detection of the clock generation circuit	—	—
63h	I/O ports	Input edge detection of input port group 1	—	—
64h		Input edge detection of input port group 2	—	—

ELS[7:0] Value of Bits	Peripheral modules (RX65N)	RX65N (ELC)	Peripheral modules (RX660)	RX660 (ELC)
65h	I/O ports	Input edge detection of single input port 0	—	—
66h		Input edge detection of single input port 1	—	—
67h		Input edge detection of single input port 2	—	—
68h		Input edge detection of single input port 3	—	—
69h	Event link controller	Software event	—	—
6Ah	Data Operation Circuit	DOC data operation condition met	—	—
6Ch	12-bit A/D converter	S12AD1 A/D conversion end	—	—
7Eh	Compare match timer W	CMTW channel 0 compare match	—	—
ACh	16-bit timer pulse unit	TPU0 compare match A	Realtime clock	RTC periodic event (select 1/256, 1/128, 1/64, 1/32, 1/16, 1/8, 1/32, 1/16, 1/8, 1/4, 1/2, 1, or 2 seconds)
ADh		TPU0 compare match B	—	—
AEh		TPU0 compare match C	—	—
AFh		TPU0 compare match D	—	—
B0h		TPU0 overflow	—	—
B1h		TPU1 compare match A	—	—
B2h		TPU1 compare match B	—	—
B3h		TPU1 overflow	—	—
B4h		TPU1 underflow	—	—
B5h		TPU2 compare match A	—	—
B6h		TPU2 compare match B	—	—
B7h		TPU2 overflow	—	—
B8h		TPU2 underflow	Serial communications interface	SCI5 error (receive error or error signal detection)
B9h		TPU3 compare match A		SCI5 receive data full
BAh		TPU3 compare match B		SCI5 transmit data empty
BBh		TPU3 compare match C		SCI5 transmit end
BCh		TPU3 compare match D	—	—
BDh		TPU3 overflow	—	—
CCh	—	—	I^2C Bus Interface	RIIC0 communication error or event generation
CDh	—	—		RIIC0 receive data full
CEh	—	—		RIIC0 transmit data empty
CFh	—	—		RIIC0 transmit end

ELS[7:0] Value of Bits	Peripheral modules (RX65N)	RX65N (ELC)	Peripheral modules (RX660)	RX660 (ELC)
D0h	—	—	Serial peripheral interface	RSPI0 error (mode fault, overrun, underrun, or parity error)
D1h	—	—		RSPI0 idle
D2h	—	—		RSPI0 receive buffer full
D3h	—	—		RSPI0 transmit buffer empty
D4h	—	—		RSPI0 transmit end
D6h	—	—	12-bit A/D converter	S12AD A/D conversion end
DCh	—	—	Comparator C	Comparator C0 comparison result change
DDh	—	—		Comparator C1 comparison result change
DEh	—	—		Comparator C2 comparison result change
DFh	—	—		Comparator C3 comparison result change
E2h	—	—	Voltage Detection Circuit	LVD1 voltage detection
E3h	—	—		LVD2 voltage detection
E4h	—	—	DMA controller	DMAC0 transfer end
E5h	—	—		DMAC1 transfer end
E6h	—	—		DMAC2 transfer end
E7h	—	—		DMAC3 transfer end
E8h	—	—	Data transfer controller	DTC transfer end
E9h	—	—	Clock Generation Circuit	Oscillation stop detection of the clock generation circuit
EAh	—	—	I/O ports	Input edge detection of input port group 1
EBh	—	—		Input edge detection of input port group 2
ECh	—	—		Input edge detection of single input port 0
EDh	—	—		Input edge detection of single input port 1
EEh	—	—		Input edge detection of single input port 2
EFh	—	—		Input edge detection of single input port 3
F0h	—	—	Event Link Controller	Software event
F1h	—	—	Data operation circuit	DOC data operation condition met
Settings other than the above are prohibited.				

2.12 I/O Ports

Table 2.21 to Table 2.23 provide comparative overviews of I/O ports, Table 2.24 shows Comparison of I/O Port Functions, and Table 2.26 is Comparison of I/O Port Registers.

Table 2.21 Comparative Overview of I/O Ports (144-Pin)

Port Symbol	RX65N (144-Pin)	RX660 (144-Pin)
PORT0	P00 to P03, P05, P07	P00 to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P56	P50 to P56
PORT6	P60 to P67	P60 to P67
PORT7	P70 to P77	P70 to P77
PORT8	P80 to P83, P86, P87	P80 to P83, P86, P87
PORT9	P90 to P93	P90 to P93
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTF	PF5	PF5 to PF7
PORTG	—	—
PORTH	—	PH0 to PH3, PH6(Note 1), PH7(Note 1)
PORTJ	PJ3, PJ5	PJ1, PJ3 to PJ7
PORTK	—	PK2 to PK5
PORTL	—	PL0, PL1
PORTN	—	PN6, PN7

Note 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.

Table 2.22 Comparative Overview of I/O Ports (100-Pin)

Port Symbol	RX65N (100-Pin)	RX660 (100-Pin)
PORT0	P05, P07	P03(Note 2) to P07
PORT1	P12 to P17	P12 to P17
PORT2	P20 to P27	P20 to P27
PORT3	P30 to P37	P30 to P37
PORT4	P40 to P47	P40 to P47
PORT5	P50 to P55	P50 to P55
PORTA	PA0 to PA7	PA0 to PA7
PORTB	PB0 to PB7	PB0 to PB7
PORTC	PC0 to PC7	PC0 to PC7
PORTD	PD0 to PD7	PD0 to PD7
PORTE	PE0 to PE7	PE0 to PE7
PORTH	—	PH0 to PH3, PH6(Note 2), PH7(Note 1)
PORTJ	PJ3	PJ1, PJ3, PJ6, PJ7
PORTN	—	PN6

Note 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.

Note 2. P03 is not present on products provided with a JTAG.

Table 2.23 Comparative Overview of I/O Ports (64-Pin)

Port Symbol	RX65N (64-Pin)	RX660 (64-Pin)
PORT0	P05(Note 2)	P03, P07
PORT1	P12, P13, P16, P17	P14 to P17
PORT2	P26, P27	P26, P27
PORT3	P30, P31, P34 to P37	P30 to P32, P35 to P37
PORT4	P40 to P43	P40 to P47
PORT5	P53	P54, P55
PORTA	PA1, PA2, PA4, PA6, PA7	PA0, PA1, PA3, PA4, PA6
PORTB	PB5 to PB7	PB0, PB1, PB3, PB5 to PB7
PORTC	PC0, PC1, PC4 to PC7	PC2 to PC7
PORTD	PD2 to PD7	—
PORTE	PE0 to PE2, PE6, PE7	PE0 to PE5
PORTH	—	PH0 to PH3, PH6(Note 1), PH7(Note 1)
PORTJ	—	PJ6, PJ7
PORTN	—	PN6

Note 1. PH6 and PH7 are not present on products provided with a sub-clock oscillator.
Note 2. Not present on 64-pin TFBGA.

Table 2.24 Comparison of I/O Port Functions

Item	Port Symbol	RX65N	RX660
Input pull-up function	PORT0	P00 to P03, P05, P07	P00 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67
	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5 to PF7
	PORTG	PG0 to PG2, PG4 to PG7	—
	PORTH	—	PH0 to PH3, PH6, PH7
	PORTJ	PJ0 to PJ3, PJ5	PJ1, PJ3 to PJ7
	PORTK	—	PK2 to PK5
	PORTL	—	PL0, PL1
	PORTN	—	PN6, PN7
Open drain output function	PORT0	P00 to P03, P05, P07	P00 to P07
	PORT1	P12 to P17	P12 to P17
	PORT2	P20 to P27	P20 to P27
	PORT3	P30 to P34, P36, P37	P30 to P34, P36, P37
	PORT4	P40 to P47	P40 to P47
	PORT5	P50 to P57	P50 to P56
	PORT6	P60 to P67	P60 to P67

Item	Port Symbol	RX65N	RX660
Open drain output function	PORT7	P70 to P77	P70 to P77
	PORT8	P80 to P87	P80 to P83, P86, P87
	PORT9	P90 to P97	P90 to P93
	PORTA	PA0 to PA7	PA0 to PA7
	PORTB	PB0 to PB7	PB0 to PB7
	PORTC	PC0 to PC7	PC0 to PC7
	PORTD	PD0 to PD7	PD0 to PD7
	PORTE	PE0 to PE7	PE0 to PE7
	PORTF	PF0 to PF5	PF5 to PF7
	PORTG	PG0 to PG2, PG4 to PG7	—
	PORTH	—	PH0 to PH3, PH6, PH7
	PORTJ	PJ0 to PJ3, PJ5	PJ1, PJ3 to PJ7
	PORTK	—	PK2 to PK5
	PORTL	—	PL0, PL1
	PORTN	—	PN6, PN7
5 V tolerant	PORT0	P07	—
	PORT1	P11 to P17	P12, P13, P16, P17
	PORT2	P20, P21	—
	PORT3	P30 to P33	—
	PORT6	P67	—
	PORTC	PC0 to PC3	—

Table 2.25 Comparison of Driving Ability Switching on I/O Ports

Port Symbol	Driving Ability Switching	RX65N	RX660
PORT0	Fixed to normal output	—	P03, 05 to P07
	Normal/high	—	P00 to P02, P04
	Normal/high/high for high-speed interface	P00 to P02	—
	Fixed to high drive output	P03, P05, P07	—
PORT1	Normal/high	—	P12 to P17
	Normal/high/high for high-speed interface	P11 to P14	—
	High/high for high-speed interface	P17	—
	Fixed to high drive output	P10, P15, P16	—
PORT2	Normal/high	—	P20 to P27
	Normal/high/high for high-speed interface	P27	—
	High/high for high-speed interface	P20 to P23	—
	Fixed to high drive output	P24 to P26	—
PORT3	Fixed to normal output	P36	P36, P37
	Normal/high	—	P30 to P34
	High/high for high-speed interface	P30, P31	—
	Fixed to high drive output	P32 to P34, P37	—
PORT4	Fixed to normal output	P40 to P47	P40 to P47

Port Symbol	Driving Ability Switching	RX65N	RX660
PORT5	Normal/high	—	P50 to P56
	Normal/high/high for high-speed interface	P50 to P52, P54 to P57	—
	High/high for high-speed interface	P53	—
PORT6	Normal/high	—	P60 to P67
	Fixed to high drive output	P60 to P67	—
PORT7	Normal/high	—	P70 to P77
	Normal/high/high for high-speed interface	P72, P74 to P77	—
	High/high for high-speed interface	P70, P73	—
	Fixed to high drive output	P71	—
PORT8	Normal/high	—	P80 to P83, P86, P87
	Normal/high/high for high-speed interface	P80 to P85	—
	High/high for high-speed interface	P87	—
	Fixed to high drive output	P86	—
PORT9	Normal/high	—	P90 to P93
	Normal/high/high for high-speed interface	P90 to P97	—
PORTA	Normal/high	—	PA0 to PA7
	Normal/high/high for high-speed interface	PA0 to PA7	—
PORTB	Normal/high	—	PB0 to PB7
	Normal/high/high for high-speed interface	PB0 to PB7	—
PORTC	Normal/high	—	PC0 to PC7
	Normal/high/high for high-speed interface	PC0 to PC7	—
PORTD	Normal/high	—	PD0 to PD7
	Normal/high/high for high-speed interface	PD0 to PD7	—
PORTE	Normal/high	—	PE0 to PE7
	Normal/high/high for high-speed interface	PE0 to PE7	—
PORTF	Normal/high	—	PF5 to PF7
	Fixed to high drive output	PF0 to PF5	—
PORTG	Normal/high/high for high-speed interface	PG0, PG1	—
	High/high for high-speed interface	PG2 to PG7	—
PORTH	Normal/high	—	PH0 to PH3, PH6, PH7
PORTJ	Fixed to normal output	—	PJ6, PJ7
	Normal/high	—	PJ1, PJ3 to PJ5
	Normal/high/high for high-speed interface	PJ0 to PJ2	—
	Fixed to high drive output	PJ3, PJ5	—
PORTK	Normal/high	—	PK2 to PK5
PORTL	Normal/high	—	PL0, PL1
PORTN	Normal/high	—	PN6, PN7

Table 2.26 Comparison of I/O Port Registers

Register	Bit	RX65N	RX660
PDR	B0 to B7	Pm0 to 7 I/O select bits (m = 0 to 9, A to G, J)	Pm0 to 7 I/O select bits (m = 0 to 9, A to F, H, J to L, N)
PODR	B0 to B7	Pm0 to Pm7 output data store bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 output data store bits (m = 0 to 9, A to F, H, J to L, N)
PIDR	B0 to B7	Pm0 to Pm7 bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 bits (m = 0 to 9, A to F, H, J to L, N)
PMR	B0 to B7	Pm0 pin mode control bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 pin mode control bits (m = 0 to 9, A to F, H, J to L, N)
ODR0	B0, B2, B4, B6	Pm0, 2, 3, 4, and 6 output type select bits (m = 0 to 9, A to G, J) For pins other than the port PE1 pin Odd bit Even bit x 0: CMOS output x 1: N-channel open drain (b1, b3, b5, b7: Reserved) For port PE1 pin b3 b2 0 0: CMOS output 0 1: N-channel open drain 1 0: P-channel open drain 1 1: Setting prohibited.	Pm0, Pm2, Pm4, and Pm6 output type select bits (m = 0 to 9, A to E, H, J to L) 0: CMOS output 1: N-channel open drain
ODR1	B0, B2, B4, B6	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 0 to 9, A to G, J)	Pm4, Pm5, Pm6, and Pm7 output type select bits (m = 0 to 8, A to F, H, J, K, N)
PCR	B0 to B7	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to G, J)	Pm0 to Pm7 input pull-up resistor control bits (m = 0 to 9, A to F, H, J to L, N)
DSCR	—	Drive capacity control register (m =0 to 2, 5, 7 to 9, A to E, G, J)	Drive capacity control register (m = 0 to 3, 5 to 9, A to F, H, J to L, N)
DSCR2	—	Drive capacity control register 2	—

2.13 Multi-Function Pin Controller

Table 2.27 is Comparison of Multiplexed Pin Assignments, and Table 2.28 to Table 2.46 are Comparisons of Multi-Function Pin Controller Registers.

In the following comparison of the assignments of multiplexed pins, orange text pins that exist on the RX65N Group only and blue text designates pins that exist on the RX660 Group only. A circle (○) indicates that a function is assigned, a cross (×) that the pin does not exist or that no function is assigned, and grayed out items mean that the function is not implemented.

Table 2.27 Comparison of Multiplexed Pin Assignments

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
EXDMA controller	EDREQ0 (input)	P22	○	○	×			
		P55	○	○	×			
		P80	○	×	×			
	EDACK0 (output)	P23	○	○	×			
		P54	○	○	×			
		P81	○	×	×			
	EDREQ1 (input)	P24	○	○	×			
		P33	○	○	×			
		P82	○	×	×			
	EDACK1 (output)	P25	○	○	×			
		P56	○	×	×			
		P83	○	×	×			
		PJ3	○	○	×			
Interrupts	NMI (input)	P35	○	○	○	○	○	○
	IRQ0-DS (input)	P30	○	○	○	○	○	○
	IRQ0 (input)	P50	×	×	×	○	○	×
		P60	×	×	×	○	×	×
		P70	×	×	×	○	×	×
		P90	×	×	×	○	×	×
		PA0	×	×	×	○	○	○
		PD0	○	○	×	○	○	×
		PH1	×	×	×	○	○	○
	IRQ1-DS (input)	P31	○	○	○	○	○	○
	IRQ1 (input)	P51	×	×	×	○	○	×
		P61	×	×	×	○	×	×
		P71	×	×	×	○	×	×
		PD1	○	○	×	○	○	×
		PH2	×	×	×	○	○	○
	IRQ2-DS (input)	P32	○	○	×	○	○	○
	IRQ2 (input)	P12	○	○	○	○	○	×
		P52	×	×	×	○	○	×
		P62	×	×	×	○	×	×
		P82	×	×	×	○	×	×
		PB2	×	×	×	○	○	×
		PD2	○	○	○	○	○	×
	IRQ3-DS (input)	P33	○	○	×	○	○	×
	IRQ3 (input)	P13	○	○	○	○	○	×
		P23	×	×	×	○	○	×
		P53	×	×	×	○	○	×
		P63	×	×	×	○	×	×

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Interrupts	IRQ3 (input)	P83	×	×	×	○	×	×
		PB3	×	×	×	○	○	○
		PD3	○	○	○	○	○	×
	IRQ4-DS (input)	PB1	○	○	×	○	○	○
	IRQ4 (input)	P14	○	○	×	○	○	○
		P34	○	○	○	○	○	×
		P37	×	×	×	○	○	○
		P54	×	×	×	○	○	○
		P64	×	×	×	○	×	×
		PB4	×	×	×	○	○	×
		PD4	○	○	○	○	○	×
		PF5	○	×	×	○	×	×
	IRQ5-DS (input)	PA4	○	○	○	○	○	○
	IRQ5 (input)	P15	○	○	×	○	○	○
		P25	×	×	×	○	○	×
		P36	×	×	×	○	○	○
		PA5	×	×	×	○	○	×
		PC5	×	×	×	○	○	○
		PD5	○	○	○	○	○	×
		PE5	○	○	×	○	○	○
	IRQ6-DS (input)	PA3	○	○	×	○	○	○
	IRQ6 (input)	P16	○	○	○	○	○	○
		P26	×	×	×	○	○	○
		P56	×	×	×	○	×	×
		PB6	×	×	×	○	○	○
		PD6	○	○	○	○	○	×
		PE6	○	○	○	○	○	×
	IRQ7-DS (input)	PE2	○	○	○	○	○	○
	IRQ7 (input)	P17	○	○	○	○	○	○
		P27	×	×	×	○	○	○
		P77	×	×	×	○	×	×
		PA7	×	×	×	○	○	×
		PD7	○	○	○	○	○	×
		PE7	○	○	○	○	○	×
	IRQ8-DS (input)	P40	○	○	○	○	○	○
	IRQ8 (input)	P00	○	×	×	○	×	×
		P20	○	○	×	○	○	×
		P73	×	×	×	○	×	×
		P80	×	×	×	○	×	×
		PE0	×	×	×	○	○	○
	IRQ9-DS (input)	P41	○	○	○	○	○	○
	IRQ9 (input)	P01	○	×	×	○	×	×
		P21	○	○	×	○	○	×
		P81	×	×	×	○	×	×
		P91	×	×	×	○	×	×
		PE1	×	×	×	○	○	○
	IRQ10-DS (input)	P42	○	○	○	○	○	○
	IRQ10 (input)	P02	○	×	×	○	×	×
		P55	○	○	×	○	○	○
		P72	×	×	×	○	×	×

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Interrupts	IRQ10 (input)	P92	×	×	×	○	×	×
		PA2	×	×	×	○	○	×
		PC2	×	×	×	○	○	○
	IRQ11-DS (input)	P43	○	○	○	○	○	○
	IRQ11 (input)	P03	○	×	×	○	○(Note 1)	○
		P93	×	×	×	○	×	×
		PA1	○	○	○	○	○	○
		PC3	×	×	×	○	○	○
		PE3	×	×	×	○	○	○
		PJ3	×	×	×	○	○	×
	IRQ12-DS (input)	P44	○	○	×	○	○	○
	IRQ12 (input)	P24	×	×	×	○	○	×
		P74	×	×	×	○	×	×
		PB0	○	○	×	○	○	○
		PC1	○	○	○	○	○	×
		PC4	×	×	×	○	○	○
		PE4	×	×	×	○	○	○
	IRQ13-DS (input)	P45	○	○	×	○	○	○
	IRQ13 (input)	P05	○	○	○(Note 2)	○	○	×
		P65	×	×	×	○	×	×
		P75	×	×	×	○	×	×
		PB5	×	×	×	○	○	○
		PC6	○	○	○	○	○	○
		PJ5	×	×	×	○	×	×
	IRQ14-DS (input)	P46	○	○	×	○	○	○
	IRQ14 (input)	P66	×	×	×	○	×	×
		P76	×	×	×	○	×	×
		P86	×	×	×	○	×	×
		PA6	×	×	×	○	○	○
		PC0	○	○	○	○	○	×
		PC7	○	○	○	○	○	○
	IRQ15-DS (input)	P47	○	○	×	○	○	○
	IRQ15 (input)	P07	○	○	×	○	○	○
		P22	×	×	×	○	○	×
		P67	○	×	×	○	×	×
		P87	×	×	×	○	×	×
		PB7	×	×	×	○	○	○
Multi-function timer unit 3	MTIOC0A (input/output)	P34	○	○	○	○	○	×
		PB3	○	○	×	○	○	○
		PC4	×	×	×	○	○	○
	MTIOC0B (input/output)	P13	○	○	○	○	○	×
		P15	○	○	×	○	○	○
		PA1	○	○	○	○	○	○
	MTIOC0C (input/output)	P32	○	○	×	○	○	○
		PB1	○	○	×	○	○	○
		PC5	×	×	×	○	○	○
	MTIOC0D (input/output)	P33	○	○	×	○	○	×
		PA3	○	○	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Multi-function timer unit 3	MTIOC1A (input/output)	P20	○	○	×	○	○	×
		PE4	○	○	×	○	○	○
	MTIOC1B (input/output)	P21	○	○	×	○	○	×
		PB5	○	○	○	○	○	○
		PE3	×	×	×	○	○	○
	MTIOC2A (input/output)	P26	○	○	○	○	○	○
		PB5	○	○	○	○	○	○
	MTIOC2B (input/output)	P27	○	○	○	○	○	○
		PE5	○	○	×	○	○	○
	MTIOC3A (input/output)	P14	○	○	×	○	○	○
		P17	○	○	○	○	○	○
		PC1	○	○	○	○	○	×
		PC7	○	○	○	○	○	○
		PJ1	×	×	×	○	○	×
	MTIOC3B (input/output)	P17	○	○	○	○	○	○
		P22	○	○	×	○	○	×
		P80	○	×	×	○	×	×
		PA1	×	×	×	○	○	○
		PB7	○	○	○	○	○	○
		PC5	○	○	○	○	○	○
		PE1	○	○	○	○	○	○
		PH0	×	×	×	○	○	○
	MTIOC3C (input/output)	P16	○	○	○	○	○	○
		P56	○	×	×	○	×	×
		PC0	○	○	○	○	○	×
		PC6	○	○	○	○	○	○
		PJ3	○	○	×	○	○	×
	MTIOC3D (input/output)	P16	○	○	○	○	○	○
		P23	○	○	×	○	○	×
		P81	○	×	×	○	×	×
		PA6	×	×	×	○	○	○
		PB0	×	×	×	○	○	○
		PB6	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
		PE0	○	○	○	○	○	○
		PH1	×	×	×	○	○	○
	MTIOC4A (input/output)	P21	○	○	×	○	○	×
		P24	○	○	×	○	○	×
		P55	×	×	×	○	○	○
		P82	○	×	×	○	×	×
		PA0	○	○	×	○	○	○
		PB3	○	○	×	○	○	○
		PE2	○	○	○	○	○	○
		PE4	×	×	×	○	○	○
	MTIOC4B (input/output)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		P54	○	○	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Multi-function timer unit 3	MTIOC4B (input/output)	PC2	○	○	×	○	○	○
		PD1	○	○	×	○	○	×
		PE3	○	○	×	○	○	○
	MTIOC4C (input/output)	P25	○	○	×	○	○	×
		P83	○	×	×	○	×	×
		P87	○	×	×	○	×	×
		PA4	×	×	×	○	○	○
		PB1	○	○	×	○	○	○
		PE1	○	○	○	○	○	○
		PE5	○	○	×	○	○	○
		PH2	×	×	×	○	○	○
	MTIOC4D (input/output)	P31	○	○	○	○	○	○
		P55	○	○	×	○	○	○
		P86	○	×	×	○	×	×
		PA3	×	×	×	○	○	○
		PC3	○	○	×	○	○	○
		PD2	○	○	○	○	○	×
		PE4	○	○	×	○	○	○
		PH3	×	×	×	○	○	○
	MTIC5U (input)	P12	×	×	×	○	○	×
		PA4	○	○	○	○	○	○
		PD7	○	○	○	○	○	×
	MTIC5V (input)	PA3	×	×	×	○	○	○
		PA6	○	○	○	○	○	○
		PD6	○	○	○	○	○	×
	MTIC5W (input)	PB0	○	○	×	○	○	○
		PD5	○	○	○	○	○	×
	MTIOC6A (input/output)	PE7	○	○	○	○	○	×
	MTIOC6B (input/output)	PA5	○	○	×	○	○	×
		PA6	×	×	×	○	○	○
	MTIOC6C (input/output)	PE6	○	○	○	○	○	×
	MTIOC6D (input/output)	PA0	○	○	×	○	○	○
	MTIOC7A (input/output)	PA2	○	○	○	○	○	×
		PE2	×	×	×	○	○	○
	MTIOC7B (input/output)	PA1	○	○	○	○	○	○
	MTIOC7C (input/output)	P67	○	×	×	○	×	×
		PA4	×	×	×	○	○	○
	MTIOC7D (input/output)	P66	○	×	×	○	×	×
		PE4	×	×	×	○	○	○
	MTIOC8A (input/output)	PD6	○	○	○	○	○	×
	MTIOC8B (input/output)	PD4	○	○	○	○	○	×
	MTIOC8C (input/output)	PD5	○	○	○	○	○	×

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Multi-function timer unit 3	MTIOC8D (input/output)	PD3	○	○	○	○	○	×
	MTCLKA (input)	P14	○	○	×	○	○	○
		P24	○	○	×	○	○	×
		PA4	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	MTCLKB (input)	P15	○	○	×	○	○	○
		P25	○	○	×	○	○	×
	MTCLKB (input)	PA6	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	MTCLKC (input)	P22	○	○	×	○	○	×
		PA1	○	○	○	○	○	○
		PC4	○	○	○	○	○	○
	MTCLKD (input)	P23	○	○	×	○	○	×
		PA3	○	○	×	○	○	○
		PC5	○	○	○	○	○	○
Port output enable 3	POE0# (input)	P32	○	○	×	○	○	○
		P93	○	×	×	○	×	×
		PC4	○	○	○	○	○	○
		PD1	○	○	×	○	○	×
		PD7	○	○	○	○	○	×
	POE4# (input)	P33	○	○	×	○	○	×
		P92	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
		PD0	○	○	×	○	○	×
		PD6	○	○	○	○	○	×
	POE8# (input)	P17	○	○	○	○	○	○
		P30	○	○	○	○	○	○
		PD3	○	○	○	○	○	×
		PE3	○	○	×	○	○	○
		PJ5	○	×	×	○	×	×
	POE10# (input)	P32	○	○	×	○	○	○
		P34	○	○	○	○	○	×
		PA6	○	○	○	○	○	○
		PD5	○	○	○	○	○	×
	POE11# (input)	P33	○	○	×	○	○	×
		PB3	○	○	×	○	○	○
		PD4	○	○	○	○	○	×
16-bit timer pulse unit	TIOCA0 (input/output)	P86	○	×	×			
		PA0	○	○	×			
	TIOCB0 (input/output)	P17	○	○	○			
		PA1	○	○	○			
	TIOCC0 (input/output)	P32	○	○	×			
	TIOCD0 (input/output)	P33	○	○	×			
		PA3	○	○	×			
	TIOCA1 (input/output)	P56	○	×	×			
		PA4	○	○	○			

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
16-bit timer pulse unit	TIOCB1 (input/output)	P16	○	○	○			
		PA5	○	○	×			
	TIOCA2 (input/output)	P87	○	×	×			
		PA6	○	○	○			
	TIOCB2 (input/output)	P15	○	○	×			
		PA7	○	○	○			
	TIOCA3 (input/output)	P21	○	○	×			
		PB0	○	○	×			
	TIOCB3 (input/output)	P20	○	○	×			
		PB1	○	○	×			
	TIOCC3 (input/output)	P22	○	○	×			
		PB2	○	○	×			
	TIOCD3 (input/output)	P23	○	○	×			
		PB3	○	○	×			
	TIOCA4 (input/output)	P25	○	○	×			
		PB4	○	○	×			
	TIOCB4 (input/output)	P24	○	○	×			
		PB5	○	○	○			
	TIOCA5 (input/output)	P13	○	○	○			
		PB6	○	○	○			
	TIOCB5 (input/output)	P14	○	○	×			
		PB7	○	○	○			
	TCLKA (input)	P14	○	○	×			
		PC2	○	○	×			
	TCLKB (input)	P15	○	○	×			
		PA3	○	○	×			
		PC3	○	○	×			
	TCLKC (input)	P16	○	○	○			
		PB2	○	○	×			
		PC0	○	○	○			
	TCLKD (input)	P17	○	○	○			
		PB3	○	○	×			
		PC1	○	○	○			
Programmable pulse generator	PO0 (output)	P20	○	○	×			
	PO1 (output)	P21	○	○	×			
	PO2 (output)	P22	○	○	×			
	PO3 (output)	P23	○	○	×			
	PO4 (output)	P24	○	○	×			
	PO5 (output)	P25	○	○	×			
	PO6 (output)	P26	○	○	×			
	PO7 (output)	P27	○	○	×			
	PO8 (output)	P30	○	○	×			
	PO9 (output)	P31	○	○	×			
	PO10 (output)	P32	○	○	×			
	PO11 (output)	P33	○	○	×			
	PO12 (output)	P34	○	○	×			
	PO13 (output)	P13	○	○	×			
		P15	○	○	×			
	PO14 (output)	P16	○	○	×			

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Programmable pulse generator	PO15 (output)	P14	○	○	×			
		P17	○	○	×			
	PO16 (output)	P73	○	×	×			
		PA0	○	○	×			
	PO17 (output)	PA1	○	○	×			
		PC0	○	○	×			
	PO18 (output)	PA2	○	○	×			
		PC1	○	○	×			
		PE1	○	○	×			
	PO19 (output)	P74	○	×	×			
		PA3	○	○	×			
	PO20 (output)	P75	○	×	×			
		PA4	○	○	×			
	PO21 (output)	PA5	○	○	×			
		PC2	○	○	×			
	PO22 (output)	P76	○	×	×			
		PA6	○	○	×			
	PO23 (output)	P77	○	×	×			
		PA7	○	○	×			
		PE2	○	○	×			
	PO24 (output)	PB0	○	○	×			
		PC3	○	○	×			
	PO25 (output)	PB1	○	○	×			
		PC4	○	○	×			
	PO26 (output)	P80	○	×	×			
		PB2	○	○	×			
		PE3	○	○	×			
	PO27 (output)	P81	○	×	×			
		PB3	○	○	×			
	PO28 (output)	P82	○	×	×			
		PB4	○	○	×			
		PE4	○	○	×			
	PO29 (output)	PB5	○	○	×			
		PC5	○	○	×			
	PO30 (output)	PB6	○	○	×			
		PC6	○	○	×			
	PO31 (output)	PB7	○	○	×			
		PC7	○	○	×			
8-bit timer	TMO0 (output)	P22	○	○	×	○	○	×
		PB3	○	○	×	○	○	○
		PH1	×	×	×	○	○	○
	TMCI0 (input)	P01	○	×	×	○	×	×
		P21	○	○	×	○	○	×
		PB1	○	○	×	○	○	○
		PH3	×	×	×	○	○	○
	TMRI0 (input)	P00	○	×	×	○	×	×
		P20	○	○	×	○	○	×
		PA4	○	○	○	○	○	○
		PH2	×	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
8-bit timer	TMO1 (output)	P17	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	TMCI1 (input)	P02	○	×	×	○	×	×
		P12	○	○	○	○	○	×
		P54	○	○	×	○	○	○
		PC4	○	○	○	○	○	○
	TMRI1 (input)	P24	○	○	×	○	○	×
		PB5	○	○	○	○	○	○
	TMO2 (output)	P16	○	○	○	○	○	○
		PC7	○	○	○	○	○	○
	TMCI2 (input)	P15	○	○	×	○	○	○
		P31	○	○	○	○	○	○
		PC6	○	○	○	○	○	○
	TMRI2 (input)	P14	○	○	×	○	○	○
		PC5	○	○	○	○	○	○
	TMO3 (output)	P13	○	○	○	○	○	×
		P32	○	○	×	○	○	○
		P55	○	○	×	○	○	○
	TMCI3 (input)	P27	○	○	○	○	○	○
		P34	○	○	○	○	○	×
		PA6	○	○	○	○	○	○
	TMRI3 (input)	P30	○	○	○	○	○	○
		P33	○	○	○	○	○	○
Compare match timer W	TOC0 (output)	PC7	○	○	○	○	○	○
	TIC0 (input)	PC6	○	○	○	○	○	○
	TOC1 (output)	PE7	○	○	○	○	○	×
		PH2	×	×	×	○	○	○
	TIC1 (input)	PE6	○	○	○	○	○	×
		PH1	×	×	×	○	○	○
	TOC2 (output)	PD3	○	○	○	○	○	×
		PB5	×	×	×	○	○	○
	TIC2 (input)	PD2	○	○	○	○	○	×
		PB3	×	×	×	○	○	○
	TOC3 (output)	PE3	○	○	×	○	○	○
	TIC3 (input)	PE2	○	○	○	○	○	○
Ethernet controller	REF50CK0 (input)	P76	○	×	×			
		PB2	○	○	×			
		PE5	○	○	×			
	RMII0_CRS_DV (input)	P83	○	×	×			
	RMII0_CRS_DV (input)	PB7	○	○	×			
	RMII0_TXD0 (output)	P81	○	×	×			
		PB5	○	○	×			
	RMII0_TXD1 (output)	P82	○	×	×			
		PB6	○	○	×			
	RMII0_RXD0 (input)	P75	○	×	×			
		PB1	○	○	×			
	RMII0_RXD1 (input)	P74	○	×	×			
		PB0	○	○	×			

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Ethernet controller	RMII0_TXD_EN (output)	P80	○	×	×			
		PA0	○	○	×			
		PB4	○	○	×			
	RMII0_RX_ER (input)	P77	○	×	×			
		PB3	○	○	×			
	ET0_CRS (input)	P83	○	×	×			
		PB7	○	○	×			
	ET0_RX_DV (input)	PC2	○	○	×			
	ET0_EXOUT (output)	P55	○	○	×			
		PA6	○	○	×			
	ET0_EXOUT (output)	PJ3	○	○	×			
	ET0_LINKSTA (input)	P34	○	○	×			
		P54	○	○	×			
		PA5	○	○	×			
	ET0_ETXD0 (output)	P81	○	×	×			
		PB5	○	○	×			
	ET0_ETXD1 (output)	P82	○	×	×			
		PB6	○	○	×			
	ET0_ETXD2 (output)	PC5	○	○	×			
	ET0_ETXD3 (output)	PC6	○	○	×			
	ET0_ERXD0 (input)	P75	○	×	×			
		PB1	○	○	×			
	ET0_ERXD1 (input)	P74	○	×	×			
		PB0	○	○	×			
	ET0_ERXD2 (input)	PC1	○	○	×			
		PE4	○	○	×			
	ET0_ERXD3 (input)	PC0	○	○	×			
		PE3	○	○	×			
	ET0_TX_EN (output)	P80	○	×	×			
		PA0	○	○	×			
		PB4	○	○	×			
	ET0_TX_ER (output)	PC3	○	○	×			
	ET0_RX_ER (input)	P77	○	×	×			
		PB3	○	○	×			
	ET0_TX_CLK (input)	PC4	○	○	×			
	ET0_RX_CLK (input)	P76	○	×	×			
		PB2	○	○	×			
		PE5	○	○	×			
	ET0_COL (input)	PC7	○	○	×			
	ET0_WOL (output)	P73	○	×	×			
		PA1	○	○	×			
		PA7	○	○	×			
	ET0_MDC (output)	P72	○	×	×			
		PA4	○	○	×			
	ET0_MDIO (input/output)	P71	○	×	×			
		PA3	○	○	×			

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Serial communications interface	RXD0 (input)/ SMISO0 (input/output)/ SSCL0 (input/output)	P21	○	○	×	○	○	×
		P33	○	○	×	○	○	×
	TXD0 (output)/ SMOSI0 (input/output)/ SSDA0 (input/output)	P20	○	○	×	○	○	×
		P32	○	○	×	○	○	×
	SCK0 (input/output)	P22	○	○	×	○	○	×
		P34	○	○	×	○	○	×
	CTS0# (input)/ RTS0# (output)/ SS0# (input)	P23	○	○	×	○	○	×
		PJ3	○	○	×	○	○	×
	RXD1 (input)/ SMISO1 (input/output)/ SSCL1 (input/output)	P15	○	○	×	○	○	○
		P30	○	○	○	○	○	○
	TXD1 (output)/ SMOSI1 (input/output)/ SSDA1 (input/output)	P16	○	○	○	○	○	○
		P26	○	○	○	○	○	○
	SCK1 (input/output)	P17	○	○	○	○	○	○
		P27	○	○	○	○	○	○
	CTS1# (input)/ RTS1# (output)/ SS1# (input)	P14	○	○	×	○	○	○
		P31	○	○	○	○	○	○
	RXD2 (input)/ SMISO2 (input/output)/ SSCL2 (input/output)	P12	○	○	○(Note 3)	○	○	×
		P52	○	○	×	○	○	×
	TXD2 (output)/ SMOSI2 (input/output)/ SSDA2 (input/output)	P13	○	○	○(Note 3)	○	○	×
		P50	○	○	×	○	○	×
	SCK2 (input/output)	P51	○	○	×	○	○	×
	CTS2# (input)/ RTS2# (output)/ SS2# (input)	P54	○	○	×	○	○	×
		PJ5	○	×	×	○	×	×
	RXD3 (input)/ SMISO3 (input/output)/ SSCL3 (input/output)	P16	○	○	○(Note 3)	○	○	○
		P25	○	○	×	○	○	×
	TXD3 (output)/ SMOSI3 (input/output)/ SSDA3 (input/output)	P17	○	○	○(Note 3)	○	○	○
		P23	○	○	×	○	○	×
	SCK3 (input/output)	P15	○	○	×	○	○	○
		P24	○	○	×	○	○	×
	CTS3# (input)/ RTS3# (output)/ SS3# (input)	P26	○	○	○(Note 3)	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Serial communications interface	RXD4 (input)/ SMISO4 (input/output)/ SSCL4 (input/output)	PB0	○	×	×	○	○	○
		PK4	×	×	×	○	×	×
	TXD4 (output)/ SMOSI4 (input/output)/ SSDA4 (input/output)	PB1	○	×	×	○	○	○
		PK5	×	×	×	○	×	×
	SCK4 (input/output)	P70	×	×	×	○	×	×
		PB3	○	×	×	○	○	○
	CTS4# (input)/ RTS4# (output)/ SS4# (input)	PB2	○	×	×	○	○	×
		PE6	×	×	×	○	○	×
	RXD5 (input)/ SMISO5 (input/output)/ SSCL5 (input/output)	PA2	○	○	○	○	○	×
		PA3	○	○	×	○	○	○
		PC2	○	○	×	○	○	○
	TXD5 (output)/ SMOSI5 (input/output)/ SSDA5 (input/output)	PA4	○	○	○	○	○	○
		PC3	○	○	×	○	○	○
	SCK5 (input/output)	PA1	○	○	○	○	○	○
		PC1	○	○	×	○	○	×
		PC4	○	○	×	○	○	○
	CTS5# (input)/ RTS5# (output)/ SS5# (input)	PA6	○	○	○	○	○	○
		PC0	○	○	×	○	○	×
	RXD6 (input)/ SMISO6 (input/output)/ SSCL6 (input/output)	P01	○	×	×	○	×	×
		P33	○	○	×	○	○	×
		PB0	○	○	×	○	○	○
	TXD6 (output)/ SMOSI6 (input/output)/ SSDA6 (input/output)	P00	○	×	×	○	×	×
		P32	○	○	×	○	○	○
		PB1	○	○	×	○	○	○
	SCK6 (input/output)	P02	○	×	×	○	×	×
		P34	○	○	×	○	○	×
		PB3	○	○	×	○	○	○
	CTS6# (input)/ RTS6# (output)/ SS6# (input)	PB2	○	○	×	○	○	×
		PJ3	○	○	×	○	○	×
	RXD7 (input)/ SMISO7 (input/output)/ SSCL7 (input/output)	P92	○	×	×	○	×	×
	TXD7 (output)/ SMOSI7 (input/output)/ SSDA7 (input/output)	P55	○(Note 4)	×	×	○	×	×
		P90	○	×	×	○	×	×

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Serial communications interface	SCK7 (input/output)	P56	○(Note 4)	×	×	○	×	×
		P91	○	×	×	○	×	×
	CTS7# (input)/ RTS7# (output)/ SS7# (input)	P93	○	×	×	○	×	×
	RXD8 (input)/ SMISO8 (input/output)/ SSCL8 (input/output)	PC6	○	○	○	○	○	○
	TXD8 (output)/ SMOSI8 (input/output)/ SSDA8 (input/output)	PC7	○	○	○	○	○	○
	SCK8 (input/output)	PC5	○	○	○	○	○	○
	CTS8# (input)/ RTS8# (output)/ SS8# (input)	PC4	○	○	○	○	○	○
	RXD9 (input)/ SMISO9 (input/output)/ SSCL9 (input/output)	PB6	○	○	○(Note 3)	○	○	○
		PK3	×	×	×	○	×	×
	TXD9 (output)/ SMOSI9 (input/output)/ SSDA9 (input/output)	PB7	○	○	○(Note 3)	○	○	○
		PK2	×	×	×	○	×	×
	SCK9 (input/output)	PB5	○	○	○	○	○	○
		P60	×	×	×	○	×	×
	CTS9# (input)/ RTS9# (output)/ SS9# (input)	P61	×	×	×	○	×	×
		PB4	○	○	×	○	○	×
	RXD10 (input)/ SMISO10 (input/output)/ SSCL10 (input/output)	P81	○	×	×	○	×	×
		P86	○	×	×	○	×	×
		PC6	○	○	○	○	○	○
	TXD10 (output)/ SMOSI10 (input/output)/ SSDA10 (input/output)	P82	○	×	×	○	×	×
		P87	○	×	×	○	×	×
		PC7	○	○	○	○	○	○
	SCK10 (input/output)	P80	○	×	×	○	×	×
		P83	○	×	×	○	×	×
		PC5	○	○	○	○	○	○
	RTS10# (output)	P80	○	×	×	○	×	×
	CTS10# (input)/ SS10# (input)	P83	○	×	×	○	×	×
	CTS10# (input)/ RTS10# (output)/ SS10# (input)	PC4	○	○	○	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Serial communications interface	RXD11 (input)/ SMISO11 (input/output)/ SSCL11 (input/output)	P76	○	×	×	○	×	×
		PB6	○	○	○(Note 3)	○	○	○
	TXD11 (output)/ SMOSI11 (input/output)/ SSDA11 (input/output)	P77	○	×	×	○	×	×
		PB7	○	○	○(Note 3)	○	○	○
	SCK11 (input/output)	P75	○	×	×	○	×	×
		PB5	○	○	○	○	○	○
	RTS11# (output)	P75	○	×	×	○	×	×
	CTS11# (input)/ SS11# (input)	P74	○	×	×	○	×	×
	CTS11# (input)/ RTS11# (output)/ SS11# (input)	PB4	○	○	×	○	○	×
	RXD12 (input)/ SMISO12 (input/output)/ SSCL12 (input/output)/ RXDX12 (input)	PA2	×	×	×	○	○	×
		PE2	○	○	○(Note 3)	○	○	○
	TXD12 (output)/ SMOSI12 (input/output)/ SSDA12 (input/output)/ TXDX12 (output)/ SIOX12 (input/output)	PA4	×	×	×	○	○	○
		PE1	○	○	○(Note 3)	○	○	○
	SCK12 (input/output)	PE0	○	○	○	○	○	○
		PA1	×	×	×	○	○	○
	CTS12# (input)/ RTS12# (output)/ SS12# (input)	PA6	×	×	×	○	○	○
		PE3	○	○	×	○	○	○
I^2C bus interface	SCL0[FM+] (input/output)	P12	○	○	○			
	SDA0[FM+] (input/output)	P13	○	○	○			
	SCL1 (input/output)	P21	○	○	×			
	SDA1 (input/output)	P20	○	○	×			
	SCL2-DS (input/output)	P16	○	○	○			
	SDA2-DS (input/output)	P17	○	○	○			

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
USB2.0FS host or function module	USB0_VBUS (input)	P16	○	○	○			
	USB0_EXICEN (output)	P21	○	○	×			
	USB0_VBUSEN (output)	P16	○	○	×			
		P24	○	○	×			
		P32	○	○	×			
	USB0_OVRCURA (input)	P14	○	○	×			
	USB0_OVRCURB (input)	P16	○	○	×			
		P22	○	○	×			
	USB0_ID (input)	P20	○	○	×			
CAN module	CRX0 (input)	P33	○	○	×			
		PD2	○	○	×			
	CTX0 (output)	P32	○	○	×			
		PD1	○	○	×			
	CRX1-DS (input)	P15	○	○	×			
	CRX1 (input)	P55	○	○	×			
	CTX1 (output)	P14	○	○	×			
		P54	○	○	×			
CANFD module	CRX0 (input)	P15				○	○	×
		P55				○	○	×
	CTX0 (output)	P14				○	○	○
		P54				○	○	×
Serial peripheral interface	RSPCKA (input/output)	PA5	○	○	×	○	○	×
		PC5	○	○	○	○	○	○
		PB0	×	×	×	○	○	○
	MOSIA (input/output)	P16	×	×	×	○	○	○
		PA6	○	○	×	○	○	○
		PC6	○	○	○	○	○	○
	MISOA (input/output)	PA7	○	○	×	○	○	×
		P17	×	×	×	○	○	○
		PC7	○	○	○	○	○	○
	SSLA0 (input/output)	PA4	○	○	×	○	○	○
		PC4	○	○	○	○	○	○
	SSLA1 (output)	PA0	○	○	×	○	○	○
		PC0	○	○	○	○	○	×
	SSLA2 (output)	PA1	○	○	×	○	○	○
		PC1	○	○	○	○	○	×
	SSLA3 (output)	PA2	○	○	×	○	○	×
		PC2	○	○	×	○	○	○
	RSPCKB (input/output)	P27	○	○	○			
		PE5	○	○	×			
	MOSIB (input/output)	P26	○	○	○			
		PE6	○	○	×			
	MISOB (input/output)	P30	○	○	○			
		PE7	○	○	×			
	SSLB0 (input/output)	P31	○	○	○			
		PE4	○	○	×			
	SSLB1 (output)	P50	○	○	×			
		PE0	○	○	×			

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Serial peripheral interface	SSLB2 (output)	P51	○	○	×			
		PE1	○	○	×			
	SSLB3 (output)	P52	○	○	×			
		PE2	○	○	×			
	RSPCKC (input/output)	PD3	○	○	×			
	MOSIC (input/output)	PD1	○	○	×			
	MISOC (input/output)	PD2	○	○	×			
	SSLC0 (input/output)	PD4	○	○	×			
	SSLC1 (output)	PD5	○	○	×			
	SSLC2 (output)	PD6	○	○	×			
	SSLC3 (output)	PD7	○	○	×			
Realtime clock	RTCOUT (output)	P16	○	○	○	○	○	○
		P32	○	○	×	○	○	○
	RTCIC0 (input)	P30	○	○	○			
	RTCIC1 (input)	P31	○	○	○			
	RTCIC2 (input)	P32	○	○	×			
12-bit A/D converter	AN000 (input)	P40	○	○	○	○	○	○
	AN001 (input)	P41	○	○	○	○	○	○
	AN002 (input)	P42	○	○	○	○	○	○
	AN003 (input)	P43	○	○	○	○	○	○
	AN004 (input)	P44	○	○	×	○	○	○
	AN005 (input)	P45	○	○	×	○	○	○
	AN006 (input)	P46	○	○	×	○	○	○
	AN007 (input)	P47	○	○	×	○	○	○
	AN008 (input)	PE0				○	○	○
	AN009 (input)	PE1				○	○	○
	AN010 (input)	PE2				○	○	○
	AN011 (input)	PE3				○	○	○
	AN012 (input)	PE4				○	○	○
	AN013 (input)	PE5				○	○	○
	AN014 (input)	PE6				○	○	×
	AN015 (input)	PE7				○	○	×
	AN016 (input)	PD0				○	○	×
	AN017 (input)	PD1				○	○	×
	AN018 (input)	PD2				○	○	×
	AN019 (input)	PD3				○	○	×
	AN020 (input)	PD4				○	○	×
	AN021 (input)	PD5				○	○	×
	AN022 (input)	PD6				○	○	×
	AN023 (input)	PD7				○	○	×
	ADST0 (output)	PA4				○	○	○
		PH1				○	○	○
	ADTRG0# (input)	P07	○	○	×	○	○	○
		P16	○	○	○	○	○	○
		P25	○	○	×	○	○	×
		PA1	×	×	×	○	○	○
		PH0	×	×	×	○	○	○

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
12-bit A/D converter	AN100 (input)	PE2	○	○	×			
	AN101 (input)	PE3	○	○	×			
	AN102 (input)	PE4	○	○	×			
	AN103 (input)	PE5	○	○	×			
	AN104 (input)	PE6	○	○	×			
	AN105 (input)	PE7	○	○	×			
	AN106 (input)	PD6	○	○	○			
	AN107 (input)	PD7	○	○	○			
	AN108 (input)	PD0	○	○	×			
	AN109 (input)	PD1	○	○	×			
	AN110 (input)	PD2	○	○	○			
	AN111 (input)	PD3	○	○	○			
	AN112 (input)	PD4	○	○	○			
	AN113 (input)	PD5	○	○	○			
	AN114 (input)	P90	○	×	×			
	AN115 (input)	P91	○	×	×			
	AN116 (input)	P92	○	×	×			
	AN117 (input)	P93	○	×	×			
	AN118 (input)	P00	○	×	×			
	AN119 (input)	P01	○	×	×			
	AN120 (input)	P02	○	×	×			
	ANEX0 (output)	PE0	○	○	○			
	ANEX1 (input)	PE1	○	○	○			
	ADTRG1# (input)	P13	○	○	○			
		P17	○	○	○			
	DA0 (output)	P03	○	×	×	○	○(Note 1)	○
	DA1 (output)	P05	○	○	○(Note 2)	○	○	×
Parallel data capture unit	PIXCLK (input)	P24	○	×	×			
	VSYNC (input)	P32	○	×	×			
	HSYNC (input)	P25	○	×	×			
	PIXD0 (input)	P15	○	×	×			
	PIXD1 (input)	P86	○	×	×			
	PIXD2 (input)	P87	○	×	×			
	PIXD3 (input)	P17	○	×	×			
	PIXD4 (input)	P20	○	×	×			
	PIXD5 (input)	P21	○	×	×			
	PIXD6 (input)	P22	○	×	×			
	PIXD7 (input)	P23	○	×	×			
	PCKO (output)	P33	○	×	×			
MMC host interface	MMC_RES# (output)	P75	○	×	×			
		PE7	○	○	×			
	MMC_CLK (output)	P77	○	×	×			
		PD5	○	○	×			
	MMC_CD (input)	PC2	○	×	×			
		PE6	○	○	×			
	MMC_CMD (input/output)	P76	○	×	×			
		PD4	○	○	×			

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
MMC host interface	MMC_D0 (input/output)	PC3	○	×	×			
		PD6	○	○	×			
	MMC_D1 (input/output)	PC4	○	×	×			
		PD7	○	○	×			
	MMC_D2 (input/output)	P80	○	×	×			
	MMC_D2 (input/output)	PD2	○	○	×			
	MMC_D3 (input/output)	P81	○	×	×			
		PD3	○	○	×			
	MMC_D4 (input/output)	P82	○	×	×			
		PE0	○	○	×			
	MMC_D5 (input/output)	PC5	○	×	×			
		PE1	○	○	×			
	MMC_D6 (input/output)	PC6	○	×	×			
		PE2	○	○	×			
	MMC_D7 (input/output)	PC7	○	×	×			
		PE3	○	○	×			
SD host interface	SDHI_CLK (output)	P21	○(Note 4)	×	×			
		P77	○	×	×			
		PD5	○	○	○			
	SDHI_CMD (input/output)	P20	○(Note 4)	×	×			
		P76	○	×	×			
		PD4	○	○	○			
	SDHI_CD (input)	P25	○(Note 4)	×	×			
		P81	○	×	×			
		PE6	○	○	○			
	SDHI_WP (input)	P24	○(Note 4)	×	×			
		P80	○	×	×			
		PE7	○	○	○			
	SDHI_D0 (input/output)	P22	○(Note 4)	×	×			
		PC3	○	×	×			
		PD6	○	○	○			
	SDHI_D1 (input/output)	P23	○(Note 4)	×	×			
		PC4	○	×	×			
		PD7	○	○	○			
	SDHI_D2 (input/output)	P75	○	×	×			
		P87	○(Note 4)	×	×			
		PD2	○	○	○			
	SDHI_D3 (input/output)	P17	○(Note 4)	×	×			
		PC2	○	×	×			
		PD3	○	○	○			
SD slave interface	SDSI_CLK (input)	P77	○	×	×			
		PB5	○	○	×			
	SDSI_CMD (input/output)	P76	○	×	×			
		PB4	○	○	×			
	SDSI_D0 (input/output)	PC3	○	×	×			
		PB6	○	○	×			
	SDSI_D1 (input/output)	PC4	○	×	×			
		PB7	○	○	×			

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
SD slave interface	SDSI_D2 (input/output)	P75	○	×	×			
		PB2	○	○	×			
	SDSI_D3 (input/output)	PC2	○	×	×			
		PB3	○	○	×			
Clock frequency accuracy measurement circuit	CACREF (input)	PC7	○	○	○	○	○	○
		PA0	○	○	×	○	○	○
		PH0	×	×	×	○	○	○
Quad serial peripheral interface	QSPCLK (input/output)	P77	○	×	×			
		PD5	○	○	○			
	QSSL (input/output)	P76	○	×	×			
		PD4	○	○	○			
	QMO/QIO0 (input/output)	PC3	○	×	×			
		PD6	○	○	○			
	QMI/QIO1 (input/output)	PC4	○	×	×			
		PD7	○	○	○			
	QIO2 (input/output)	P80	○	×	×			
		PD2	○	○	○			
	QIO3 (input/output)	P81	○	×	×			
		PD3	○	○	○			
LCD control(Note 4)	LCD_EXTCLK (input)	PD0	○	○	×			
	LCD_CLK (output)	PB5	○	○	×			
	LCD_TCON0 (output)	PB4	○	○	×			
	LCD_TCON1 (output)	PB3	○	○	×			
	LCD_TCON2 (output)	PB2	○	○	×			
	LCD_TCON3 (output)	PB1	○	○	×			
	LCD_DATA0 (output)	PB0	○	○	×			
	LCD_DATA1 (output)	PA7	○	○	×			
	LCD_DATA2 (output)	PA6	○	○	×			
	LCD_DATA3 (output)	PA5	○	○	×			
	LCD_DATA4 (output)	PA4	○	○	×			
	LCD_DATA5 (output)	PA3	○	○	×			
	LCD_DATA6 (output)	PA2	○	○	×			
	LCD_DATA7 (output)	PA1	○	○	×			
	LCD_DATA8 (output)	PA0	○	○	×			
	LCD_DATA9 (output)	PE7	○	○	×			
	LCD_DATA10 (output)	PE6	○	○	×			
	LCD_DATA11 (output)	PE5	○	○	×			
	LCD_DATA12 (output)	PE4	○	○	×			
	LCD_DATA13 (output)	PE3	○	○	×			
	LCD_DATA14 (output)	PE2	○	○	×			
	LCD_DATA15 (output)	PE1	○	○	×			
	LCD_DATA16 (output)	PE0	○	○	×			

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
LCD control(Note 4)	LCD_DATA17 (output)	PD7	○	○	×			
	LCD_DATA18 (output)	PD6	○	○	×			
	LCD_DATA19 (output)	PD5	○	○	×			
	LCD_DATA20 (output)	PD4	○	○	×			
	LCD_DATA21 (output)	PD3	○	○	×			
	LCD_DATA22 (output)	PD2	○	○	×			
	LCD_DATA23 (output)	PD1	○	○	×			
Realtime clock	RTCIC0 (input)(Note 5)	P30				○	○	○
	RTCIC1 (input)(Note 5)	P31				○	○	○
	RTCIC2 (input)(Note 5)	P32				○	○	○
Serial communications interface	RXD010 (input)/ SMISO010 (input/output)/ SSCL010 (input/output)	P81				○	×	×
		P86				○	×	×
		PC6				○	○	○
	TXD010 (output)/ SMOSI010 (input/output)/ SSDA010 (input/output)	P82				○	×	×
		P87				○	×	×
		PC7				○	○	○
	SCK010 (input/output)/ RTS010# (output)/ DE010 (output)	P80				○	×	×
	SCK010 (input/output)/ CTS010# (input)/ SS010# (input)	P83				○	×	×
	SCK010 (input/output)	PC5				○	○	○
	CTS010# (input)/ RTS010# (output)/ SS010# (input)/ DE010 (output)	PC4				○	○	○
	RXD011 (input)/ SMISO011 (input/output)/ SSCL011 (input/output)	P76				○	×	×
		PB6				○	○	○
		PC0				○	○	×

Module/ Function	Pin Function	Port Allocation	RX65N			RX660		
			144-Pin	100-Pin	64-Pin	144-Pin	100-Pin	64-Pin
Serial communications interface	TXD011 (output)/ SMOSI011 (input/output)/ SSDA011 (input/output)	P77				○	×	×
		PB7				○	○	○
		PC1				○	○	×
	SCK011 (input/output)/ RTS011# (output)/ DE011 (output)	P75				○	×	×
	SCK011 (input/output)	PB5				○	○	○
	TXDA011 (output)	PC1				○	○	×
	TXDB011 (output)	PC2				○	○	○
	CTS011# (input)/ SS011# (input)	P74				○	×	×
	CTS011# (input)/ RTS011# (output)/ SS011# (input)/ DE011 (output)	PB4				○	○	×
I^2C bus interface	SCL0 (input/output)	P12				○	○	×
	SDA0 (input/output)	P13				○	○	×
	SCL2 (input/output)	P16				○	○	○
	SDA2 (input/output)	P17				○	○	○
Remote control signal receiver	PMC0 (input)	P51				○	○	×
		P53				○	○	×
		PB3				○	○	○
		PC3				○	○	○
		PC4				○	○	○
		PC5				○	○	○
Comparator C	CMPC00 (input)	PE1				○	○	○
	CMPC10 (input)	PA3				○	○	○
	CMPC20 (input)	P15				○	○	○
	CMPC30 (input)	P26				○	○	○
	COMP0 (output)	PE5				○	○	○
	COMP1 (output)	PB1				○	○	○
	COMP2 (output)	P17				○	○	○
	COMP3 (output)	P30				○	○	○
	CVREFC0 (input)	PE2				○	○	○
	CVREFC1 (input)	PA4				○	○	○
	CVREFC2 (input)	P14				○	○	○
	CVREFC3 (input)	P27				○	○	○

Note 1. Not present on products not provided with a JTAG.
Note 2. Not present on 64-pin TFBGA.
Note 3. Simple SPI mode is not supported.
Note 4. Products with code flash memory capacity of 1 MB or less are not supported.
Note 5. Not available on products without a sub-clock oscillator.

Table 2.28 Comparison of P0n Pin Function Control Registers (P0nPFS)

Register	Bit	RX65N (n = 0 to 3, 5, or 7)	RX660 (n = 0 to 3, 5, or 7)
P0nPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P00: AN118 (177/176/145/144-pin) P01: AN119 (177/176/145/144-pin) P02: AN120 (177/176/145/144-pin) P03: DA0 (177/176/145/144-pin) P05: DA1 (177/176/145/144/100/64-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin P03: DA0 (144/100(Note 1)/80/64-pin) P05: DA1 (144/100/80-pin)

Note 1. Not present on products not provided with a JTAG.

Table 2.29 Comparison of P1n Pin Function Control Registers (P1nPFS)

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 2 to 7)
P10PFS	PSEL[5:0]	P10 pin function select bits	—
P11PFS	PSEL[5:0]	P11 pin function select bits	—
P12PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2/SMISO2/SSCL2 001111b: SCL0[FM+] 100101b: LCD_TCON1-A	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000101b: TMCI1 001010b: RXD2(Note 2)/SMISO2(Note 2)/ SSCL2(Note 2) 001111b: SCL0
P13PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000011b: TIOCA5 000101b: TMO3 000110b: PO13 001001b: ADTRG1# 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0[FM+] 100101b: LCD_TCON0-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000101b: TMO3 001010b: TXD2/SMOSI2/SSDA2 001111b: SDA0
P14PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000011b: TIOCB5 000100b: TCLKA 000101b: TMRI2 000110b: PO15 001011b: CTS1#/RTS1#/SS1# 010000b: CTX1 010010b: USB0_OVRCURA 100101b: LCD_CLK-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKA 000101b: TMRI2 001011b: CTS1#/RTS1#/SS1# 010000b: CTX0

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 2 to 7)
P15PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000011b: TIOCB2 000100b: TCLKB 000101b: TMCI2 000110b: PO13 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX1-DS 011100b: PIXD0	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKB 000101b: TMCI2 001010b: RXD1/SMISO1/SSCL1 001011b: SCK3 010000b: CRX0
P16PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTIOC3D 000011b: TIOCB1 000100b: TCLKC 000101b: TMO2 000110b: PO14 000111b: RTCOUT 001001b: ADTRG0# 001010b: TXD1/SMOSI1/SSDA1 001011b: RXD3/SMISO3/SSCL3 001111b: SCL2-DS 010001b: USB0_VBUS 010010b: USB0_VBUSEN 010011b: USB0_OVRCURB	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTIOC3D 000101b: TMO2 000111b: RTCOUT(Note 1) 001000b: ADTRG0# 001010b: TXD1/SMOSI1/SSDA1 001011b: RXD3/SMISO3/SSCL3 001101b: MOSIA 001111b: SCL2
P17PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000011b: TIOCB0 000100b: TCLKD 000101b: TMO1 000110b: PO15 000111b: POE8# 001000b: MTIOC4B 001001b: ADTRG1# 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001111b: SDA2-DS 011010b: SDHI_D3-C 001100b: PIXD3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTIOC3B 000101b: TMO1 000111b: POE8# 001000b: MTIOC4B 001010b: SCK1 001011b: TXD3/SMOSI3/SSDA3 001101b: MISOA 001111b: SDA2 011110b: COMP2

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 2 to 7)
P1nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P10: IRQ0 (177/176-pin) P11: IRQ1 (177/176-pin) P12: IRQ2 (177/176/145/144/100/64-pin) P13: IRQ3 (177/176/145/144/100/64-pin) P14: IRQ4 (177/176/145/144/100-pin) P15: IRQ5 (177/176/145/144/100-pin) P16: IRQ6 (177/176/145/144/100/64-pin) P17: IRQ7 (177/176/145/144/100/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P12: IRQ2 (144/100/80-pin) P13: IRQ3 (144/100/80-pin) P14: IRQ4 (144/100/80/64/48-pin) P15: IRQ5 (144/100/80/64/48-pin) P16: IRQ6 (144/100/80/64/48-pin) P17: IRQ7 (144/100/80/64/48-pin)
	ASEL	—	Analog function select bit

Note 1. Not available on products without a sub-clock oscillator.
Note 2. Not supported on 80-pin products.

Table 2.30 Comparison of P2n Pin Function Control Registers (P2nPFS)

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
P20PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000011b: TIOCB3 000101b: TMRI0 000110b: PO0 001010b: TXD0/SMOSI0/SSDA0 010011b: USB0_ID 001111b: SDA1(Note 2) 011010b: SDHI_CMDC(Note 1) (Note 2) 011100b: PIXD4(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1A 000101b: TMRI0 001010b: TXD0/SMOSI0/SSDA0
P21PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000011b: TIOCA3 000101b: TMCI0 000110b: PO1 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0 010011b: USB0_EXICEN 001111b: SCL1(Note 2) 011010b: SDHI_CLK-C(Note 1) (Note 2) 011100b: PIXD5(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC1B 000101b: TMCI0 001000b: MTIOC4A 001010b: RXD0/SMISO0/SSCL0

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
P22PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000011b: TIOCC3 000101b: TMO0 000110b: PO2 001010b: SCK0 010011b: USB0_OVRC URB 011000b: EDREQ0 011010b: SDHI_D0-C(Note 1) (Note 2) 011100b: PIXD6(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKC 000101b: TMO0 001010b: SCK0
P23PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 000011b: TIOCD3 000110b: PO3 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0# 011000b: EDACK0 011010b: SDHI_D1-C(Note 1) (Note 2) 011100b: PIXD7(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKD 001010b: TXD3/SMOSI3/SSDA3 001011b: CTS0#/RTS0#/SS0#
P24PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000011b: TIOCB4 000101b: TMRI1 000110b: PO4 001010b: SCK3 010011b: USB0_VBUS EN 011000b: EDREQ1 011010b: SDHI_WP(Note 1) (Note 2) 011100b: PIXCLK(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000010b: MTCLKA 000101b: TMRI1 001010b: SCK3
P25PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 000011b: TIOCA4 000110b: PO5 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3 011000b: EDACK1 011010b: SDHI_CD(Note 1) (Note 2) 011100b: HSYNC(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTCLKB 001001b: ADTRG0# 001010b: RXD3/SMISO3/SSCL3

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
P26PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 000110b: PO6 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3# 001101b: MOSIB-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000101b: TMO1 001010b: TXD1/SMOSI1/SSDA1 001011b: CTS3#/RTS3#/SS3#
P27PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 000110b: PO7 001010b: SCK1 001101b: RSPCKB-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2B 000101b: TMCI3 001010b: SCK1
P2nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (177/176/145/144/100-pin) P21: IRQ9 (177/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P20: IRQ8 (144/100/80-pin) P21: IRQ9 (144/100/80-pin) P22: IRQ15 (144/100-pin) P23: IRQ3 (144/100-pin) P24: IRQ12 (144/100-pin) P25: IRQ5 (144/100-pin) P26: IRQ6 (144/100/80/64/48-pin) P27: RQ7 (144/100/80/64/48-pin)
	ASEL	—	Analog function select bit

Note 1. This setting is not supported by 100-pin products.

Note 2. Products with code flash memory capacity of 1 MB or less are not supported.

Table 2.31 Comparison of P3n Pin Function Control Registers (P3nPFS)

Register	Bit	RX65N (n = 0 to 4)	RX660 (n = 0 to 4, 6, or 7)
P30PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000110b: PO8 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 001101b: MISOB-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMRI3 000111b: POE8# 001010b: RXD1/SMISO1/SSCL1 011110b: COMP3
P31PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 000110b: PO9 001011b: CTS1#/RTS1#/SS1# 001101b: SSLB0-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMCI2 001011b: CTS1#/RTS1#/SS1#
P32PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000011b: TIOCC0 000101b: TMO3 000110b: PO10 000111b: RTCOUT 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 010011b: USB0_VBUSEN 011100b: VSYNC(Note 2) 100001b: POE10#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000101b: TMO3 000111b: RTCOUT(Note 1) 001000b: POE0# 001010b: TXD6/SMOSI6/SSDA6 001011b: TXD0/SMOSI0/SSDA0 010000b: CTX0 100001b: POE10#
P33PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000011b: TIOCD0 000101b: TMRI3 000110b: PO11 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 011000b: EDREQ1 011100b: PCKO(Note 2) 100001b: POE11#	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000101b: TMRI3 001000b: POE4# 001010b: RXD6/SMISO6/SSCL6 001011b: RXD0/SMISO0/SSCL0 010000b: CRX0 100001b: POE11#

Register	Bit	RX65N (n = 0 to 4)	RX660 (n = 0 to 4, 6, or 7)
P34PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000110b: PO12 000111b: POE10# 001010b: SCK6 001011b: SCK0 010001b: ET0_LINKSTA	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000101b: TMCI3 000111b: POE10# 001010b: SCK6 001011b: SCK0
P3nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (177/176/145/144/100/64-pin) P31: IRQ1-DS (177/176/145/144/100/64-pin) P32: IRQ2-DS (177/176/145/144/100-pin) P33: IRQ3-DS (177/176/145/144/100-pin) P34: IRQ4 (177/176/145/144/100/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P30: IRQ0-DS (144/100/80/64/48-pin) P31: IRQ1-DS (144/100/80/64/48-pin) P32: IRQ2-DS (144/100/80/64-pin) P33: IRQ3-DS (144/100-pin) P34: IRQ4 (144/100/80-pin) P36: IRQ5 (144/100/80/64/48-pin) P37: IRQ4 (144/100/80/64/48-pin)

Note 1. Not available on products without a sub-clock oscillator.
Note 2. This setting is not supported by 100-pin products.

Table 2.32 Comparison of P5n Pin Function Control Registers (P5nPFS)

Register	Bit	RX65N (n = 0 to 2, 4 to 7)	RX660 (n = 0 to 6)
P50PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: TXD2/SMOSI2/SSDA2 001101b: SSLB1-A	Pin function select bits 000000b: Hi-Z 001010b: TXD2/SMOSI2/SSDA2
P51PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: SCK2 001101b: SSLB2-A	Pin function select bits 000000b: Hi-Z 001010b: SCK2
P52PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001010b: RXD2/SMISO2/SSCL2 001101b: SSLB3-A	Pin function select bits 000000b: Hi-Z 001010b: RXD2/SMISO2/SSCL2
P53PFS	PSEL[5:0]	—	P53 pin function select bits

Register	Bit	RX65N (n = 0 to 2, 4 to 7)	RX660 (n = 0 to 6)
P54PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 001101b: MOSIC-B 010000b: CTX1 010001b: ET0_LINKSTA 011000b: EDACK0 100101b: LCD_DATA6-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000101b: TMCI1 001011b: CTS2#/RTS2#/SS2# 010000b: CTX0
P55PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMO3 001010b: TXD7/SMOSI7/SSDA7 001101b: MISOC-B 010000b: CRX1 010001b: ET0_EXOUT 011000b: EDREQ0 100101b: LCD_DATA5-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000101b: TMO3
P56PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TIOCA1 001010b: SCK7 001101b: RSPCKC-B 011000b: EDACK1 100101b: LCD_DATA4-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: SCK7
P57PFS	PSEL[5:0]	P57 pin function select bits	—
P5nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P55: IRQ10 (177/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P50: IRQ0 (144/100-pin) P51: IRQ1 (144/100-pin) P52: IRQ2 (144/100-pin) P53: IRQ3 (144/100-pin) P54: IRQ4 (144/100/80/64-pin) P55: IRQ10 (144/100/80/64-pin) P56: IRQ6 (144-pin)

Table 2.33 Comparison of P6n Pin Function Control Registers (P6nPFS)

Register	Bit	RX65N (n = 6, 7)	RX660 (n = 0 to 7)
P60PFS	PSEL[5:0]	—	P60 pin function control register
P61PFS	PSEL[5:0]	—	P61 pin function control register
P6nPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P67: IRQ15 (177/176/145/144-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin P60: IRQ0 (144-pin) P61: IRQ1 (144-pin) P62: IRQ2 (144-pin) P63: IRQ3 (144-pin) P64: IRQ4 (144-pin) P65: IRQ13 (144-pin) P66: IRQ14 (144-pin) P67: IRQ15 (144-pin)

Table 2.34 Comparison of P7n Pin Function Control Registers (P7nPFS)

Register	Bit	RX65N (n = 1 to 7)	RX660 (n = 0 to 7)
P70PFS	PSEL[5:0]	—	P70 pin function control register
P71PFS	PSEL[5:0]	P71 pin function control register	—
P72PFS	PSEL[5:0]	P72 pin function control register	—
P73PFS	PSEL[5:0]	P73 pin function control register	—
P74PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000110b: PO19 001011b: CTS11#/SS11# 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA21-A(Note 1) (Note 2)	Pin function control register 000000b: Hi-Z 001011b: CTS11#/SS11# 101101b: CTS011#/SS011#
P75PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000110b: PO20 001010b: SCK11 001011b: RTS11# 010001b: ET0_ERXD0 010010b: RMII0_RXD0 011001b: MMC_RES#-A 011010b: SDHI_D2-A 100011b: SDSI_D2 100101b: LCD_DATA20-A(Note 1) (Note 2)	Pin function control register 000000b: Hi-Z 001010b: SCK11 001011b: RTS11# 101100b: SCK011 101101b: RTS011# 101110b: DE011

Register	Bit	RX65N (n = 1 to 7)	RX660 (n = 0 to 7)
P76PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000110b: PO22 001010b: RXD11/SMISO11/SSCL11 010001b: ET0_RX_CLK 010010b: REF50CK0 011001b: MMC_CMD-A 011010b: SDHI_CMD-A 011011b: QSSL-A 100011b: SDSI_CMD 100101b: LCD_DATA18-A(Note 1) (Note 2)	Pin function control register 000000b: Hi-Z 001010b: RXD11/SMISO11/SSCL11 001011b: RXD011/SMISO011/ SSCL011 101100b: TXD011/SMOSI011/ SSDA011
P77PFS	PSEL[5:0]	Pin function control register 000000b: Hi-Z 000110b: PO23 001010b: TXD11/SMOSI11/SSDA11 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 011001b: MMC_CLK-A 011010b: SDHI_CLK-A 011011b: QSPCLK-A 100011b: SDSI_CLK 100101b: LCD_DATA17-A(Note 1) (Note 2)	Pin function control register 000000b: Hi-Z 001010b: TXD11/SMOSI11/SSDA11 101100b: TXD011/SMOSI011/ SSDA011
P7nPFS	ISEL	—	Interrupt input function select bit

Note 1. This setting is not supported by 145/144-pin products.
Note 2. Products with code flash memory capacity of 1 MB or less are not supported.

Table 2.35 Comparison of P8n Pin Function Control Registers (P8nPFS)

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 3, 6, or 7)
P80PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000110b: PO26 001010b: SCK10 001011b: RTS10# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 011000b: EDREQ0 011001b: MMC_D2-A 011010b: SDHI_WP 011011b: QIO2-A 100101b: LCD_DATA1 4-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 001010b: SCK10 001011b: RTS10# 101100b: SCK010 101101b: RTS010# 101110b: DE010
P81PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000110b: PO27 001010b: RXD10/SMISO10/SSCL10 010001b: ET0_ETXD0 010010b: RMII0_TXD0 011000b: EDACK0 011001b: MMC_D3-A 011010b: SDHI_CD 011011b: QIO3-A 100101b: LCD_DATA1 3-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010
P82PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO28 001010b: TXD10/SMOSI10/SSDA10 010001b: ET0_ETXD1 010010b: RMII0_TXD1 011000b: EDREQ1 011001b: MMC_D4-A 100101b: LCD_DATA1 2-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 001010b: TXD10/SMOSI10/SSDA10 101100b: TXD010/SMOSI010/ SSDA010

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 3, 6, or 7)
P83PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: CTS10#/SS10# 010001b: ET0_CRS 010010b: RMII0_CRS_DV 011000b: EDACK1 100101b: LCD_DATA8A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001010b: SCK10 001011b: CTS10#/SS10# 101100b: SCK010 101101b: CTS010#/SS010#
P84PFS	PSEL[5:0]	P84 pin function select bits	—
P85PFS	PSEL[5:0]	P85 pin function select bits	—
P86PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA0 001000b: MTIOC4D 001010b: RXD10/SMISO10/SSCL10 011100b: PIXD1	Pin function select bits 000000b: Hi-Z 001000b: MTIOC4D 001010b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010
P87PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA2 001000b: MTIOC4C 001010b: TXD10/SMOSI10/SSDA10 011100b: PIXD2 011010b: SDHI_D2-C	Pin function select bits 000000b: Hi-Z 001000b: MTIOC4C 001010b: TXD10/SMOSI10/SSDA10 101100b: TXD010/SMOSI010/ SSDA010
P8nPFS	ISEL	—	Interrupt input function select bit

Table 2.36 Comparison of P9n Pin Function Control Registers (P9nPFS)

Register	Bit	RX65N (n = 0 to 3)	RX660 (n = 0 to 3)
P9nPFS	ISEL	—	Interrupt input function select bit
	ASEL	Analog input function select bit	—

Table 2.37 Comparison of PAn Pin Function Control Registers (PAnPFS)

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PA0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000011b: TIOCA0 000110b: PO16 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1-B 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100101b: LCD_DATA8-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000111b: CACREF 001000b: MTIOC6D 001101b: SSLA1
PA1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 000011b: TIOCB0 000110b: PO17 001000b: MTIOC7B 001010b: SCK5 001101b: SSLA2-B 010001b: ET0_WOL 100101b: LCD_DATA7-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0B 000010b: MTCLKC 001000b: MTIOC7B 001001b: ADTRG0# 001010b: SCK5 001100b: SCK12 001101b: SSLA2 100111b: MTIOC3B
PA2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000110b: PO18 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-B 100101b: LCD_DATA6-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC7A 001010b: RXD5/SMISO5/SSCL5 001100b: RXD12/SMISO12/SSCL12/ RXDX12 001101b: SSLA3
PA3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 000011b: TIOCD0 000100b: TCLKB 000110b: PO19 001010b: RXD5/SMISO5/SSCL5 010001b: ET0_MDIO 100101b: LCD_DATA5-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0D 000010b: MTCLKD 001000b: MTIC5V 001010b: RXD5/SMISO5/SSCL5 100111b: MTIOC4D

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PA4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000011b: TIOCA1 000101b: TMRI0 000110b: PO20 001010b: TXD5/SMOSI5/SSDA5 001101b: SSLA0-B 010001b: ET0_MDC 100101b: LCD_DATA4-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000010b: MTCLKA 000101b: TMRI0 001000b: MTIOC4C 001001b: ADST0 001010b: TXD5/SMOSI5/SSDA5 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: SSLA0 100111b: MTIOC7C
PA5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCB1 000110b: PO21 001000b: MTIOC6B 001101b: RSPCKA-B 010001b: ET0_LINKST A 100101b: LCD_DATA3-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6B 001101b: RSPCKA
PA6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000011b: TIOCA2 000101b: TMCI3 000110b: PO22 000111b: POE10# 001011b: CTS5#/RTS5#/SS5# 001101b: MOSIA-B 010001b: ET0_EXOUT 100101b: LCD_DATA2-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000010b: MTCLKB 000101b: TMCI3 000111b: POE10# 001000b: MTIOC3D 001011b: CTS5#/RTS5#/SS5# 001100b: CTS12#/RTS12#/SS12# 001101b: MOSIA 100111b: MTIOC6B
PA7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCB2 000110b: PO23 001101b: MISOA-B 010001b: ET0_WOL 100101b: LCD_DATA1-B	Pin function select bits 000000b: Hi-Z 001101b: MISOA

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PAnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA1: IRQ11 (177/176/145/144/100/64-pin) PA3: IRQ6-DS (177/176/145/144/100-pin) PA4: IRQ5-DS (177/176/145/144/100/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PA0: IRQ0 (144/100/80/64-pin) PA1: IRQ11 (144/100/80/64/48-pin) PA2: IRQ10 (144/100/80-pin) PA3: IRQ6-DS (144/100/80/64/48-pin) PA4: IRQ5-DS (144/100/80/64/48-pin) PA5: IRQ5 (144/100/80-pin) PA6: IRQ14 (144/100/80/64/48-pin) PA7: IRQ7 (144/100-pin)
PAnPFS	ASEL	—	Analog function select bit

Table 2.38 Comparison of PBn Pin Function Control Registers (PBnPFS)

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PB0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000011b: TIOCA3 000110b: PO24 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 010001b: ET0_ERXD1 010010b: RMII0_RXD1 100101b: LCD_DATA0-B(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000010b: MTIOC3D 001010b: RXD4/SMISO4/SSCL4 001011b: RXD6/SMISO6/SSCL6 001101b: RSPCKA
PB1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000011b: TIOCB3 000101b: TMCI0 000110b: PO25 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 010001b: ET0_ERXD0 010010b: RMII0_RXD0 100101b: LCD_TCON3-B(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0C 000010b: MTIOC4C 000101b: TMCI0 001010b: TXD4/SMOSI4/SSDA4 001011b: TXD6/SMOSI6/SSDA6 011110b: COMP1

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PB2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCC3 000100b: TCLKC 000110b: PO26 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6# 010001b: ET0_RX_CL K 010010b: REF50CK0 100011b: SDSI_D2 100101b: LCD_TCON2-B(Note 1)	Pin function select bits 000000b: Hi-Z 001010b: CTS4#/RTS4#/SS4# 001011b: CTS6#/RTS6#/SS6#
PB3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000011b: TIOCD3 000100b: TCLKD 000101b: TMO0 000110b: PO27 000111b: POE11# 001010b: SCK4 001011b: SCK6 010001b: ET0_RX_ER 010010b: RMII0_RX_ER 100011b: SDSI_D3 100101b: LCD_TCON1-B(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC0A 000010b: MTIOC4A 000101b: TMO0 000111b: POE11# 001010b: SCK4 001011b: SCK6 011101b: TIC2 100110b: PMC0
PB4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000011b: TIOCA4 000110b: PO28 001011b: CTS9#/RTS9#/SS9# 010001b: ET0_TX_EN 010010b: RMII0_TXD_EN 100011b: SDSI_CMD 100100b: CTS11#/RTS11#/SS11# 100101b: LCD_TCON0-B(Note 1)	Pin function select bits 000000b: Hi-Z 001011b: CTS9#/RTS9#/SS9# 100100b: CTS11#/RTS11#/SS11# 101100b: CTS011#/RTS011#/SS011# 101110b: DE011

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PB5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000011b: TIOCB4 000101b: TMRI1 000110b: PO29 000111b: POE4# 001010b: SCK9 010001b: ET0_ETXD0 010010b: RMII0_TXD0 100011b: SDSI_CLK 100100b: SCK11 100101b: LCD_CLK-B(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC2A 000010b: MTIOC1B 000101b: TMRI1 000111b: POE4# 001010b: SCK9 011101b: TOC2 100100b: SCK11 101100b: SCK011
PB6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000011b: TIOCA5 000110b: PO30 001010b: RXD9/SMISO9/SSCL9 010001b: ET0_ETXD1 010010b: RMII0_TXD1 100011b: SDSI_D0 100100b: RXD11/SMISO11/SSCL11	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 001010b: RXD9/SMISO9/SSCL9 100100b: RXD11/SMISO11/SSCL11 101100b: RXD011/SMISO011/ SSCL011
PB7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000011b: TIOCB5 000110b: PO31 001010b: TXD9/SMOSI9/SSDA9 010001b: ET0_CRS 010010b: RMII0_CRS_DV 100011b: SDSI_D1 100100b: TXD11/SMOSI11/SSDA11	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 001010b: TXD9/SMOSI9/SSDA9 100100b: TXD11/SMOSI11/SSDA11 101100b: TXD011/SMOSI011/ SSDA011

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PBnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (177/176/145/144/100-pin) PB1: IRQ4-DS (177/176/145/144/100-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PB0: IRQ12 (144/100/80/64/48-pin) PB1: IRQ4-DS (144/100/80/64/48-pin) PB2: IRQ2 (144/100/80-pin) PB3: IRQ3 (144/100/80/64/48-pin) PB4: IRQ4 (144/100/80-pin) PB5: IRQ13 (144/100/80/64/48-pin) PB6: IRQ6 (144/100/80/64-pin) PB7: IRQ15 (144/100/80/64-pin)

Note 1. Products with code flash memory capacity of 1 MB or less are not supported.

Table 2.39 Comparison of PCn Pin Function Control Registers (PCnPFS)

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PC0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000011b: TCLKC 000110b: PO17 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1-A 010001b: ET0_ERXD3	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001011b: CTS5#/RTS5#/SS5# 001101b: SSLA1 101100b: RXD011/SMISO011/ SSCL011
PC1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000011b: TCLKD 000110b: PO18 001010b: SCK5 001101b: SSLA2-A 010001b: ET0_ERXD2 100101b: LCD_DATA2-A(Note 2) (Note 3)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 001010b: SCK5 001101b: SSLA2 101100b: TXD011/SMOSI011 SSDA011/TXDA011

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PC2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000011b: TCLKA 000110b: PO21 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3-A 010001b: ET0_RX_DV 011001b: MMC_CD-A(Note 1) 011010b: SDHI_D3-A(Note 1) 100011b: SDSI_D3(Note 1) 100101b: LCD_DATA19-A(Note 2) (Note 3)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001010b: RXD5/SMISO5/SSCL5 001101b: SSLA3 101100b: TXDB011
PC3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000011b: TCLKB 000110b: PO24 001010b: TXD5/SMOSI5/SSDA5 010001b: ET0_TX_ER 011001b: MMC_D0-A(Note 1) 011010b: SDHI_D0-A(Note 1) 011011b: QIO0-A/QMO-A 100011b: SDSI_D0(Note 1) 100101b: LCD_DATA16-A(Note 2) (Note 3)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001010b: TXD5/SMOSI5/SSDA5 100110b: PMC0
PC4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000110b: PO25 000111b: POE0# 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0-A 010001b: ET0_TX_CLK 011001b: MMC_D1-A(Note 1) 011010b: SDHI_D1-A(Note 1) 011011b: QIO1-A/QMI-A 100011b: SDSI_D1(Note 1) 100100b: CTS10#/RTS10#/SS10# 100101b: LCD_DATA15-A(Note 2) (Note 3)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3D 000010b: MTCLKC 000101b: TMCI1 000111b: POE0# 001000b: MTIOC0A 001010b: SCK5 001011b: CTS8#/RTS8#/SS8# 001101b: SSLA0 100100b: CTS10#/RTS10#/SS10# 100110b: PMC0 101100b: CTS010#/RTS010#/SS010# 101110b: DE010

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PC5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 000110b: PO29 001010b: SCK8 001101b: RSPCKA-A 010001b: ET0_ETXD2 011001b: MMC_D5-A(Note 1) 100100b: SCK10 100101b: LCD_DATA11-A(Note 2) (Note 3)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3B 000010b: MTCLKD 000101b: TMRI2 001000b: MTIOC0C 001010b: SCK8 001101b: RSPCKA 100100b: SCK10 100110b: PMC0 101100b: SCK010
PC6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 000110b: PO30 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA-A 010001b: ET0_ETXD3 011001b: MMC_D6-A(Note 1) 011101b: TIC0 100100b: RXD10/SMISO10/SSCL10 100101b: LCD_DATA10-A(Note 2) (Note 3)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 000010b: MTCLKA 000101b: TMCI2 001010b: RXD8/SMISO8/SSCL8 001101b: MOSIA 011101b: TIC0 100100b: RXD10/SMISO10/SSCL10 101100b: RXD010/SMISO010/ SSCL010
PC7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000110b: PO31 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA-A 010001b: ET0_COL 011001b: MMC_D7-A(Note 1) 011101b: TOC0 100100b: TXD10/SMOSI10/SSDA10 100101b: LCD_DATA9-A(Note 2) (Note 3)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A 000010b: MTCLKB 000101b: TMO2 000111b: CACREF 001010b: TXD8/SMOSI8/SSDA8 001101b: MISOA 011101b: TOC0 100100b: TXD10/SMOSI10/SSDA10 101100b: TXD010/SMOSI010/ SSDA010

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PCnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (177/176/145/144/100/64-pin) PC1: IRQ12 (177/176/145/144/100/64-pin) PC6: IRQ13 (177/176/145/144/100/64-pin) PC7: IRQ14 (177/176/145/144/100/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PC0: IRQ14 (144/100-pin) PC1: IRQ12 (144/100-pin) PC2: IRQ10 (144/100/80/64-pin) PC3: IRQ11 (144/100/80/64-pin) PC4: IRQ12 (144/100/80/64/48-pin) PC5: IRQ5 (144/100/80/64/48-pin) PC6: IRQ13 (144/100/80/64/48-pin) PC7: IRQ14 (144/100/80/64/48-pin)

Note 1. This setting is not supported by 100-pin products.
Note 2. This setting is not supported by 145/144/100-pin products.
Note 3. Products with code flash memory capacity of 1 MB or less are not supported.

Table 2.40 Comparison of PDn Pin Function Control Registers (PDnPFS)

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PD0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: POE4# 100101b: LCD_EXTCLK-B	Pin function select bits 000000b: Hi-Z 001000b: POE4#
PD1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 001101b: MOSIC-A 010000b: CTX0 100101b: LCD_DATA23-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 001000b: POE0# 010000b: CTX0
PD2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 001101b: MISOC-A 010000b: CRX0 011001b: MMC_D2-B 011010b: SDHI_D2-B 011011b: QIO2-B 011101b: TIC2 100101b: LCD_DATA22-B	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 010000b: CRX0 011101b: TIC2

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PD3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 001101b: RSPCKC-A 011001b: MMC_D3-B 011010b: SDHI_D3-B 011011b: QIO3-B 011101b: TOC2 100101b: LCD_DATA21-B	Pin function select bits 000000b: Hi-Z 000111b: POE8# 001000b: MTIOC8D 011101b: TOC2
PD4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B 001101b: SSLC0-A 011001b: MMC_CMDB 011010b: SDHI_CMDB 011011b: QSSL-B 100101b: LCD_DATA20-B	Pin function select bits 000000b: Hi-Z 000111b: POE11# 001000b: MTIOC8B
PD5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C 001101b: SSLC1-A 011001b: MMC_CLK-B 011010b: SDHI_CLK-B 011011b: QSPCLK-B 100101b: LCD_DATA19-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5W 000111b: POE10# 001000b: MTIOC8C
PD6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A 001101b: SSLC2-A 011001b: MMC_D0-B 011010b: SDHI_D0-B 011011b: QIO0-B/QMO-B 100101b: LCD_DATA18-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5V 000111b: POE4# 001000b: MTIOC8A

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PD7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0# 001101b: SSLC3-A 011001b: MMC_D1-B 011010b: SDHI_D1-B 011011b: QIO1-B/QMI-B 100101b: LCD_DATA17-B	Pin function select bits 000000b: Hi-Z 000001b: MTIC5U 000111b: POE0#
PDnPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN108 (177/176/145/144/100-pin) PD1: AN109 (177/176/145/144/100-pin) PD2: AN110 (177/176/145/144/100/64-pin) PD3: AN111 (177/176/145/144/100/64-pin) PD4: AN112 (177/176/145/144/100/64-pin) PD5: AN113 (177/176/145/144/100/64-pin) PD6: AN106 (177/176/145/144/100/64-pin) PD7: AN107 (177/176/145/144/100/64-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PD0: AN016 (144/100/80-pin) PD1: AN017 (144/100/80-pin) PD2: AN018 (144/100/80-pin) PD3: AN019 (144/100-pin) PD4: AN020 (144/100-pin) PD5: AN021 (144/100-pin) PD6: AN022 (144/100-pin) PD7: AN023 (144/100-pin)

Table 2.41 Comparison of PEn Pin Function Control Registers (PEnPFS)

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PE0PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12 001101b: SSLB1-B 011001b: MMC_D4-B 100101b: LCD_DATA16-B	Pin function select bits 000000b: Hi-Z 001000b: MTIOC3D 001100b: SCK12
PE1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000110b: PO18 001000b: MTIOC3B 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12 001101b: SSLB2-B 011001b: MMC_D5-B 100101b: LCD_DATA15-B(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 001000b: MTIOC3B 001100b: TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12
PE2PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 000110b: PO23 001100b: RXD12/SMISO12/ SSCL12/RXDX12 001101b: SSLB3-B 011001b: MMC_D6-B 011101b: TIC3 100101b: LCD_DATA14-B(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4A 001000b: MTIOC7A 001100b: RXD12/SMISO12/ SSCL12/RXDX12 011101b: TIC3
PE3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000110b: PO26 000111b: POE8# 001100b: CTS12#/RTS12#/SS12# 010001b: ET0_ERXD3 011001b: MMC_D7-B 011101b: TOC3 100101b: LCD_DATA13-B(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4B 000111b: POE8# 001000b: MTIOC1B 001100b: CTS12#/RTS12#/SS12# 011101b: TOC3

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PE4PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 000110b: PO28 001101b: SSLB0-B 010001b: ET0_ERXD2 100101b: LCD_DATA12-B(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4D 000010b: MTIOC1A 001000b: MTIOC4A 100111b: MTIOC7D
PE5PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 001101b: RSPCKB-B 010001b: ET0_RX_CLK 010010b: REF50CK0 100101b: LCD_DATA11-B(Note 1)	Pin function select bits 000000b: Hi-Z 000001b: MTIOC4C 000010b: MTIOC2B 011110b: COMP0
PE6PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001101b: MOSIB-B 011001b: MMC_CD-B 011010b: SDHI_CD 011101b: TIC1 100101b: LCD_DATA10-B(Note 1)	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6C 001010b: CTS4#/RTS4#/SS4# 011101b: TIC1
PE7PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 001101b: MISOB-B 011001b: MMC_RES#B 011010b: SDHI_WP 011101b: TOC1 100101b: LCD_DATA9B(Note 1)	Pin function select bits 000000b: Hi-Z 001000b: MTIOC6A 001010b: CTS4#/RTS4#/SS4# 011101b: TOC1

Register	Bit	RX65N (n = 0 to 7)	RX660 (n = 0 to 7)
PEnPFS	ISEL	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE2: IRQ7-DS (177/176/145/144/100/64-pin) PE5: IRQ5 (177/176/145/144/100-pin) PE6: IRQ6 (177/176/145/144/100/64-pin) PE7: IRQ7 (177/176/145/144/100/64-pin)	Interrupt input function select bit 0: Not used as IRQn input pin 1: Used as IRQn input pin PE0: IRQ8 (144/100/80/64-pin) PE1: IRQ9 (144/100/80/64/48-pin) PE2: IRQ7-DS (144/100/80/64/48-pin) PE3: IRQ11 (144/100/80/64/48-pin) PE4: IRQ12 (144/100/80/64/48-pin) PE5: IRQ5 (100/80/64-pin) PE6: IRQ6 (144/100-pin) PE7: IRQ7 (144/100-pin)
PEnPFS	ASEL	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: ANEX0 (177/176/145/144/100/64-pin) PE1: ANEX1 (177/176/145/144/100/64-pin) PE2: AN100 (177/176/145/144/100-pin) PE3: AN101 (177/176/145/144/100-pin) PE4: AN102 (177/176/145/144/100-pin) PE5: AN103 (177/176/145/144/100-pin) PE6: AN104 (177/176/145/144/100-pin) PE7: AN105 (177/176/145/144/100-pin)	Analog function select bit 0: Used as other than as analog pin 1: Used as analog pin PE0: AN008 (144/100/80/64-pin) PE1: AN009 (144/100/80/64/48-pin) PE2: AN010 (144/100/80/64/48-pin) PE3: AN011 (144/100/80/64/48-pin) PE4: AN012 (144/100/80/64/48-pin) PE5: AN013 (144/100/80/64-pin) PE6: AN014 (144/100-pin) PE7: AN015 (144/100-pin)

Note 1. Products with code flash memory capacity of 1 MB or less are not supported.

Table 2.42 Comparison of PF5 Pin Function Control Registers (PF5PFS)

Register	Bit	RX65N (n = 0 to 2.5)	RX660
PFnPFS	PSEL[5:0]	PFn pin function select bits	—

Table 2.43 Comparison of PHn Pin Function Control Register (PHnPFS)

Register	Bit	RX65N	RX660 (n=0 to 3)
PHnPFS	—	—	PHn pin function control register

Table 2.44 Comparison of PJn Pin Function Control Registers (PJnPFS)

Register	Bit	RX65N (n = 0 to 3.5)	RX660 (n = 1, 3, or 5)
PJ0PFS	PSEL[5:0]	PJ0 pin function select bits	—
PJ1PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC6A 001010b: RXD8/SMISO8/SSCL8 001101b: SSLC2-B 100101b: LCD_TCON3-A	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3A
PJ2PFS	PSEL[5:0]	PJ2 pin function control register	—
PJ3PFS	PSEL[5:0]	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0# 010001b: ET0_EXOUT 011000b: EDACK1	Pin function select bits 000000b: Hi-Z 000001b: MTIOC3C 001010b: CTS6#/RTS6#/SS6# 001011b: CTS0#/RTS0#/SS0#
PJnPFS	ISEL	—	Interrupt input function select bit

Table 2.45 Comparison of PKn Pin Function Control Registers (PKnPFS)

Register	Bit	RX65N	RX660 (n = 2 to 5)
PKnPFS	—	—	PKn pin function control register

Table 2.46 Comparisons of Multi-Function Pin Controller Registers

Register	Bit	RX65N	RX660
PFCSE	CS4E to CS7E	CSn enable bit	—
PFCSS0	CS0S (RX65N) CS1S[1:0] (RX660)	CS0# output pin select bits 0: P60 is set as CS0# output pin. 1: PC7 is set as CS0# output pin.	CS0# output pin select bits b1 b0 0 0: P24 is set as CS0# output pin. 0 1: P60 is set as CS0# output pin. 1 x: PC7 is set as CS0# output pin.
	CS1S[1:0]	CS1# output pin select bits b3 b2 0 0: P61 is set as CS1# output pin. 0 1: P71 is set as CS1# output pin. 1 x: PC6 is set as CS1# output pin.	CS1# output pin select bits b3 b2 0 0: P25 is set as CS1# output pin. 0 1: P61 is set as CS1# output pin. 1 0: P71 is set as CS1# output pin. 1 1: PC6 is set as CS1# output pin.
	CS2S[1:0]	CS2# output pin select bits b5 b4 0 0: P62 is set as CS2# output pin. 0 1: P72 is set as CS2# output pin. 1 x: PC5 is set as CS2# output pin.	CS2# output pin select bits b5 b4 0 0: P26 is set as CS2# output pin. 0 1: P62 is set as CS2# output pin. 1 0: P72 is set as CS2# output pin. 1 1: PC5 is set as CS2# output pin.
	CS3S[1:0]	CS3# output pin select bits b7 b6 0 0: P63 is set as CS3# output pin. 0 1: P73 is set as CS3# output pin. 1 x: PC4 is set as CS2# output pin.	CS3# output pin select bits b7 b6 0 0: P27 is set as CS3# output pin. 0 1: P63 is set as CS3# output pin. 1 0: P73 is set as CS3# output pin. 1 1: PC4 is set as CS3# output pin.
PFCSS1	—	CS output pin select register 1	—
PFAOE1	A21E to A23E	Address output enable bit	—
PFBCR0	DH32E	D16 to D31 output enable bit	—
	WR32BC32E	WR3#/BC3# or WR2#/BC2# output enable bit	—
PFBCR1	ALES	ALE select bit	—
	MDSDE	SDRAM pin enable bit	—
	DQM1E	DQM1 enable bit	—
	SDCLKE	SDCLK enable bit	—
PFENET	—	Ethernet control register	—

2.14 Port Output Enable 3

Table 2.47 is a Comparison of Port Output Enable 3 Registers.

Table 2.47 Comparison of Port Output Enable 3 Registers

Register	Bit	RX65N (POE3a)	RX660 (POE3a)
M6SELR	—	MTU6 pin select register	—

2.15 8-bit timer

Table 2.48 is a Comparative Overview of 8-Bit Timers.

Table 2.48 Comparative Overview of 8-Bit Timers

Item	RX65N (TMRb)	RX660 (TMRb)
Count clocks	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock	• Internal clock: PCLK/1, PCLK/2, PCLK/8, PCLK/32, PCLK/64, PCLK/1,024, PCLK/8,192 • External clock: External count clock
Number of channels	(8 bits × 2 channels) × 2 units	(8 bits × 2 channels) × 2 units
compare match	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)	• 8-bit mode (compare match A, compare match B) • 16-bit mode (compare match A, compare match B)
Counter clear	Selectable among compare match A or B, or an external counter reset signal.	Selectable among compare match A or B, or an external counter reset signal.
Timer output	Output pulses with a user-defined duty cycle or PWM output	Output pulses with a user-defined duty cycle or PWM output
Cascading of two channels	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).	• 16-bit count mode 16-bit timer using TMR0 for the upper 8 bits and TMR1 for the lower 8 bits (TMR2 for the upper 8 bits and TMR3 for the lower 8 bits) • Compare match count mode TMR1 can be used to count TMR0 compare matches (TMR3 can be used to count TMR2 compare matches).
Interrupt sources	Compare match A, compare match B, and overflow	Compare match A, compare match B, and overflow
Event link function (output)	Compare match A, compare match B, and overflow (TMR0 to TMR3)	Compare match A, compare match B, and overflow (TMR0 to TMR3)
Event link function (input)	Ability to perform one of three actions according to accepted event (1) Counter start (TMR0 to TMR3) (2) Event counter (TMR0 to TMR3) (1) Counter restart (TMR0 to TMR3)	Ability to perform one of three actions according to accepted event (3) Counter start (TMR0 to TMR3) (4) Event counter (TMR0 to TMR3) (5) Counter restart (TMR0 to TMR3)
Generation of trigger to start A/D converter	Compare match A of TMR0 or TMR2	Compare match A of TMR0 or TMR2
DTC activation	The DTC can be activated by compare match A interrupts or compare match B interrupts.	The DTC can be activated by compare match A interrupts or compare match B interrupts.
Generation of SCI basic clock	Generation of baud rate clock for SCI	Generation of SCI basic clock
Generation of REMC operation clock	—	Generation of REMC (remote control signal receiver) operation clock
Low power consumption function	Transition to the module stop state is possible for each unit.	Transition to the module stop state is possible for each unit.

2.16 Compare match timer W

Table 2.49 is a Comparative Overview of Compare Match Timer W.

Table 2.49 Comparative Overview of Compare Match Timer W

Item	RX65N (CMTW)	RX660 (CMTW)
Number of channels	2 channels (unit 0 and unit 1)	2 channels (unit 0 and unit 1)
Timer counter	Up counter switchable between 16-bit and 32-bit Returns to 0000 0000h after a compare match.	Up counter switchable between 16-bit and 32-bit Returns to 0000 0000h after a compare match.
Prescaler	Outputs 4 types of divided clocks Selectable from PCLK/8, PCLK/32, PCLK/128, and PCLK/512	Outputs 4 types of divided clocks Selectable from PCLK/8, PCLK/32, PCLK/128, and PCLK/512
Input capture	Up to 2 input capture inputs possible	Up to 2 input capture inputs possible
Output compare	Up to 2 output compare outputs possible	Up to 2 output compare outputs possible
Compare match	1 compare match possible (No output compare output pin)	1 compare match possible (No output compare output pin)
Interrupts	Compare match interrupt Input capture 0 Input capture 1 interrupt Output compare 0 Output compare 1 interrupt	Compare match interrupt Input capture 0 Input capture 1 interrupt Output compare 0 Output compare 1 interrupt
Event link function (output) (unit 0)	Compare match	—
Event link function (input) (unit 0)	Ability to perform one of three actions according to accepted event — Count start operation — Event count operation — Count restart operation	—
Low Power Consumption	Transition to the module stop state is possible for each unit.	Transition to the module stop state is possible for each unit.

2.17 Realtime clock

Table 2.50 is a Comparative Overview of Realtime Clocks, and Table 2.51 is a Comparison of Realtime Clock Registers.

Table 2.50 Comparative Overview of Realtime Clocks

Item	RX65N (RTCd)	RX660 (RTCC)
Count modes	Calendar count mode/ binary count mode	Calendar count mode/ binary count mode
Count source	Sub-clock (XCIN) or main clock (EXTAL)	Sub-clock (XCIN)
Clock and calendar functions	• Calendar count mode Year, month, date, day-of-week, hour, minute, second are counted, BCD display 12 hours/24 hours mode switching function 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) Automatic adjustment function for leap years (compare match A, compare match B) • Binary count mode Count seconds in 32 bits, binary display • Common to both modes Start/stop function The sub-second digit is displayed in binary units (1 Hz, 2 Hz, 4 Hz, 8 Hz, 16 Hz, 32 Hz, 64Hz) • Clock error correction function Clock (1 Hz/64 Hz) output	• Calendar count mode Year, month, date, day-of-week, hour, minute, second are counted, BCD display 12 hours/24 hours mode switching function 30 seconds adjustment function (a number less than 30 is rounded down to 00 seconds, and 30 seconds or more are rounded up to one minute) Automatic adjustment function for leap years (compare match A, compare match B) • Binary count mode Count seconds in 32 bits, binary display Common to both modes Start/stop function The sub-second digit is displayed in binary units (1Hz, 2 Hz, 4Hz, 8Hz, 16 Hz, 32 Hz, 64 Hz) • Clock error correction function Clock (1 Hz/64 Hz) output

Item	RX65N (RTCd)	RX660 (RTCC)
Interrupts	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: - Calendar count mode: Year, month, date, day-of-week, hour, minute, or second - Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second,1/64second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) An interrupt request is generated at either of the following timings: - When a carry from the 64 Hz counter to the second counter is generated. - When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt	• Alarm interrupt (ALM) As an alarm interrupt condition, selectable which of the below is compared with: - Calendar count mode: Year, month, date, day-of-week, hour, minute, or second - Binary count mode: Each bit of the 32-bit binary counter • Periodic interrupt (PRD) 2 seconds, 1 second, 1/2 second, 1/4 second, 1/8 second, 1/16 second, 1/32 second,1/64second, 1/128 second, or 1/256 second can be selected as an interrupt period. • Carry interrupt (CUP) An interrupt request is generated at either of the following timings: - When a carry from the 64 Hz counter to the second counter is generated. - When the 64-Hz counter is changed and the R64CNT register is read at the same time. • Recovery from software standby mode or deep software standby mode can be performed by an alarm interrupt or periodic interrupt
Time-capture function	Times can be captured by detecting an edge of a signal on a time capture event input pin. For every event input, the month, date, hour, minute, and second, or the 32-bit binary counter value, is captured.	Times can be captured by detecting an edge of a signal on a time capture event input pin. For every event input, the month, date, hour, minute, and second, or the 32-bit binary counter value, is captured.
Event link function	Periodic event output	Periodic event output

Table 2.51 Comparison of Realtime Clock Registers

Register	Bit	RX65N (RTCd)	RX660 (RTCC)
RCR3	RTCEN	Sub-clock oscillator control bit 0: Sub-clock oscillator is stopped. 1: Sub-clock oscillator is operating.	RTC enable bit 0: RTC is disabled. 1: RTC is enabled.
	RTCDV[2:0]	Sub-clock oscillator drivability control bit	—
RCR4	RCKSEL	Count source select bit 0: Sub-clock oscillator is selected. 1: Main clock oscillator is selected.	Count source select bit 0: Sub-clock oscillator is selected. 1: Settings prohibited.
RFRH/ RFRL	—	Frequency register H/L	—

2.18 Serial Communications Interface

Table 2.52 is Comparative Overview of Serial Communications Interfaces, Table 2.53 is Comparison of Serial Communications Interface Channel Specifications, and Table 2.54 is Comparison of Serial Communications Interface Registers.

Table 2.52 Comparative Overview of Serial Communications Interfaces

Item		RX65N (SCIg, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Number of channels		• SCIg: 10 channels • SCIi: 2 channel • SCIh: 1 channel	• SCIk: 10 channels • SCIm: 2 channels • SCIh: 1 channel
Serial communications modes		• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus	• Asynchronous • Clock synchronous • Smart card interface • Simple I²C bus • Simple SPI bus
Transfer speed		Bit rate specifiable by on-chip baud rate generator.	Bit rate specifiable by on-chip baud rate generator.
Full-duplex communication		• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.	• Transmitter: Continuous transmission possible using double-buffer structure. • Receiver: Continuous reception possible using double-buffer structure.
Data transfer		Selectable as LSB first or MSB first transfer.	Selectable as LSB first or MSB first transfer.
I/O signal level inversion		—	The levels of input and output signals can be inverted independently.
Interrupt sources		• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and data match • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)	• Transmit end, transmit data empty, receive data full, receive error, receive data ready, and data match • Completion of generation of a start condition, restart condition, or stop condition (for simple I²C mode)
Low power consumption function		Transition to the module stop state is possible for each channel.	Transition to the module stop state is possible for each channel.
Asynchronous mode	Data length	7, 8, or 9 bits	7, 8, or 9 bits
	Transmission stop bits	1 or 2 bits	1 or 2 bits
	Parity	Even parity, odd parity, or no parity	Even parity, odd parity, or no parity
	Receive error detection function	Parity, overrun, and framing errors	Parity, overrun, and framing errors
	Hardware flow control	CTSn# and RTSn# pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)

Item		RX65N (SCIg, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	Data match detection	Compares receive data and comparison data register, and generates an interrupt request when they are matched (SCI11).	Compares receive data and comparison data register, and generates interrupt when they are matched (SCI0 to SCI11).
	Start-bit detection	Low level or falling edge is selectable.	Low level or falling edge is selectable.
	Receive data sampling timing adjustment	—	The receive data sampling point can be shifted from the center of the data forward or backward to a base point.
	Transmit signal change timing adjustment	—	Either the falling or rising edge of the transmit data can be delayed.
	Break detection	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.	When a framing error occurs, a break can be detected by reading the RXDn pin level directly or by reading the SPTR.RXDMON flag.
	Clock source	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).	• An internal or external clock can be selected. • Transfer rate clock input from the TMR can be used (SCI5, SCI6, and SCI12).
	Double-speed mode	Baud rate generator double-speed mode is selectable.	Baud rate generator double-speed mode is selectable.
	Multi-processor communications function	Serial communication among multiple processors	Serial communication among multiple processors
	Noise cancellation	The signal paths from input on the RXDn pins incorporate digital noise filters.	The signal paths from input on the RXDn pins incorporate digital noise filters.
Clock synchronous mode	Data length	8 bits	8 bits
	Receive error detection	Overrun error	Overrun error
	Hardware flow control	CTSn# and RTSn pins can be used in controlling transmission/reception.	CTSn# and RTSn# pins can be used in controlling transmission/reception.
	Transmit/receive FIFO	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)	Ability to use 16-stage FIFOs for transmission and reception (SCI10 and SCI11)
Smart card interface mode	Error processing	• An error signal can be automatically transmitted when detecting a parity error during reception • Data can be automatically retransmitted when receiving an error signal during transmission	• An error signal can be automatically transmitted when detecting a parity error during reception. • Data can be automatically retransmitted when receiving an error signal during transmission.
	Data type	Both direct convention and inverse convention are supported.	Both direct convention and inverse convention are supported.

Item		RX65N (SCIg, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Simple I²C mode	Communication format	I²C bus format	I²C bus format
	Operating mode	Master (single-master operation only)	Master (single-master operation only)
	Transfer speed	Fast mode is supported.	Fast mode is supported.
	Noise cancellation	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.	• The signal paths from input on the SSCLn and SSDAn pins incorporate digital noise filters. • The interval for noise cancellation is adjustable.
Simple SPI mode	Data length	8 bits	8 bits
	Detection of errors	Overrun error	Overrun error
	SS input pin function	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.	Applying the high level to the SSn# pin can cause the output pins to enter the high-impedance state.
	Clock settings	Four kinds of settings for clock phase and clock polarity are selectable.	Four kinds of settings for clock phase and clock polarity are selectable.
Extended serial mode (supported by SCI12 only)	Start frame transmission	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection	• Break field low width output and generation of interrupt on completion • Detection of bus collision and generation of interrupt on detection
	Start frame reception	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates	• Detection of break field low width and generation of interrupt on detection • Data comparison of control fields 0 and 1 and generation of interrupt when they match • Ability to specify two kinds of data for comparison (primary and secondary) in control field 1 • Ability to specify priority interrupt bit in control field 1 • Support for start frames that do not include a break field • Support for start frames that do not include a control field 0 • Function for measuring bit rates
	I/O control function	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin	• Ability to select polarity or TXDX12 and RXDX12 signals • Ability to specify digital filtering of RXDX12 signal • Half-duplex operation employing RXDX12 and TXDX12 signals multiplexed on the same pin • Ability to select receive data sampling timing of RXDX12 pin
	Timer function	Usable as reloading timer	Usable as reloading timer

Item	RX65N (SCIg, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Bit rate modulation function	Correction of outputs from the on-chip baud rate generator can reduce errors.	Correction of outputs from the on-chip baud rate generator can reduce errors.
Event link function (supported by SCI5 only)	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output	• Error (receive error or error signal detection) event output • Receive data full event output • Transmit data empty event output • Transmit end event output

Table 2.53 Comparison of Serial Communications Interface Channel Specifications

Item	RX65N (SCIg, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
Asynchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Clock synchronous mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Smart card interface mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple I^2C mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
Simple SPI mode	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11, SCI12
FIFO mode	SCI10, SCI11	SCI10, SCI11
Data match detection	SCI10, SCI11	SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6, SCI7, SCI8, SCI9, SCI10, SCI11
Extended serial mode	SCI12	SCI12
TMR clock input	SCI5, SCI6, SCI12	SCI5, SCI6, SCI12
Event link function	SCI5	SCI5
Peripheral module clock	PCLKA: SCI10, SCI11 PCLKB: SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI12	PCLKA: SCI10, SCI11 PCLKB: SCI0, SCI1, SCI2, SCI3, SCI4, SCI5, SCI6 SCI7, SCI8, SCI9, SCI12

Table 2.54 Comparison of Serial Communications Interface Registers

Register	Bit	RX65N (SCIg, SCIi, SCIh)	RX660 (SCIk, SCIm, SCIh)
SEMR	ITE	—	Immediate transmission enable bit
	ABCSE	—	Asynchronous mode base clock select extended bit
SPTR	RXDMON	RXD line monitoring flag 0: RXDn pin is at the low level. 1: RXDn pin is at the high level.	RXD line monitoring flag When the RINV bit is set to 0: 0: RXDn pin is at the low level. 1: RXDn pin is at the high level. When the RINV bit is set to 1: 0: RXDn pin is at the high level. 1: RXDn pin is at the low level.
	RINV	—	Receiver input invert bit
	TINV	—	Transmission output inversion bit
	RTADJ	—	Receive data sampling timing adjustment bit
	TTADJ	—	Transmit signal change timing adjustment bit
TMGR	—	—	Transmit/receive timing select register

2.19 I²C Bus Interface

Table 2.55 is a Comparative Overview of I2C Bus Interface, and Table 2.56 is a Comparison of I2C Bus Interface Registers.

Table 2.55 Comparative Overview of I²C Bus Interface

Item	RX65N (RIICa)	RX660 (RIICa)
Communication format	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate	• I²C bus format or SMBus format • Master mode or slave mode selectable • Automatic securing of the various setup times, hold times, and bus-free times for the transfer rate
Transfer speed	Fast-mode Plus is supported (up to 1 Mbps)	Fast-mode supported (up to 400 kbps)
SCL clock	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%	For master operation, the duty cycle of the SCL clock is selectable in the range from 4% to 96%
Issuing and detecting conditions	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable	Start, restart, and stop conditions are automatically generated. Start conditions (including restart conditions) and stop conditions are detectable
Slave address	• Configurable for up to three different slave addresses • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.	• Configurable for up to three different slave addresses • 7-bit and 10-bit address formats are supported (along with the use of both at once). • General call addresses, device ID addresses, and SMBus host addresses are detectable.
Acknowledgment	• For transmission, the acknowledge bit is automatically loaded. • Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.	• For transmission, the acknowledge bit is automatically loaded. • Transfer of the next data for transmission can be automatically suspended on detection of a not-acknowledge bit. • For reception, the acknowledge bit is automatically transmitted. If a wait between the eighth and ninth clock cycles has been selected, software control of the value in the acknowledge field in response to the received value is possible.
Wait function	• In reception, the following periods of waiting can be obtained by holding the SCL clock at the low level: — Waiting between the eighth and ninth clock cycles — Waiting between the 9th and 1th clock cycles	• In reception, the following periods of waiting can be obtained by holding the SCL line at the low level: — Waiting between the eighth and ninth clock cycles — Waiting between the 9th and 1th clock cycles

Item	RX65N (RIICa)	RX660 (RIICa)
SDA output delay function	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.	Timing of the output of transmitted data, including the acknowledge bit, can be delayed.
Arbitration	• For multi-master operation Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration is detectable when start condition is issued while the bus is busy (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detectable by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • In slave transmission, loss of arbitration is detectable if data mismatch.	• For multi-master operation Operation to synchronize the SCL clock in cases of conflict with the SCL signal from another master is possible. When issuing the start condition would create conflict on the bus, loss of arbitration is detected by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. In master operation, loss of arbitration is detected by testing for non-matching between the signal on the SDA line and the internal signal for the SDA line. • Loss of arbitration is detectable when start condition is issued while the bus is busy (to prevent the issuing of double start conditions). • When transmitting a not-acknowledge bit, loss of arbitration is detectable by testing for non-matching between the internal signal for the SDA line and the level on the SDA line. • In slave transmission, loss of arbitration is detectable if data mismatch.
Timeout function	The internal timeout function is capable of detecting long-interval stop of the SCL clock	The internal timeout function is capable of detecting long-interval stop of the SCL clock
Noise cancellation	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the interval for noise cancellation is adjustable by software.	The interface incorporates digital noise filters for both the SCL and SDA inputs, and the interval for noise cancellation is adjustable by software.
Interrupt sources	4 sources • Transfer error or event occurrence — Arbitration detection — NACK detection — Timeout detection — Start condition (or restart condition) detection — Stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmission complete	4 sources • Transfer error or event occurrence — Arbitration detection — NACK detection — Timeout detection — Start condition (or restart condition) detection — Stop condition detection • Receive data full (including matching with a slave address) • Transmit data empty (including matching with a slave address) • Transmission complete
Low Power Consumption	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Table 2.56 Comparison of I²C Bus Interface Registers

Register	Bit	RX65N (RIICa)	RX660 (RIICa)
ICFER	FMPE(Note 1)	Fast mode plus enable bit	—

Note 1. The Fast-mode Plus enable bit (FMPE) is only supported by RIIC0. In RIIC1 and RIIC2, bit 7 is reserved.

2.20 CAN Module and CANFD Module

Table 2.57 is Comparative Overview of CAN Module and CANFD Module, and Table2.58 is Comparison of CAN Module/CANFD Module Registers.

Table 2.57 Comparative Overview of CAN Module and CANFD Module

Item	RX65N (CAN)	RX660 (CANFD-Lite)
Protocol	Conforming to the ISO 11898-1 standard (standard frame or extension frame)	Conforming to the ISO 11898-1:2015 specifications
Bit rate (RX65N) Data transfer rate (RX660)	Programming is possible with a maximum bit rate of 1 Mbps (fCAN is equal to or larger than 8 MHz). — fCAN: CAN clock source	• Arbitration phase: Maximum of 1 Mbps • Data phase: Maximum 8 Mbps(Note 1)
Operating frequency	PCLKB: 60MHz (max) CANFDMCLK: 24 MHz (max)	• Register block: Maximum of 60 MHz (PCLKB) • Message buffer RAM: Maximum of 120 MHz (PCLKA)
Operating clock for data link layer (DLL clock)	—	Maximum of 60 MHz (either CANFDMCLK or CANFDCLK can be selected)
Message box (RX65N) Message buffer (RX660)	32 mailboxes: Two mail box modes can be selected. • Normal mailbox mode: 32 mailboxes can be configured for transmission or reception. • FIFO mailbox mode: 24 mailboxes can be configured for transmission or reception. The remaining mailboxes can be configured as a 4-stage transmit FIFO and a 4-stage receive FIFO.	• 32 receive message buffers • Four transmit message buffers • One transmit queue Automatic transfer of messages to the transmit queue is supported.
Frame type	• Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID)	Classic CAN (CAN 2.0) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID) • Remote frame in base format (11-bit ID) • Remote frame in extended format (29-bit ID) CAN FD(Note 1) • Data frame in base format (11-bit ID) • Data frame in extended format (29-bit ID)

Item	RX65N (CAN)	RX660 (CANFD-Lite)
Reception	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot receive function can be selected. • Overwrite mode (message is overwritten) or overrun mode (message is discarded) can be selected. • Reception end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be received. • The ID format to be received (base ID only, extended ID only, or both base ID and extended ID) can be selected. • Receive message buffer interrupt can be enabled or disabled individually for each message buffer.
Data length	0 to 8 bytes	Classic CAN: 0 to 8 bytes CAN FD: 0 to 8, 12, 16, 20, 24, 32, 48, and 64 bytes(Note 1)
Acceptance filter	• Eight acceptance masks (an individual mask for every four mailboxes) • Mailbox masks can be enabled or disabled individually.	Filtering is possible in the following fields: • IDE bit (base format, extended format, or both) • ID field • RTR bit (data frame or remote frame) (only for Classic CAN) • DLC field Data (data length) The protection function when the payload size is exceeded is provided. Acceptance filter list (AFL) entries can be updated during communication.
Transmission	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only, extended ID only, or both base ID and extended ID) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or mailbox number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Transmission end interrupt can be enabled or disabled individually for each mailbox.	• Data frames and remote frames can be sent. • The ID format to be sent (base ID only or extended ID only) can be selected. • The one-shot transmission function can be selected. • Either ID priority transmission mode or message buffer number priority transmission mode can be selected. • Transmission requests can be aborted (completion of abort can be confirmed with a flag). • Channel transmission interrupt can be enabled and disabled.
FIFO	• 24 mailboxes can be configured for transmission or reception. • The remaining mailboxes can be configured as a 4-stage transmit FIFO and a 4-stage receive FIFO.	The FIFO size is programmable. • Two receive FIFOs • One common FIFO (Whether to use the FIFO as a receive FIFO or transmit FIFO can be selected.)
Automatic transmission interval adjustment	—	• Available when the common FIFO is configured as a transmit FIFO • The interval between messages sent from the FIFO can be adjusted.

Item	RX65N (CAN)	RX660 (CANFD-Lite)
Bus-off recovery method	How to recover from the bus-off state can be selected. • Conforming to the ISO 11898-1 standard • The mode automatically changes to CAN Halt mode when bus off starts. • The mode automatically changes to CAN Halt mode when bus off ends. • A program causes a transition to CAN Halt mode. • A program causes a transition to error active state.	How to recover from the bus-off state can be selected. • Normal mode (ISO 11898-1 compliant) • Automatically enters CH_HALT mode when bus off starts. • Automatically enters CAN Halt mode when bus off ends • Software causes a transition CH_HALT mode (during bus-off recovery period). • A program causes a transition to error active state.
Timestamp function	• Timestamp function with a 16-bit counter • The reference clock can be selected from 1, 2, 4, and 8 bit time.	Transmission and reception timestamp function
Interrupt function	Five types of interrupt sources (reception end interrupt, transmission end interrupt, receive FIFO interrupt, transmit FIFO interrupt, and error interrupt)	Receive FIFO interrupt Global error interrupt Channel transmission interrupt Channel error interrupt Common FIFO reception interrupt Receive message buffer interrupt
CAN sleep mode	Current consumption can be reduced by stopping the CAN clock.	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode)
Software support	—	Label information is automatically added to received messages.
Software support units	Three software support unis • Acceptance filter support • Mailbox search support (receive mailbox search, transmit mailbox search, and message lost search) • Channel search support	—
Test modes	Three test modes are provided for user evaluation: • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback)	• Basic test mode • Listen-only mode • Self test mode 0 (external loopback) • Self test mode 1 (internal loopback)
Low power consumption function (RX65N) Power down function (RX660)	Transition to the module stop state is possible.	Module start/stop function for each CAN node (CH_SLEEP mode and GL_SLEEP mode) Transition to the module stop state is possible.
RAM	—	RAM with ECC protection

Note 1. This is only available for products that support the CAN FD protocol.

Table2.58 Comparison of CAN Module/CANFD Module Registers

Register	Bit	RX65N (CAN)	RX660 (CANFD-Lite)
CTLR	—	Control register	—
BCR	—	Bit configuration register	—
MKRk	—	Mask register k (k = 0 to 7)	—
FIDCR0 FIDCR1	—	FIFO receive ID comparison register	—
MKIVLR	—	Mask disable register	—
MBj	—	Mailbox register j (j = 0 to 31)	—
MIER	—	Mailbox interrupt enable register	—
MCTLj	—	Message control register j (j = 0 to 3)	—
RFCR	—	Receive FIFO control register	—
RFPCR	—	Receive FIFO pointer control register	—
TFCR	—	Transmit FIFO control register	—
TFPCR	—	Transmit FIFO pointer control register	—
STR	—	Status register	—
MSMR	—	Mailbox search mode register	—
MSSR	—	Mailbox search status register	—
CSSR	—	Channel search support register	—
AFSR	—	Acceptance filter support register	—
EIER	—	Error interrupt enable register	—
EIFR	—	Error interrupt source decision register	—
RECR	—	Receive error count register	—
TECR	—	Transmit error count register	—
ECSR	—	Error code storage register	—
TSR	—	Timestamp register	—
TCR	—	Test control register	—
NBCR	—	—	Nominal bit rate configuration register
CHCR	—	—	Channel control register
CHSR	—	—	Channel status register
CHESR	—	—	Channel error status register
DBCR	—	—	Data bit rate configuration register
FDCFG	—	—	CAN FD configuration register
FDCTR	—	—	CAN FD control register
FDSTS	—	—	CAN FD status register
FDCRC	—	—	CAN FD CRC register
GCFG	—	—	Global configuration register
GCR	—	—	Global control register
GSR	—	—	Global status register
GESR	—	—	Global error status register
TISR	—	—	Transmit interrupt status register
TSCR	—	—	Timestamp counter register
AFCR	—	—	Acceptance filter list control register
AFCFG	—	—	Acceptance filter list configuration register

Register	Bit	RX65N (CAN)	RX660 (CANFD-Lite)
AFLn.IDR	—	—	Acceptance filter list n ID register (n = 0 to 15)
AFLn.MASK	—	—	Acceptance filter list n mask register (n = 0 to 15)
AFLn.PTR0	—	—	Acceptance filter list n pointer register 0 (n = 0 to 15)
AFLn.PTR1	—	—	Acceptance filter list n pointer register 1 (n = 0 to 15)
RMCR	—	—	Receive message buffer configuration register
RMNDR	—	—	Receive message buffer new data register
RFCRn	—	—	Receive FIFO n configuration register (n = 0 or 1)
RFSRn	—	—	Receive FIFO n status register (n = 0 or 1)
RFPCRn	—	—	Receive FIFO n pointer control register (n = 0 or 1)
CFCR0	—	—	Common FIFO 0 configuration register
CFSR0	—	—	Common FIFO 0 status register
CFPCR0	—	—	Common FIFO 0 pointer control register
FESR	—	—	FIFO empty status register
FFSR	—	—	FIFO full status register
FMLSR	—	—	FIFO message lost status register
RFISR	—	—	Receive FIFO interrupt status register
DTCR	—	—	DMA transfer control register
DTSR	—	—	DMA transfer status register
TMCRn	—	—	Transmit message buffer n control register (n = 0 to 3)
TMSRn	—	—	Transmit message buffer n status register (n = 0 to 3)
TMTRSR0	—	—	Transmit message buffer transmission request status register 0
TMARSR0	—	—	Transmit message buffer transmission abort request status register 0
TMTCSR0	—	—	Transmit message buffer transmission completion status register 0
TMTASR0	—	—	Transmit message buffer transmission abort status register 0
TMIER0	—	—	transmission message buffer interrupt enable register 0
TQCR0	—	—	Transmit queue 0 configuration register
TQSR0	—	—	Transmit queue 0 status register
TQPCR0	—	—	Transmit queue 0 pointer control register
THCR	—	—	Transmission history configuration register
THSR	—	—	Transmission history status register

Register	Bit	RX65N (CAN)	RX660 (CANFD-Lite)
THACR0	—	—	Transmission history access register 0
THACR1	—	—	Transmission history access register 1
THPCR	—	—	Transmission history pointer control register
GRCR	—	—	Global reset control register
GTMCR	—	—	Global test mode configuration register
GTMER	—	—	Global test mode enable register
GTMLKR	—	—	Global test mode lock key register
RTPARk	—	—	RAM test page access register k (k = 0 to 63)
AFIGSR	—	—	Acceptance filter list ignore entry setting register
AFIGER	—	—	Acceptance filter list ignore entry enable register
RMIER	—	—	Receive message buffer interrupt enable register
ECCSR	—	—	ECC control/status register
ECTMR	—	—	ECC test mode register
ECTDR	—	—	ECC decoder test data register
ECEAR	—	—	ECC error address register

2.21 Serial Peripheral Interface

Table 2.59 is a Comparative Overview of Serial Peripheral Interfaces, and Table 2.60 is a Comparison of Serial Peripheral Interface Registers.

Table 2.59 Comparative Overview of Serial Peripheral Interfaces

Item	RX65N (RSPIc)	RX660 (RSPId)
Number of channels	3 channels	1 channel
RSPI transfer functions	• Use of MOSI (master out/slave in), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK	• Use of MOSI (master out/slave in), SSL (slave select), and RSPCK (RSPI clock) signals allows serial communications through SPI operation (4-wire method) or clock synchronous operation (3-wire method). • Communication modes: Full-duplex or simplex (transmit-only or reception-only (in slave mode)) can be selected. • Switching of the polarity of RSPCK • Switching of the phase of RSPCK
Data format	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable	• MSB first/LSB first selectable • Transfer bit length is selectable as 8, 9, 10, 11, 12, 13, 14, 15, 16, 20, 24, or 32 bits. • 128-bit transmit/receive buffers • Up to four frames can be transferred in one round of transmission/reception (each frame consisting of up to 32 bits). • Byte swapping of transmit and receive data is selectable • Ability to invert the logic level of transmit/receive data
Bit rate	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK	• In master mode, the on-chip baud rate generator generates RSPCK by frequency-dividing PCLK (the division ratio ranges from divided by 2 to divided by 4096). • In slave mode, the minimum PCLK clock divided by 4 can be input as RSPCK (the maximum frequency of RSPCK is that of PCLK divided by 4). — Width at high level: 2 cycles of PCLK — Width at low level: 2 cycles of PCLK
Buffer configuration	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers	• Double buffer configuration for the transmit/receive buffers • 128 bits for the transmit/receive buffers

Item	RX65N (RSPIc)	RX660 (RSPId)
Error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection	• Mode fault error detection • Overrun error detection • Parity error detection • Underrun error detection
SSL control function	• Four SSL pins (SSLx0 to SSLx3) for each channel • In single-master mode, SSLx0 to SSLx3 pins are output. • In multi-master mode: SSLx0 pin for input, and SSLx1 to SSLx3 pins for either output or unused. • In slave mode: SSLx0 pin for input, and SSLx1 to SSLx3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Function for changing SSL polarity	• Four SSL pins (SSLA0 to SSLA3) for each channel • In single-master mode, SSLA0 to SSLA3 pins are output. • In multi-master mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for either output or unused. • In slave mode: SSLA0 pin for input, and SSLA1 to SSLA3 pins for unused. • Controllable delay from SSL output assertion to RSPCK operation (RSPCK delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable delay from RSPCK stop to SSL output negation (SSL negation delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Controllable wait for next-access SSL output assertion (next-access delay) — Range: 1 to 8 RSPCK cycles — (set in RSPCK-cycle units) • Function for changing SSL polarity
Control in master transfer	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function	• A transfer of up to eight commands can be executed sequentially in looped execution. • For each command, the following can be set: SSL signal value, bit rate, RSPCK polarity/phase, transfer data length, MSB/LSB first, burst, RSPCK delay, SSL negation delay, and next-access delay • A transfer can be initiated by writing to the transmit buffer. • MOSI signal value specifiable in SSL negation • RSPCK auto-stop function • The delay between data bytes can be shortened during burst transfers.

Item	RX65N (RSPIc)	RX660 (RSPId)
Interrupt sources	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — RSPI error interrupt (mode fault, overrun, underrun, or parity error) — RSPI idle interrupt (RSPI idle)	• Interrupt sources — Receive buffer full interrupt — Transmit buffer empty interrupt — Error interrupt (mode fault, overrun, underrun, or parity error) — Idle interrupt — Communication end interrupt
Event link function (output)	• The following events can be output to the event link controller (RSPI0): — Receive buffer full event signal — Transmit buffer empty event signal — Mode fault, overrun, underrun, or parity error event signal — RSPI idle event signal — Transmission-completed event signal	• Interrupt sources — Receive buffer full events — Transmit buffer empty events — Error events (mode fault, overrun, underrun, and parity error) — Idle events — Communication completion events
Other functions	• Function for switching between CMOS output and open-drain output • Function for initializing the RSPI • Loop back mode	• Function for initializing the RSPI • Loopback mode
Low power consumption function	• Transition to the module stop state is possible.	• Transition to the module stop state is possible.

Table 2.60 Comparison of Serial Peripheral Interface Registers

Register	Bit	RX65N (RSPIc)	RX660 (RSPId)
SPSR	SPCF	—	Communication completion flag
SPDCR2	DINV	—	Transfer data invert bit
SPCR3	—	—	RSPI control register 3

2.22 12-Bit A/D Converter

Table 2.61 is a Comparative Overview of 12-Bit A/D Converters, and Table 2.62 is a Comparison of 12-Bit A/D Converter Registers.

Table 2.61 Comparative Overview of 12-Bit A/D Converters

Item	RX65N (S12ADFa)	RX660 (S12ADH)
Number of units	2 units (S12AD and S12AD1)	One unit (S12AD)
Input channels	S12AD: 8 channels S12AD1: 21 channels + 1 extended	24 channels
Extended analog function	Temperature sensor output, internal reference voltage	Temperature sensor output, internal reference voltage
A/D conversion method	Successive approximation method	Successive approximation method
Resolution	12 bits	12 bits
Conversion time	0.48 µs per channel (for 12-bit conversion) 0.45 µs per channel (for 10-bit conversion) 0.42 µs per channel (for 8-bit conversion) (when A/D conversion clock (ADCLK) = 60 MHz)	0.9 µs per channel (when A/D conversion clock (ADCLK) = 60 MHz)
A/D conversion clock	Peripheral module clock PCLK and A/D conversion clock (ADCLK) can be set so that the frequency division ratio should be one of the following. PCLK to ADCLK frequency division ratio = 1:1, 2:1, 4:1, 8:1 ADCLK is set using the clock generation circuit.	Peripheral module clock PCLKB and A/D conversion clock (ADCLK) can be set so that the frequency ratio should be one of the following. PCLKB to ADCLK frequency ratio = 1:1, 1:2, 2:1, 4:1 ADCLK is set using the clock generation circuit. The A/D conversion clock (ADCLK) can operate at frequencies from a maximum of 60 MHz to a minimum of 8 MHz.

Item	RX65N (S12ADFa)	RX660 (S12ADH)
Data registers	• 29 registers for analog input (S12AD: 8 registers, S12AD1: 21 registers), one register for A/D-converted data duplication in double trigger mode for each unit, and two registers for A/D-converted data duplication during extended operation in double trigger mode for each unit • One register for temperature sensor output (S12AD1) • One register for internal reference (S12AD1) • One register for self-diagnosis for each unit • The results of A/D conversion are stored in 12-bit A/D data registers. • 8-, 10-, and 12-bit accuracy output for A/D conversion results • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes) The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.	• 24 registers for analog input, one for A/D-converted data duplication in double trigger mode Two registers for A/D-converted data duplication during extended operation in double trigger mode • One register for temperature sensor output • One register for internal reference One register for self-diagnosis The results of A/D conversion are stored in 12-bit A/D data registers. • The value obtained by adding up A/D-converted results is stored as a value in the number of bit for conversion accuracy + 2 bits/4 bits in the A/D data registers in A/D-converted value addition mode. • Double trigger mode (selectable in single scan and group scan modes) The first piece of A/D-converted analog-input data on one selected channel is stored in the data register for the channel, and the second piece is stored in the duplication register. • Extended operation in double trigger mode (available for specific triggers) A/D-converted analog-input data on one selected channel is stored in the duplication register that is prepared for each type of trigger.

Item	RX65N (S12ADFa)	RX660 (S12ADH)
Operating mode	The operating mode can be set individually for each of two units. • Single scan mode: A/D conversion is performed only once on arbitrarily selected analog inputs. A/D conversion is performed only once on the temperature sensor output (S12AD1). A/D conversion is performed only once on the internal reference voltage (S12AD1). A/D conversion is performed only once on the extended analog input (S12AD1). • Continuous scan mode: A/D conversion is performed repeatedly on the analog inputs of arbitrarily selected channels, the temperature sensor output (S12AD1), and the internal reference voltage (S12AD1). A/D conversion is performed repeatedly on the extended analog input (S12AD1). • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) Arbitrarily selected analog input channels, the temperature sensor output (S12AD1), and the internal reference voltage (S12AD1) are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (Group priority control selected) If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.	• Single scan mode: A/D conversion is performed only once on arbitrarily selected analog inputs. A/D conversion is performed only once on the temperature sensor output. A/D conversion is performed only once on the internal reference voltage. • Continuous scan mode: A/D conversion is performed repeatedly on arbitrarily selected analog inputs. • Group scan mode: — Two (groups A and B) or three (groups A, B, and C) can be selected as the number of groups to be used. (Only the combination of groups A and B can be selected when the number of groups is two.) Arbitrarily selected analog input channels, the temperature sensor output, and the internal reference voltage are divided into two groups (group A and B) or three groups (group A, B, and C), and A/D conversion of the analog input selected on a group basis is performed only once. — The scanning start condition for groups A, B, and C (synchronous trigger) can be independently selected, allowing A/D conversion of each group to be started independently. • Group scan mode (Group priority control selected) If a higher-priority group trigger is input during scanning of a lower-priority group, scanning of the lower-priority group stops and scanning of the higher-priority group starts. The priority order is group A (highest) > group B > group C (lowest). Whether or not to restart scanning (rescan) of the lower-priority group after processing for the higher-priority group completes, is selectable. Rescan can also be set to start either from the first selected channel or from the channel on which A/D conversion did not complete.

Item	RX65N (S12ADFa)	RX660 (S12ADH)
Conditions for A/D conversion start	• Software trigger • Synchronous trigger • Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), 16-bit timer pulse unit (TPU), or event link controller (ELC) • Asynchronous trigger • A/D conversion can be triggered by the external trigger ADTRG0# (S12AD) and ADTRG1# (S12AD1) pins (individually for each of the two units)	• Software trigger • Synchronous trigger • Trigger by the multi-function timer pulse unit (MTU), 8-bit timer (TMR), or event link controller (ELC) Asynchronous trigger • A/D conversion can be triggered by the external trigger ADTRG0# pin.
Functions	• Channel-dedicated sample-and-hold function (3ch: in S12AD only) • Variable sampling state count (settable on a per-channel basis) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection assist function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Switching function for 8-, 10-, and 12-bit conversion • Automatic clear function for A/D data registers • Extended analog input function • Compare function (window A and window B)	• Variable sampling time (settable on a per-channel basis) • Self-diagnosis of 12-bit A/D converter • Selectable A/D-converted value addition mode or average mode • Analog input disconnection detection function (discharge function/precharge function) • Double trigger mode (duplication of A/D conversion data) • Automatic clear function of A/D data registers • Compare function (window A and window B) • Ability to specify the channel conversion priority

Item	RX65N (S12ADFa)	RX660 (S12ADH)
Interrupt sources	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of single scan (individually for each of 2 units). • In double trigger mode, A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of double scan (individually for each of 2 units). • In group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI or S12GBADI1) for group B can be generated on completion of group B scan, an A/D scan end interrupt request (S12GCADI or S12GCADI1) for group C can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, an A/D scan end interrupt request (S12ADI or S12ADI1) can be generated on completion of a double scan of group A. A corresponding scan end interrupt request (S12GBADI/S12GCADI or S12GBADI1/S12GCADI1) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI, S12CMPAI1, S12CMPBI, or S12CMPBI1) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI/S12ADI1, S12GBADI/ S12GBADI1, and S12GCADI/S12GCADI1 interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).	• In the modes except double trigger mode and group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of single scan. • In double trigger mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan. • In group scan mode, an A/D scan end interrupt request (S12ADI) can be generated on completion of group A scan, an A/D scan end interrupt request (S12GBADI) for group B can be generated on completion of group B scan, and an A/D scan end interrupt request (S12GCADI) for group C can be generated on completion of group C scan. • When double trigger mode is selected in group scan mode, A/D scan end interrupt request (S12ADI) can be generated on completion of double scan of group A. A corresponding scan end interrupt request (S12GBADI or S12GCADI) can be generated on completion of a group B or group C scan. • A compare interrupt request (S12CMPAI or S12CMPBI) can be generated upon a match with the comparison condition for the digital compare function. • The S12ADI, S12GBADI, and S12GCADI interrupts can activate the DMA controller (DMAC) or data transfer controller (DTC).
Event link function	• An ELC event is generated on completion of all scans. • Scan can be started by a trigger output by the ELC.	• An event can be output upon completion of all scans. • In single scan mode, an event can be output when the compare function window condition is met. • Scan can be started by a trigger output by the ELC.
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.

Table 2.62 Comparison of 12-Bit A/D Converter Registers

Register	Bit	RX65N (S12ADFa)	RX660 (S12ADH)
ADDRy	—	A/D data register y (y = 0 to 7: S12AD, y = 0 to 20: S12AD1)	A/D data register y (y = 0 to 23)
ADANSA0	ANSA008 to ANSA015	—	A/D conversion channel select bits
ADANSA1	ANSA105 to ANSA107	—	A/D conversion channel select bits
ADANSB0	ANSB008 to ANSB015	—	A/D conversion channel select bits
ADANSB1	ANSB105 to ANSB107	—	A/D conversion channel select bits
ADANSC0	ANSC008 to ANSC015	—	A/D channel select register C0
ADANSC1	ANSC105 to ANSC107	—	A/D channel select register C1
ADSCSn	—	—	A/D channel conversion order setting register n (n = 0 to 23)
ADADS0	ADS008 to ADS015	—	A/D-converted value addition/average function select bits
ADADS1	ADS105 to ADS107	—	A/D-converted value addition/average function select bits
ADCER	ADPRC[1:0]	A/D conversion accuracy specify bit	—
ADEXICR	EXSEL[1:0]	Extended analog input select bit	—
	EXOEN	Extended analog output control bit	—
ADSHCR	—	A/D sample and hold circuit control register	—
ADSHMSR	—	A/D sample and hold operating mode select register	—
ADELCCR	—	—	A/D event link control register
ADCMPANSR0	CMPCHA008 to CMPCHA015	—	Compare window A channel select bits
ADCMPANSR1	CMPCHA105 to CMPCHA107	—	Compare window A channel select bits
ADCMPLR0	CMPLCHA008 to CMPLCHA015	—	Compare window A comparison condition select bits
ADCMPLR1	CMPLCHA105 to CMPLCHA107	—	Compare window A comparison condition select bits
ADCMPSR0	CMPSTCHA008 to CMPSTCHA015	—	Compare window A flag
ADCMPSR1	CMPSTCHA105 to CMPSTCHA107	—	Compare window A flag

Register	Bit	RX65N (S12ADFa)	RX660 (S12ADH)
ADCMPBNSR	CMPCHB[5:0]	Compare window B channel select bits These bits select channels to be compared with the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 0 0 1 1 0: AN006 0 0 0 1 1 1: AN007 Settings other than the above are prohibited.	Compare window B channel select bits These bits select channels to be compared with the compare window B conditions. b5 b0 0 0 0 0 0 0: AN000 0 0 0 0 0 1: AN001 0 0 0 0 1 0: AN002 : : 0 1 0 1 1 0: AN022 0 1 0 1 1 1: AN023 1 0 0 0 0 0: Temperature sensor 1 0 0 0 0 1: Internal reference voltage Settings other than the above are prohibited.
ADSAM	—	A/D successive approximation conversion time setting register	—
ADSAMPR	—	A/D successive approximation conversion time setting protection unlock register	—
ADVMONCR	—	—	A/D internal reference voltage monitoring circuit enable register
ADVMONO	—	—	A/D internal reference voltage monitoring circuit output enable register
ADVREFCR	—	—	A/D reference voltage control register

2.23 12-Bit D/A Converter

Table 2.63 is a Comparative Overview of 12-bit D/A Converters.

Table 2.63 Comparative Overview of 12-bit D/A Converters

Item	RX65N (R12DAa)	RX660 (R12DAb)
Resolution	12-bit	12 bits
Output channels	2 channel	2 channel
Measure against interference between analog modules	• Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter (unit 1). This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit D/A converter inrush current with the enable signal.	• Measure against interference between D/A and A/D converters: D/A converted data update timing is controlled by the 12-bit A/D converter synchronous D/A conversion enable signal output by the 12-bit A/D converter. This reduces degradation of A/D conversion accuracy due to interference by controlling the timing of the 12-bit /A converter inrush current with the enable signal.
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.
Event link function (input)	Ability to start D/A conversion on channel 0 when an event signal is input	Ability to start D/A conversion on channel 0 when an event signal is input
Output destination selection	Ability to switch between buffered output (gain = 1) and unbuffered output	Output to external pins and to comparator C can be controlled independently.

Table 2.64 Comparison of 12-bit D/A Converter Registers

Register	Bit	RX65N (R12DAa)	RX660 (R12DAb)
DAAMPCR	—	D/A output amplifier control register	—
DAASWCR	—	D/A output amplifier stabilization wait control register	—
DAADUSR	—	D/A A/D synchronous unit select register	—
DADSELR	—	—	D/A destination select register

2.24 Temperature Sensor

Table 2.65 is a Comparative Overview of Temperature Sensors.

Table 2.65 Comparative Overview of Temperature Sensors

Item	RX65N (TEMPS)	RX660 (TEMPS)
Temperature sensor voltage output	The temperature sensor outputs a voltage to the 12-bit A/D converter (unit 1).	The temperature sensor outputs a voltage to the 12-bit A/D converter (unit 0).
Low Power Consumption	Transition to the module stop state is possible.	—
Temperature sensor calibration data	Reference data measured for each chip at the time of shipment from the factory is stored in a register.	Reference data measured for each chip at the time of shipment from the factory is stored in a register.

Table 2.66 Comparison of Temperature Sensor Registers

Register	Bit	RX65N (TEMPS)	RX660 (TEMPS)
TSCR	—	Temperature sensor control register	—

2.25 Data Operation Circuit

Table 2.67 is Comparative Overview of Data Operation Circuits, and Table 2.68 is Comparison of Data Operation Circuit Registers.

Table 2.67 Comparative Overview of Data Operation Circuits

Item	RX65N (DOC)	RX660 (DOCA)
Data operation functions	16-bit data comparison, addition, and subtraction	• Comparison of 16- or 32-bit data (match/mismatch, greater/less, in/out of range) • Addition or subtraction of 16- or 32 bit data
Low power consumption function	Transition to the module stop state is possible.	Transition to the module stop state is possible.
Interrupts	• The compared values either match or mismatch • The result of data addition is greater than FFFFh (overflow). • The result of data subtraction is less than 0000h (underflow).	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)
Event link function (output)	• The compared values either match or mismatch. • The result of data addition is greater than FFFFh (overflow). • The result of data subtraction is less than 0000h (underflow).	• When data comparison result matches detection condition • When data addition result is greater than FFFFh (when DOCR.DOPSZ = 0) or FFFF FFFFh (when DOCR.DOPSZ = 1) (overflow) • When data subtraction result is less than 0000h (when DOCR.DOPSZ = 0) or 0000 0000h (when DOCR.DOPSZ = 1) (underflow)

Table 2.68 Comparison of Data Operation Circuit Registers

Register	Bit	RX65N (DOC)	RX660 (DOCA)
DOCR	DOPSZ	—	Data operation size select bit
	DCSEL (RX65N) DCSEL[2:0] (RX660)	Detection condition select bit 0: Data mismatches are detected. 1: Data matches are detected.	Detection condition select bits b6 b4 0 0 0: Mismatch (DODIR ≠ DODSR0) 0 0 1: Match (DODIR = DODSR0) 0 1 0: Less (DODIR < DODSR0) 0 1 1: Greater (DODIR > DODSR0) 1 0 0: In range (DODSR0 < DODIR < DODSR1) 1 0 1: Out of range (DODIR < DODSR0, DODSR1 < DODIR) Other than above: Setting prohibited.
	DOPCF	Data operation circuit flag	—
	DOPCFCL	DOPCF clear bit	—
DOSR	—	—	DOC status register
DOSCR	—	—	DOC status clear register
DODIR	—	DOC data input register	DOC data input register
		16-bit readable/writable register.	32-bit readable/writable register.
DODSR (RX65N) DODSR0/ DODSR1 (RX660)	—	DOC data setting register	DOC data setting registers 0 DOC data setting registers 1
		16-bit readable/writable register.	32-bit readable/writable register.

2.26 RAM

Table 2.69 is a Comparative Overview of RAM.

Table 2.69 Comparative Overview of RAM

Item	RX65N		RX660
	RAM	Extended RAM	—
RAM capacity	256 KB	384 KB	128 KB
RAM address	0000 0000h to 0003 FFFFh	0080 0000h to 0085 FFFFh	• RAM:0000 0000h to 0001 FFFFh
Memory buses	Memory bus 1	Memory bus 3	Memory bus 1
Access	Single-cycle access is possible for both reading and writing. The RAM can be enabled or disabled.		Single-cycle access is possible for both reading and writing. The RAM can be enabled or disabled.
Data retention function	Not available in deep software standby mode		Not available in deep software standby mode
Low power consumption function	RAM and extended RAM(Note 1) can individually transition to the module stop state.		Transition to the module stop state is possible.
Error checking	• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.		• Parity check: Detection of 1-bit errors • A non-maskable interrupt or an interrupt is generated when an error occurs.

Note 1. Only available for products with code flash memory capacity of 1.5 MB or more.

Table 2.70 Comparison of RAM Registers

Register	Bit	RX65N	RX660
EXRAMMODE	—	Extended RAM operation mode control register	—
EXRAMSTS	—	Extended RAM error status register	—
EXRAMECAD	—	Extended RAM error address capture register	—
EXRAMPRCR	—	Extended RAM protection register	—

2.27 Flash memory

Table 2.71 is a Comparative Overview of Flash Memory, and Table 2.72 is a Comparison of Flash Memory Registers.

Table 2.71 Comparative Overview of Flash Memory

Item	RX65N		RX660	
	Code Flash Memory	Data Flash Memory	Code Flash Memory	Data Flash Memory
Memory capacity	• User area: Up to 2 MB	• Data area: 32 KB	• User area: Up to 1 MB • User boot area: 32 KB	• Data area: 32 KB
ROM cache	• Capacity: Up to 256 bytes • Mapping method: 8-way set associative • Replacing method: LRU algorithm • Line size: 16 bytes	—	—	
Read cycles	• When a cache hit occurs: 1 cycle • When a cache miss occurs with ROM cache operation enabled or when ROM cache operation is prohibited: — 1 cycle if ICLK is equal to or smaller than 50 MHz, and — 2 cycles if ICLK is larger than 50 MHz and equal to or smaller than 100 MHz — 3 cycles if ICLK is larger than 100 MHz	Read access at each FCLK frequency cycle	One cycle	16-bit or 8-bit read access requires 8 FCLK clock cycles.
Value after erasure	FFh	Undefined	FFh	Undefined

Item	RX65N		RX660	
	Code Flash Memory	Data Flash Memory	Code Flash Memory	Data Flash Memory
Programming/ erasing method	• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory and to program option-setting memory (self-programming). • A serial programmer can be used to program and erase the flash memory via a serial interface (serial programming).		• FACI commands specified in the FACI command issuing area (007E 0000h) can be used to program and erase the code flash memory and data flash memory. • A flash memory programmer can be used to program and erase the flash memory via a serial interface (serial programming). • A user program can be used to program and erase the flash memory (self-programming).	
Security function	Protects against illicit tampering with or reading of data in flash memory.		Protects against illicit tampering with or reading of data in flash memory.	
Protection function	Protects against erroneous programming of the flash memory.		Protects against erroneous programming of the flash memory.	
Dual bank function	Dual bank configuration enables safe update that is not susceptible to interruption during rewrite operation. • Linear mode: A mode in which the code flash memory is used as one area. • Dual mode: A mode in which the code flash memory is divided into two areas.	—	—	
Trusted Memory (TM) function	Protects against illicit reading of the code flash memory. • Linear mode: Blocks 8, 9 • Dual mode: Blocks 8, 9, 46, 47	—	Protects against illicit reading of blocks 8 and 9 in the code flash memory.	
Background operation (BGO) function	• The code flash memory can be read while the code flash memory is being programmed or erased. • The data flash memory can be read while the code flash memory is being programmed or erased. • The code flash memory can be read while the data flash memory is being programmed or erased.		The user area can be read while the data area is being programmed or erased.	
Units of programming and erasure	• Units of programming for the user area or user boot area: 128 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: 64/128/256 bytes	• Units of programming for the user area or user boot area: 256 bytes • Units of erasure for the user area: Block units	• Unit of programming for the data area: 4 bytes • Unit of erasure for the data area: Block units

<table>
<tr><th rowspan="2">Item</th><th colspan="2">RX65N</th><th colspan="2">RX660</th></tr>
<tr><th>Code Flash Memory</th><th>Data Flash Memory</th><th>Code Flash Memory</th><th>Data Flash Memory</th></tr>
<tr><td rowspan="2">Other functions</td><td colspan="2">Interrupts can be accepted during self-programming.</td><td colspan="2">Interrupts can be accepted during self-programming.</td></tr>
<tr><td colspan="2">Initial settings of this MCU can be set in the option-setting memory.</td><td colspan="2">Initial settings of this MCU can be set in the option-setting memory.</td></tr>
<tr><td rowspan="2">On-board programming (serial programming and self-programming)</td><td colspan="2">• Programming/erasure in boot mode (SCI interface)
— The asynchronous serial interface (SCI1) is used.
— The communication speed is adjusted automatically.
• Programming/erasure in boot mode (USB interface)
— USBb is used.
— PC can be directly connected. No special hardware is needed.
• Programming/erasure in boot mode (FINE interface)
— FINE is used.</td><td colspan="2">• Programming/erasure in boot mode (SCI interface)
— The asynchronous serial interface (SCI1) is used.
— The communication speed is adjusted automatically.
— Programming and erasure of the user boot area is also possible.
• Programming/erasure in boot mode (FINE interface)
— FINE is used.</td></tr>
<tr><td colspan="2">• Programming/erasure by self-programming
— Allows flash memory programming/erasure without resetting the system.</td><td colspan="2">• Programming/erasure in user boot mode
— A user-specific boot program can be created.
• Programming/erasure in single-chip mode
— Programming or erasure by a routine within a user program for writing to the code flash memory or data flash memory is possible.</td></tr>
<tr><td>Off-board programming (programming and erasure using a parallel programmer)</td><td>Programming or erasure of the code flash memory and option-setting memory by using a parallel programmer is possible.</td><td>Programming or erasure of the data flash memory using a parallel programmer is not possible.</td><td>Programming or erasure of the user area or user boot area by using a parallel programmer is possible.</td><td>Programming or erasure of the data area using a parallel programmer is not possible.</td></tr>
<tr><td>Unique ID</td><td colspan="2">A unique 16-byte ID code is provided for each MCU.</td><td colspan="2">A unique 12-byte ID code is provided for each MCU.</td></tr>
</table>

Table 2.72 Comparison of Flash Memory Registers

Register	Bit	RX65N	RX660(FLASH)
FWEPROR	FLWE[1:0]	Flash write/erase enable bit • For products with code flash memory capacity of 1.5 MB or more: b1 b0 0 0: Prohibits programming, erasure and blank checking. 0 1: Permits programming, erasure and blank checking. 1 0: Prohibits programming, erasure and blank checking. 1 1: Prohibits programming, erasure and blank checking. • For products with code flash memory capacity of 1 MB or less: b1 b0 0 0: Prohibits programming and erasure. 0 1: Permits programming and erasure. 1 0: Prohibits programming and erasure. 1 1: Prohibits programming and erasure.	Flash write/erase enable bit b1 b0 0 0: Prohibits programming and erasure, programming and erasure of lock bits, and blank checking. 0 1: Permits programming and erasure, programming and erasure of lock bits, and blank checking. 1 0: Prohibits programming and erasure, programming and erasure of lock bits, and blank checking. 1 1: Prohibits programming and erasure, programming and erasure of lock bits, and blank checking.
ROMCE	—	ROM cache enable register	—
ROMCIV	—	ROM cache disable register	—
FASTAT	—	—	Flash access status register
FAEINT	—	—	Flash access error interrupt enable register
FRDYIE	—	—	Flash ready interrupt enable register
FSADDR	—	—	FACI command start address register
FEADDR	—	—	FACI command end address register
FSTATR	—	—	Flash status register
FENTRYR	—	—	Flash P/E mode entry register
FPROTR	—	—	Flash protection register
FSUINITR	—	—	Flash sequencer set-up initialization register
FLKSTAT	—	—	Lock bit status register
FCMDR	—	—	FACI command register
FPESTAT	—	—	Flash P/E status register
FBCCNT	—	—	Data flash blank check control register
FBCSTAT	—	—	Data flash blank check status register
FPSADDR	—	—	Data flash programming start address register
FCPSR	—	—	Flash sequencer processing switching register

Register	Bit	RX65N	RX660(FLASH)
FPCKAR	—	—	Flash sequencer processing clock notification register
UIDRn	—	Unique ID register n (n = 0 to 3)	Unique ID register n (n = 0 to 2)
EEPFCLK	—	Data flash memory access frequency setting register	—

2.28 Packages

As indicated in Table 2.73, there are discrepancies in the package drawing codes and availability of some package types, and this should be borne in mind at the board design stage.

Table 2.73 Packages

Package Type	RENESAS Code	
	RX65N	RX660
177-pin TFLGA	○	×
176-pin LFBGA 176-pin LFQFP	○	×
145-pin TFLGA	○	×
100-pin TFLGA	○	×
80-pin LFQFP	×	○
48-pin LFQFP	×	○

○: Package available (Renesas code omitted); ×: Package not available

3. Comparison of Pin Functions

This section presents a comparative description of pin functions as well as a comparison of the pins for the power supply, clocks, and system control. Items that exist only on one group are indicated by **blue text**. Items that exists on both groups with different specifications are indicated by **red text**. **Black text** indicates there is no differences in the item's specifications between groups.

3.1 144-Pin Package

Table 3.1 is Comparative Listing of 144-Pin Package Pin Functions.

Table 3.1 Comparative Listing of 144-Pin Package Pin Functions

144 Pin LFQFP	RX65N	RX660
1	AVSS0	AVSS0
2	P05/IRQ13/DA1	P05/IRQ13/DA1
3	AVCC1	P06
4	P03/IRQ11/DA0	P03/IRQ11/DA0
5	AVSS1	P04
6	P02/TMCI1/SCK6/IRQ10/AN120	P02/TMCI1/SCK6/IRQ10
7	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9/ AN119	P01/TMCI0/RXD6/SMISO6/SSCL6/IRQ9
8	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8/ AN118	P00/TMRI0/TXD6/SMOSI6/SSDA6/IRQ8
9	PF5/IRQ4	PF5/IRQ4
10	EMLE	EMLE(Note 1)/PN7(Note 2)
11	PJ5/POE8#/CTS2#/RTS2#/SS2#	PJ5/POE8#/CTS2#/RTS2#/SS2#/IRQ13
12	VSS	PJ4
13	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/CTS6#/ RTS6#/SS6#/CTS0#/RTS0#/SS0#	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/ CTS0#/RTS0#/SS0#/IRQ11
14	VCL	VCL
15	VBATT	PJ1/MTIOC3A
16	MD/FINED	MD/FINED/PN6
17	XCIN	XCIN(Note 3)/PH7(Note 4)
18	XCOUT	XCOUT(Note 3)/PH6(Note 4)
19	RES#	RES#
20	XTAL/P37	XTAL/P37/IRQ4
21	VSS	VSS
22	EXTAL/P36	EXTAL/P36/IRQ5
23	VCC	VCC
24	UPSEL/P35/NMI	P35/NMI
25	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	TRST#(Note 1)/P34/MTIOC0A/TMCI3/ POE10#/SCK6/SCK0/IRQ4
26	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/PCKO/ IRQ3-DS	P33/MTIOC0D/TMRI3/ POE4#/POE11#/RXD6/SMISO6/SSCL6/ RXD0/SMISO0/SSCL0/CRX0-A/IRQ3-DS
27	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/VSYNC/IRQ2-DS	P32/MTIOC0C/TMO3/RTCIC2(Note 5)/ RTCOUT(Note 5)/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0-A/IRQ2-DS

144 Pin LFQFP	RX65N	RX660
28	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS(Note 1)/P31/MTIOC4D/TMCI2/ RTCIC1(Note 5)/CTS1#/RTS1#/SS1#/IRQ1-DS
29	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/ MISOB-A/IRQ0-DS	TDI(Note 1)/P30/MTIOC4B/TMRI3/RTCIC0(Note 5)/ POE8#/RXD1/SMISO1/SSCL1/IRQ0-DS/ COMP3
30	TCK/P27/CS7#/MTIOC2B/TMCI3/PO7/ SCK1/RSPCKB-A	TCK(Note 1)/P27/CS3#/MTIOC2B/TMCI3/ SCK1/IRQ7/CVREFC3
31	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/ TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO(Note 1)/P26/CS2#/MTIOC2A/TMO1/ TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ IRQ6/CMPC30
32	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ SDHI_CD(Note 6)/HSYNC/ADTRG0#	P25/CS1#/MTIOC4C/MTCLKB/RXD3/ SMISO3/SSCL3/IRQ5/ADTRG0#
33	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN/ SDHI_WP(Note 6)/PIXCLK	P24/CS0#/MTIOC4A/MTCLKA/ TMRI1/SCK3/IRQ12
34	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#/SDHI_D1-C(Note 6)/PIXD7	P23/MTIOC3D/MTCLKD/TXD3/ SMOSI3/SSDA3/CTS0#/RTS0#/SS0#/IRQ3
35	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB/ SDHI_D0-C(Note 6)/PIXD6	P22/MTIOC3B/MTCLKC/TMO0/ SCK0/IRQ15
36	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/ SCL1(Note 6)/USB0_EXICEN/ SDHI_CLK-C(Note 6)/PIXD5/IRQ9	P21/MTIOC1B/TMCI0/ MTIOC4A/RXD0/SMISO0/SSCL0/IRQ9
37	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1(Note 6)/USB0_ID/ SDHI_CMD-C(Note 6)/PIXD4/IRQ8	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/ SSDA0/IRQ8
38	P17/MTIOC3A/MTIOC3B/MTIOC4B/ TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/T XD3/SMOSI3/SSDA3/SDA2-DS/ SDHI_D3-C(Note 6)/PIXD3/IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
39	P87/MTIOC4C/TIOCA2/SMOSI10/SSDA10/ TXD10/SDHI_D2-C(Note 6)/PIXD2	P87/MTIOC4C/SMOSI10/SSDA10/ TXD10/TXD010-B/SMOSI010-B/ SSDA010-B/IRQ15
40	P16/MTIOC3C/MTIOC3D/TIOCB1/ TCLKC/TMO2/PO14/RTCOUT/TXD1/ SMOSI1/SSDA1/RXD3/SMISO3/ SSCL3/SCL2-DS/USB0_VBUSEN/ USB0_VBUS/USB0_OVRCURB/ IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/ RTCOUT/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/MOSIA-C/SCL2/ IRQ6/ADTRG0#
41	P86/MTIOC4D/TIOCA0/SMISO10/SSCL10/ RXD10/PIXD1	P86/MTIOC4D/SMISO10/SSCL10/RXD10/ RXD010-B/SMISO010-B/SSCL010-B/IRQ14
42	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/PIXD0/IRQ5	P15/MTIOC0B/MTCLKB/ TMCI2/RXD1/SMISO1/SSCL1/SCK3/ CRX0-C/IRQ5/CMPC20
43	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2

144 Pin LFQFP	RX65N	RX660
44	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ ADTRG1#	P13/MTIOC0B/TMO3/TXD2/SMOSI2/ SSDA2/SDA0/IRQ3
45	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/ SSCL2/SCL0/IRQ2
46	VCC_USB	PH3/MTIOC4D/TMCI0
47	USB0_DM	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
48	USB0_DP	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
49	VSS_USB	PH0/MTIOC3B/CACREF/ADTRG0#
50	P56/EDACK1/MTIOC3C/TIOCA1/SCK7(Note 6)	P56/MTIOC3C/SCK7/IRQ6
51	TRDATA3/P55/D0[A0/D0](Note 6)/WAIT#/ EDREQ0/MTIOC4D/TMO3/ET0_EXOUT/ TXD7(Note 6)/SMOSI7(Note 6)/SSDA7(Note 6)/ CRX1/IRQ10	TRDATA3(Note 1)/P55/D0[A0/D0]/WAIT#/ MTIOC4D/MTIOC4A/TMO3/TXD7/ SMOSI7/SSDA7/CRX0-D/IRQ10
52	TRDATA2/P54/ALE/ D1[A1/D1](Note 6)/EDACK0/MTIOC4B/TMCI1/ ET0_LINKSTA/CTS2#/RTS2#/SS2#/CTX1	TRDATA2(Note 1)/P54/ALE/D1[A1/D1]/ MTIOC4B/TMCI1/CTS2#/RTS2#/SS2#/ CTX0-D/IRQ4
53	P53(Note 7)/BCLK	P53/BCLK/PMC0/IRQ3
54	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/IRQ2
55	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/PMC0/IRQ1
56	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/SSDA2/ IRQ0
57	VSS	VSS
58	TRCLK/P83/EDACK1/MTIOC4C/ET0_CRS/ RMII0_CRS_DV/SCK10/SS10#/CTS10#	TRCLK(Note 1)/P83/MTIOC4C/SCK10/SS10#/ CTS10#/SCK010-B/CTS010#-A/ SS010#-A/IRQ3
59	VCC	VCC
60	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/MMC_D7-A/IRQ14	UB/PC7/CS0#/MTIOC3A/MTCLKB/ TMO2/CACREF/TOC0/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ TXD010-C/SMOSI010-C/SSDA010-C/ MISOA-A/IRQ14
61	PC6/D2[A2/D2](Note 6)/A22/CS1#/ MTIOC3C/MTCLKA/TMCI2/PO30/TIC0/ ET0_ETXD3/RXD8/SMISO8/SSCL8/ SMISO10/SSCL10/RXD10/ MOSIA-A/MMC_D6-A/IRQ13	PC6/D2[A2/D2]/CS1#/MTIOC3C/ MTCLKA/TMCI2/TIC0/RXD8/SMISO8/ SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13
62	PC5/D3[A3/D3](Note 6)/A21/CS2#/WAIT#/ MTIOC3B/MTCLKD/TMRI2/PO29/ ET0_ETXD2/SCK8/SCK10/ RSPCKA-A/MMC_D5-A	PC5/D3[A3/D3]/CS2#/WAIT#/ MTIOC3B/MTCLKD/TMRI2/MTIOC0C/SCK8/ SCK10/SCK010-C/RSPCKA-A/PMC0/IRQ5
63	TRSYNC/P82/EDREQ1/MTIOC4A/PO28/ ET0_ETXD1/RMII0_TXD1/SMOSI10/ SSDA10/TXD10/MMC_D4-A	TRSYNC(Note 1)/P82/MTIOC4A/ SMOSI10/SSDA10/TXD10/TXD010-A/ SMOSI010-A/SSDA010-A/IRQ2
64	TRDATA1/P81/EDACK0/MTIOC3D/PO27/ ET0_ETXD0/RMII0_TXD0/SMISO10/ SSCL10/RXD10/QIO3-A/SDHI_CD/ MMC_D3-A	TRDATA1(Note 1)/P81/MTIOC3D/SMISO10/ SSCL10/RXD10/RXD010-A/SMISO010-A/ SSCL010-A/IRQ9

144 Pin LFQFP	RX65N	RX660
65	TRDATA0/P80/EDREQ0/MTIOC3B/PO26/ ET0_TX_EN/RMII0_TXD_EN/SCK10/ RTS10#/QIO2-A/SDHI_WP/MMC_D2-A	TRDATA0(Note 1)/P80/MTIOC3B/SCK10/ RTS10#/SCK010-A/RTS010#-A/ DE010-A/IRQ8
66	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ SSLA0-A/QMI-A/QIO1-A/ SDHI_D1-A/SDSI_D1-A/MMC_D1-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/ TMCI1/POE0#/MTIOC0A/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ CTS010#-B/RTS010#-B/SS010#-B/ DE010-B/SSLA0-A/PMC0/IRQ12
67	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5/ QMO-A/QIO0-A/SDHI_D0-A/ SDSI_D0-A/MMC_D0-A	PC3/A19/MTIOC4D/TXD5/SMOSI5/ SSDA5/PMC0/IRQ11
68	TRDATA7/P77/CS7#/PO23/ET0_RX_ER/ RMII0_RX_ER/SMOSI11/SSDA11/TXD11/ QSPCLK-A/SDHI_CLK-A/SDSI_CLK-A/ MMC_CLK-A	TRDATA7(Note 1)/P77/SMOSI11/SSDA11/ TXD11/TXD011-A/SMOSI011-A/SSDA011-A/ IRQ7
69	TRDATA6/P76/CS6#/PO22/ET0_RX_CLK/ REF50CK0/SMISO11/SSCL11/RXD11/ QSSL-A/SDHI_CMD-A/ SDSI_CMD-A/MMC_CMD-A	TRDATA6(Note 1)/P76/SMISO11/SSCL11/ RXD11/RXD011-A/SMISO011-A/ SSCL011-A/IRQ14
70	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A/SDHI_D3-A/SDSI_D3-A/ MMC_CD-A	PC2/A18/MTIOC4B/RXD5/SMISO5/ SSCL5/TXDB011-A/SSLA3-A/IRQ10
71	TRSYNC1/P75/CS5#/PO20/ET0_ERXD0/ RMII0_RXD0/SCK11/RTS11#/ SDHI_D2-A/SDSI_D2-A/MMC_RES#-A	TRSYNC1(Note 1)/P75/SCK11/RTS11#/ SCK011-A/RTS011#-A/DE011-A/IRQ13
72	TRDATA5/P74/A20/CS4#/PO19/ ET0_ERXD1/RMII0_RXD1/SS11#/CTS11#	TRDATA5(Note 1)/P74/A20/SS11#/CTS11#/ CTS011#-A/SS011#-A/IRQ12
73	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/SCK5/ TXD011-C/SMOSI011-C/SSDA011-C/ TXDA011-C/SSLA2-A/IRQ12
74	VCC	PL1
75	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/ SSLA1-A/IRQ14	PC0/A16/MTIOC3C/CTS5#/RTS5#/ SS5#/RXD011-C/SMISO011-C/SSCL011-C/ SSLA1-A/IRQ14
76	VSS	PL0
77	TRDATA4/P73/CS3#/PO16/ET0_WOL	TRDATA4(Note 1)/P73/CS3#/IRQ8
78	PB7/A15/MTIOC3B/TIOCB5/PO31/ ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
79	PB6/A14/MTIOC3D/TIOCA5/PO30/ET0_ETXD1/RMII0_TXD1/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/SDSI_D0-B	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
80	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/ RMII0_TXD0/SCK9/SCK11/ SDSI_CLK-B/LCD_CLK-B(Note 6)	PB5/A13/MTIOC2A/MTIOC1B/ TMRI1/POE4#/TOC2/SCK9/SCK11/ SCK011-B/IRQ13

144 Pin LFQFP	RX65N	RX660
81	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/ SDSI_CMD-B/LCD_TCON0-B(Note 6)	PB4/A12/CTS9#/RTS9#/SS9#/SS11#/ CTS11#/RTS11#/CTS011#-B/ RTS011#-B/SS011#-B/DE011-B/IRQ4
82	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/ RMII0_RX_ER/SCK4/SCK6/SDSI_D3-B/ LCD_TCON1-B(Note 6)	PB3/A11/MTIOC0A/MTIOC4A/ TMO0/POE11#/TIC2/SCK4/SCK6/ PMC0/IRQ3
83	PB2/A10/TIOCC3/TCLKC/PO26/ ET0_RX_CLK/REF50CK0/CTS4#/RTS4#/ SS4#/CTS6#/RTS6#/SS6#/SDSI_D2-B/ LCD_TCON2-B(Note 6)	PB2/A10/CTS4#/RTS4#/SS4#/ CTS6#/RTS6#/SS6#/IRQ2
84	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/ TXD4/SMOSI4/SSDA4/TXD6/SMOSI6/ SSDA6/LCD_TCON3-B(Note 6)/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/ TMCI0/TXD4/SMOSI4/SSDA4/TXD6/ SMOSI6/SSDA6/IRQ4-DS/COMP1
85	P72/A19/CS2#/ET0_MDC	P72/A19/CS2#/IRQ10
86	P71/A18/CS1#/ET0_MDIO	P71/A18/CS1#/IRQ1
87	PB0/A8/MTIC5W/TIOCA3/PO24/ ET0_ERXD1/RMII0_RXD1/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ LCD_DATA0-B(Note 6)/IRQ12	PB0/A8/MTIC5W/MTIOC3D/RXD4/ SMISO4/SSCL4/RXD6/SMISO6/SSCL6/ RSPCKA-C/IRQ12
88	PA7/A7/TIOCB2/PO23/ET0_WOL/ MISOA-B/LCD_DATA1-B(Note 6)	PA7/A7/MISOA-B/IRQ7
89	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/S S5#/MOSIA-B/LCD_DATA2-B(Note 6)	PA6/A6/MTIC5V/MTCLKB/TMCI3/ POE10#/MTIOC3D/MTIOC6B/CTS5#/ RTS5#/SS5#/CTS12#/RTS12#/SS12#/ MOSIA-B/IRQ14
90	PA5/A5/MTIOC6B/TIOCB1/PO21/ ET0_LINKSTA/RSPCKA-B/ LCD_DATA3-B(Note 6)	PA5/A5/MTIOC6B/RSPCKA-B/IRQ5
91	VCC	VCC
92	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/ SSLA0-B/LCD_DATA4-B(Note 6)/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TMRI0/ MTIOC4C/MTIOC7C/TXD5/SMOSI5/SSDA5/ TXD12/SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
93	VSS	VSS
94	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B(Note 6)/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/ MTIC5V/MTIOC4D/RXD5/SMISO5/SSCL5/ IRQ6-DS/CMPC10
95	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/LCD_DATA6-B(Note 6)	PA2/A2/MTIOC7A/RXD5/SMISO5/ SSCL5/RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
96	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/TIOCB 0/PO17/ET0_WOL/SCK5/SSLA2-B/ LCD_DATA7-B(Note 6)/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/ IRQ11/ADTRG0#
97	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/ET0_TX_EN/ RMII0_TXD_EN/SSLA1-B/ LCD_DATA8-B(Note 6)	PA0/BC0#/A0/MTIOC4A/CACREF/ MTIOC6D/SSLA1-B/IRQ0

144 Pin LFQFP	RX65N	RX660
98	P67/DQM1/CS7#/MTIOC7C/IRQ15	P67/MTIOC7C/IRQ15
99	P66/DQM0/CS6#/MTIOC7D	P66/MTIOC7D/IRQ14
100	P65/CKE/CS5#	P65/IRQ13
101	PE7/D15[A15/D15]/ D7[A7/D7](Note 6)/MTIOC6A/TOC1/ MISOB-B/SDHI_WP/MMC_RES#-B/ LCD_DATA9-B(Note 6)/IRQ7/AN105	PE7/D15[A15/D15]/ D7[A7/D7]/MTIOC6A/TOC1/IRQ7/AN015
102	PE6/D14[A14/D14]/D6[A6/D6](Note 6)/ MTIOC6C/TIC1/MOSIB-B/ SDHI_CD/MMC_CD-B/ LCD_DATA10-B(Note 6)/IRQ6/AN104	PE6/D14[A14/D14]/ D6[A6/D6]/MTIOC6C/TIC1/CTS4#/RTS4#/ SS4#/IRQ6/AN014
103	VCC	PK5/TXD4/SMOSI4/SSDA4
104	P70/SDCLK	P70/SCK4/IRQ0
105	VSS	PK4/RXD4/SMISO4/SSCL4
106	PE5/D13[A13/D13]/D5[A5/D5](Note 6)/ MTIOC4C/MTIOC2B/ET0_RX_CLK/ REF50CK0/RSPCKB-B/ LCD_DATA11-B(Note 6)/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/IRQ5/AN013/COMP0
107	PE4/D12[A12/D12]/D4[A4/D4](Note 6)/ MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/ SSLB0-B/LCD_DATA12-B(Note 6)/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
108	PE3/D11[A11/D11]/D3[A3/D3](Note 6)/ MTIOC4B/PO26/TOC3/POE8#/ET0_ERXD3/C TS12#/RTS12#/SS12#/MMC_D7-B/ LCD_DATA13-B(Note 6)/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/ SS12#/IRQ11/AN011
109	PE2/D10[A10/D10]/D2[A2/D2](Note 6)/ MTIOC4A/PO23/TIC3/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B(Note 6)/IRQ7-DS/AN100	PE2/D10[A10/D10]/ D2[A2/D2]/MTIOC4A/MTIOC7A/TIC3/ RXD12/SMISO12/SSCL12/RXDX12/ IRQ7-DS/AN010/CVREFC0
110	PE1/D9[A9/D9]/D1[A1/D1](Note 6)/ MTIOC4C/MTIOC3B/PO18/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B(Note 6)/ANEX1	PE1/D9[A9/D9]/ D1[A1/D1]/MTIOC4C/MTIOC3B/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/IRQ9/ AN009/CMPC00
111	PE0/D8[A8/D8]/D0[A0/D0](Note 6)/ MTIOC3D/SCK12/SSLB1-B/ MMC_D4-B/LCD_DATA16-B(Note 6)/ANEX0	PE0/D8[A8/D8]/ D0[A0/D0]/MTIOC3D/SCK12/IRQ8/AN008
112	P64/WE#/D3[A3/D3](Note 6)/CS4#	P64/D3[A3/D3]/IRQ4
113	P63/CAS#/D2[A2/D2](Note 6)/CS3#	P63/D2[A2/D2]/CS3#/IRQ3
114	P62/RAS#/D1[A1/D1](Note 6)/CS2#	P62/D1[A1/D1]/CS2#/IRQ2
115	P61/SDCS#/D0[A0/D0](Note 6)/CS1#	P61/D0[A0/D0]/CS1#/CTS9#/RTS9#/ SS9#/IRQ1
116	VSS	PK3/RXD9/SMISO9/SSCL9
117	P60/CS0#	P60/CS0#/SCK9/IRQ0
118	VCC	PK2/TXD9/SMOSI9/SSDA9
119	PD7/D7[A7/D7]/MTIC5U/POE0#/ SSLC3-A/QMI-B/QIO1-B/SDHI_D1-B/ MMC_D1-B/LCD_DATA17-B(Note 6)/ IRQ7/AN107	TRDATA3(Note 1)/PD7/ D7[A7/D7]/MTIC5U/POE0#/IRQ7/AN023

144 Pin LFQFP	RX65N	RX660
120	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/MMC_D0-B/LCD_DATA18-B(Note 6)/ IRQ6/AN106	TRDATA2(Note 1)/PD6/D6[A6/D6]/ MTIC5V/POE4#/MTIOC8A/IRQ6/AN022
121	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ POE10#/SSLC1-A/QSPCLK-B/ SDHI_CLK-B/MMC_CLK-B/ LCD_DATA19-B(Note 6)/IRQ5/AN113	TRCLK(Note 1)/PD5/D5[A5/D5]/ MTIC5W/POE10#/MTIOC8C/IRQ5/AN021
122	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B(Note 6)/ IRQ4/AN112	TRSYNC(Note 1)/PD4/D4[A4/D4]/ POE11#/MTIOC8B/IRQ4/AN020
123	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ RSPCKC-A/QIO3-B/SDHI_D3-B/MMC_D3-B/ LCD_DATA21-B(Note 6)/IRQ3/AN111	TRDATA1(Note 1)/PD3/D3[A3/D3]/ POE8#/MTIOC8D/TOC2/IRQ3/AN019
124	PD2/D2[A2/D2]/MTIOC4D/TIC2/MISOC-A/ CRX0/QIO2-B/SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B(Note 6)/IRQ2/AN110	TRDATA0(Note 1)/PD2/D2[A2/D2]/ MTIOC4D/TIC2/CRX0-B/IRQ2/AN018
125	PD1/D1[A1/D1]/MTIOC4B/POE0#/MOSIC-A/ CTX0/LCD_DATA23-B(Note 6)/IRQ1/AN109	TRDATA7(Note 1)/PD1/D1[A1/D1]/ MTIOC4B/POE0#/CTX0-B/IRQ1/AN017
126	PD0/D0[A0/D0]/POE4#/ LCD_EXTCLK-B(Note 6)/IRQ0/AN108	TRDATA6(Note 1)/PD0/D0[A0/D0]/ POE4#/IRQ0/AN016
127	P93/A19/POE0#/CTS7#/RTS7#/ SS7#/AN117	TRSYNC1(Note 1)/P93/A19/ POE0#/CTS7#/RTS7#/SS7#/IRQ11
128	P92/A18/POE4#/RXD7/SMISO7/ SSCL7/AN116	TRDATA5(Note 1)/P92/A18/POE4#/ RXD7/SMISO7/SSCL7/IRQ10
129	P91/A17/SCK7/AN115	TRDATA4(Note 1)/P91/A17/SCK7/IRQ9
130	VSS	PF7
131	P90/A16/TXD7/SMOSI7/SSDA7/AN114	P90/A16/TXD7/SMOSI7/SSDA7/IRQ0
132	VCC	PF6
133	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
134	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
135	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
136	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
137	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
138	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
139	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
140	VREFL0	VREFL0/PJ7
141	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
142	VREFH0	VREFH0/PJ6
143	AVCC0	AVCC0
144	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

Note 1. Not present on products without a JTAG.
Note 2. Not present on products provided with a JTAG.
Note 3. Not present on products without a sub-clock oscillator.
Note 4. Not present on products provided with a sub-clock oscillator.
Note 5. Not available on products without a sub-clock oscillator.
Note 6. Only available for products with code flash memory capacity of 2 MB or 1.5 MB.
Note 7. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

3.2 100-Pin Package

Table 3.2 is Comparative Listing of 100-Pin Package Pin Functions.

Table 3.2 Comparative Listing of 100-Pin Package Pin Functions

100 Pin LFQFP	RX65N	RX660
1	AVCC1	P06
2	EMLE	EMLE(Note 1)/P03(Note 2)/IRQ11(Note 2)/DA0(Note 2)
3	AVSS1	P04
4	PJ3/EDACK1/MTIOC3C/ET0_EXOUT/ CTS6#/RTS6#/SS6#/CTS0#/RTS0#/SS0#	PJ3/MTIOC3C/CTS6#/RTS6#/SS6#/CTS0#/R TS0#/SS0#/IRQ11
5	VCL	VCL
6	VBATT	PJ1/MTIOC3A
7	MD/FINED	MD/FINED/PN6
8	XCIN	XCIN(Note 3)/PH7(Note 4)
9	XCOUT	XCOUT(Note 3)/PH6(Note 4)
10	RES#	RES#
11	XTAL/P37	XTAL/P37/IRQ4
12	VSS	VSS
13	EXTAL/P36	EXTAL/P36/IRQ5
14	VCC	VCC
15	UPSEL/P35/NMI	P35/NMI
16	TRST#/P34/MTIOC0A/TMCI3/PO12/ POE10#/ET0_LINKSTA/SCK6/SCK0/IRQ4	TRST#(Note 1)/P34/MTIOC0A/TMCI3/ POE10#/SCK6/SCK0/IRQ4
17	P33/EDREQ1/MTIOC0D/TIOCD0/TMRI3/ PO11/POE4#/POE11#/RXD6/SMISO6/ SSCL6/RXD0/SMISO0/SSCL0/CRX0/ IRQ3-DS	P33/MTIOC0D/TMRI3/POE4#/POE11#/ RXD6/SMISO6/SSCL6/RXD0/SMISO0/ SSCL0/CRX0-A/IRQ3-DS
18	P32/MTIOC0C/TIOCC0/TMO3/PO10/ RTCIC2/RTCOUT/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0/USB0_VBUSEN/IRQ2-DS	P32/MTIOC0C/TMO3/RTCIC2(Note 5)/ RTCOUT(Note 5)/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/TXD0/SMOSI0/SSDA0/ CTX0-A/IRQ2-DS
19	TMS/P31/MTIOC4D/TMCI2/PO9/RTCIC1/ CTS1#/RTS1#/SS1#/SSLB0-A/IRQ1-DS	TMS(Note 1)/P31/MTIOC4D/TMCI2/ RTCIC1(Note 5)/CTS1#/RTS1#/SS1#/IRQ1-DS
20	TDI/P30/MTIOC4B/TMRI3/PO8/RTCIC0/ POE8#/RXD1/SMISO1/SSCL1/ MISOB-A/IRQ0-DS	TDI(Note 1)/P30/MTIOC4B/TMRI3/ RTCIC0(Note 5)/POE8#/RXD1/SMISO1/SSCL1/ IRQ0-DS/COMP3
21	TCK/P27/CS7#/MTIOC2B/TMCI3/ PO7/SCK1/RSPCKB-A	TCK(Note 1)/P27/CS3#/MTIOC2B/TMCI3/SCK1/ IRQ7/CVREFC3
22	TDO/P26/CS6#/MTIOC2A/TMO1/PO6/ TXD1/SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/ MOSIB-A	TDO(Note 1)/P26/CS2#/MTIOC2A/TMO1/TXD1/ SMOSI1/SSDA1/CTS3#/RTS3#/SS3#/IRQ6/ CMPC30
23	P25/CS5#/EDACK1/MTIOC4C/MTCLKB/ TIOCA4/PO5/RXD3/SMISO3/SSCL3/ ADTRG0#	P25/CS1#/MTIOC4C/MTCLKB/RXD3/ SMISO3/SSCL3/IRQ5/ADTRG0#
24	P24/CS4#/EDREQ1/MTIOC4A/MTCLKA/ TIOCB4/TMRI1/PO4/SCK3/USB0_VBUSEN	P24/CS0#/MTIOC4A/MTCLKA/TMRI1/SCK3/ IRQ12
25	P23/EDACK0/MTIOC3D/MTCLKD/TIOCD3/ PO3/TXD3/SMOSI3/SSDA3/CTS0#/RTS0#/ SS0#	P23/MTIOC3D/MTCLKD/TXD3/SMOSI3/ SSDA3/CTS0#/RTS0#/SS0#/IRQ3

100 Pin LFQFP	RX65N	RX660
26	P22/EDREQ0/MTIOC3B/MTCLKC/TIOCC3/ TMO0/PO2/SCK0/USB0_OVRCURB	P22/MTIOC3B/MTCLKC/TMO0/SCK0/IRQ15
27	P21/MTIOC1B/MTIOC4A/TIOCA3/TMCI0/ PO1/RXD0/SMISO0/SSCL0/SCL1(Note 6)/ USB0_EXICEN/IRQ9	P21/MTIOC1B/TMCI0/MTIOC4A/RXD0/ SMISO0/SSCL0/IRQ9
28	P20/MTIOC1A/TIOCB3/TMRI0/PO0/TXD0/ SMOSI0/SSDA0/SDA1(Note 6)/USB0_ID/IRQ8	P20/MTIOC1A/TMRI0/TXD0/SMOSI0/ SSDA0/IRQ8
29	P17/MTIOC3A/MTIOC3B/MTIOC4B/ TIOCB0/TCLKD/TMO1/PO15/POE8#/SCK1/T XD3/SMOSI3/SSDA3/SDA2-DS/ IRQ7/ADTRG1#	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
30	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/PO14/RTCOUT/TXD1/SMOSI1/ SSDA1/RXD3/SMISO3/SSCL3/SCL2-DS/ USB0_VBUSEN/USB0_VBUS/ USB0_OVRCURB/IRQ6/ADTRG0#	P16/MTIOC3C/MTIOC3D/TMO2/ RTCOUT(Note 5)/TXD1/SMOSI1/SSDA1/ RXD3/SMISO3/SSCL3/ MOSIA-C/SCL2/IRQ6/ADTRG0#
31	P15/MTIOC0B/MTCLKB/TIOCB2/TCLKB/ TMCI2/PO13/RXD1/SMISO1/SSCL1/SCK3/ CRX1-DS/IRQ5	P15/MTIOC0D/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/ CRX0-C/IRQ5/CMPC20
32	P14/MTIOC3A/MTCLKA/TIOCB5/TCLKA/ TMRI2/PO15/CTS1#/RTS1#/SS1#/CTX1/ USB0_OVRCURA/IRQ4	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
33	P13/MTIOC0B/TIOCA5/TMO3/PO13/TXD2/ SMOSI2/SSDA2/SDA0[FM+]/IRQ3/ADTRG1#	P13/MTIOC0B/TMO3/TXD2/SMOSI2/ SSDA2/SDA0/IRQ3
34	P12/TMCI1/RXD2/SMISO2/SSCL2/ SCL0[FM+]/IRQ2	P12/MTIC5U/TMCI1/RXD2/SMISO2/SSCL2/ SCL0/IRQ2
35	VCC_USB	PH3/MTIOC4D/TMCI0
36	USB0_DM	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
37	USB0_DP	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
38	VSS_USB	PH0/MTIOC3B/CACREF/ADTRG0#
39	P55/D0[A0/D0](Note 6)/WAIT#/EDREQ0/ MTIOC4D/TMO3/ET0_EXOUT/CRX1/IRQ10	P55/D0[A0/D0]/WAIT#/MTIOC4D/MTIOC4A/ TMO3/CRX0-D/IRQ10
40	P54/ALE/D1[A1/D1](Note 6)/EDACK0/ MTIOC4B/TMCI1/ET0_LINKSTA/CTS2#/ RTS2#/SS2#/CTX1	P54/ALE/D1[A1/D1]/MTIOC4B/TMCI1/ CTS2#/RTS2#/SS2#/CTX0-D/IRQ4
41	P53(Note 7)/BCLK	P53/BCLK/PMC0/IRQ3
42	P52/RD#/RXD2/SMISO2/SSCL2/SSLB3-A	P52/RD#/RXD2/SMISO2/SSCL2/IRQ2
43	P51/WR1#/BC1#/WAIT#/SCK2/SSLB2-A	P51/WR1#/BC1#/WAIT#/SCK2/PMC0/IRQ1
44	P50/WR0#/WR#/TXD2/SMOSI2/ SSDA2/SSLB1-A	P50/WR0#/WR#/TXD2/SMOSI2/ SSDA2/IRQ0
45	UB/PC7/A23/CS0#/MTIOC3A/MTCLKB/ TMO2/PO31/TOC0/CACREF/ET0_COL/ TXD8/SMOSI8/SSDA8/SMOSI10/SSDA10/ TXD10/MISOA-A/IRQ14	UB/PC7/CS0#/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/SSDA8/ SMOSI10/SSDA10/TXD10/ TXD010-C/SMOSI010-C/SSDA010-C/ MISOA-A/IRQ14
46	PC6/D2[A2/D2](Note 6)/A22/CS1#/MTIOC3C/ MTCLKA/TMCI2/PO30/TIC0/ET0_ETXD3/ RXD8/SMISO8/SSCL8/SMISO10/SSCL10/ RXD10/MOSIA-A/IRQ13	PC6/D2[A2/D2]/CS1#/MTIOC3C/MTCLKA/ TMCI2/TIC0/RXD8/SMISO8/SSCL8/ SMISO10/SSCL10/RXD10/RXD010-C/ SMISO010-C/SSCL010-C/MOSIA-A/IRQ13

100 Pin LFQFP	RX65N	RX660
47	PC5/D3[A3/D3](Note 6)/A21/CS2#/WAIT#/ MTIOC3B/MTCLKD/TMRI2/PO29/ ET0_ETXD2/SCK8/SCK10/RSPCKA-A	PC5/D3[A3/D3]/CS2#/WAIT#/MTIOC3B/ MTCLKD/TMRI2/MTIOC0C/SCK8/SCK10/ SCK010-C/RSPCKA-A/PMC0/IRQ5
48	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ PO25/POE0#/ET0_TX_CLK/SCK5/CTS8#/ RTS8#/SS8#/SS10#/CTS10#/RTS10#/ SSLA0-A	PC4/A20/CS3#/MTIOC3D/MTCLKC/TMCI1/ POE0#/MTIOC0A/SCK5/CTS8#/RTS8#/ SS8#/SS10#/CTS10#/RTS10#/ CTS010#-B/RTS010#-B/SS010#-B/ DE010-B/SSLA0-A/PMC0/IRQ12
49	PC3/A19/MTIOC4D/TCLKB/PO24/ ET0_TX_ER/TXD5/SMOSI5/SSDA5	PC3/A19/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
50	PC2/A18/MTIOC4B/TCLKA/PO21/ ET0_RX_DV/RXD5/SMISO5/SSCL5/ SSLA3-A	PC2/A18/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
51	PC1/A17/MTIOC3A/TCLKD/PO18/ ET0_ERXD2/SCK5/SSLA2-A/IRQ12	PC1/A17/MTIOC3A/SCK5/ TXD011-C/SMOSI011-C/ SSDA011-C/TXDA011-C/SSLA2-A/IRQ12
52	PC0/A16/MTIOC3C/TCLKC/PO17/ ET0_ERXD3/CTS5#/RTS5#/SS5#/ SSLA1-A/IRQ14	PC0/A16/MTIOC3C/CTS5#/RTS5#/SS5#/ RXD011-C/SMISO011-C/SSCL011-C/ SSLA1-A/IRQ14
53	PB7/A15/MTIOC3B/TIOCB5/PO31/ ET0_CRS/RMII0_CRS_DV/TXD9/SMOSI9/ SSDA9/SMOSI11/SSDA11/TXD11/ SDSI_D1-B	PB7/A15/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/ TXD011-B/SMOSI011-B/SSDA011-B/IRQ15
54	PB6/A14/MTIOC3D/TIOCA5/PO30/ ET0_ETXD1/RMII0_TXD1/RXD9/ SMISO9/SSCL9/SMISO11/SSCL11/RXD11/ SDSI_D0-B	PB6/A14/MTIOC3D/RXD9/SMISO9/SSCL9/S MISO11/SSCL11/RXD11/ RXD011-B/SMISO011-B/SSCL011-B/IRQ6
55	PB5/A13/MTIOC2A/MTIOC1B/TIOCB4/ TMRI1/PO29/POE4#/ET0_ETXD0/ RMII0_TXD0/SCK9/SCK11/ SDSI_CLK-B/LCD_CLK-B(Note 6)	PB5/A13/MTIOC2A/MTIOC1B/TMRI1/ POE4#/TOC2/SCK9/SCK11/ SCK011-B/IRQ13
56	PB4/A12/TIOCA4/PO28/ET0_TX_EN/ RMII0_TXD_EN/CTS9#/RTS9#/SS9#/ SS11#/CTS11#/RTS11#/SDSI_CMD-B/ LCD_TCON0-B(Note 6)	PB4/A12/CTS9#/RTS9#/SS9#/SS11#/ CTS11#/RTS11#/CTS011#-B/ RTS011#-B/SS011#-B/DE011-B/IRQ4
57	PB3/A11/MTIOC0A/MTIOC4A/TIOCD3/ TCLKD/TMO0/PO27/POE11#/ET0_RX_ER/R MII0_RX_ER/SCK6/SDSI_D3-B/ LCD_TCON1-B(Note 6)	PB3/A11/MTIOC0A/MTIOC4A/TMO0/ POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
58	PB2/A10/TIOCC3/TCLKC/PO26/ ET0_RX_CLK/REF50CK0/CTS6#/RTS6#/ SS6#/SDSI_D2-B/LCD_TCON2-B(Note 6)	PB2/A10/CTS4#/RTS4#/SS4#/CTS6#/ RTS6#/SS6#/IRQ2
59	PB1/A9/MTIOC0C/MTIOC4C/TIOCB3/ TMCI0/PO25/ET0_ERXD0/RMII0_RXD0/ TXD6/SMOSI6/SSDA6/ LCD_TCON3-B(Note 6)/IRQ4-DS	PB1/A9/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
60	VCC	VCC
61	PB0/A8/MTIC5W/TIOCA3/PO24/ ET0_ERXD1/RMII0_RXD1/RXD6/SMISO6/ SSCL6/LCD_DATA0-B(Note 6)/IRQ12	PB0/A8/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/ RSPCKA-C/IRQ12

100 Pin LFQFP	RX65N	RX660
62	VSS	VSS
63	PA7/A7/TIOCB2/PO23/ET0_WOL/MISOA-B/ LCD_DATA1-B(Note 6)	PA7/A7/MISOA-B/IRQ7
64	PA6/A6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ PO22/POE10#/ET0_EXOUT/CTS5#/RTS5#/S S5#/MOSIA-B/LCD_DATA2-B(Note 6)	PA6/A6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
65	PA5/A5/MTIOC6B/TIOCB1/PO21/ ET0_LINKSTA/RSPCKA-B/ LCD_DATA3-B(Note 6)	PA5/A5/MTIOC6B/RSPCKA-B/IRQ5
66	PA4/A4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ PO20/ET0_MDC/TXD5/SMOSI5/SSDA5/ SSLA0-B/LCD_DATA4-B(Note 6)/IRQ5-DS	PA4/A4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0
67	PA3/A3/MTIOC0D/MTCLKD/TIOCD0/ TCLKB/PO19/ET0_MDIO/RXD5/SMISO5/ SSCL5/LCD_DATA5-B(Note 6)/IRQ6-DS	PA3/A3/MTIOC0D/MTCLKD/MTIC5V/ MTIOC4D/RXD5/SMISO5/SSCL5/ IRQ6-DS/CMPC10
68	PA2/A2/MTIOC7A/PO18/RXD5/SMISO5/ SSCL5/SSLA3-B/LCD_DATA6-B(Note 6)	PA2/A2/MTIOC7A/RXD5/SMISO5/SSCL5/ RXD12/SMISO12/SSCL12/RXDX12/ SSLA3-B/IRQ10
69	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ TIOCB0/PO17/ET0_WOL/SCK5/ SSLA2-B/LCD_DATA7-B(Note 6)/IRQ11	PA1/A1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/ IRQ11/ADTRG0#
70	PA0/BC0#/A0/MTIOC4A/MTIOC6D/TIOCA0/ PO16/CACREF/ET0_TX_EN/RMII0_TXD_EN/ SSLA1-B/LCD_DATA8-B(Note 6)	PA0/BC0#/A0/MTIOC4A/CACREF/ MTIOC6D/SSLA1-B/IRQ0
71	PE7/D15[A15/D15]/D7[A7/D7](Note 6)/ MTIOC6A/TOC1/MISOB-B/SDHI_WP/ MMC_RES#-B/LCD_DATA9-B(Note 6)/ IRQ7/AN105	PE7/D15[A15/D15]/D7[A7/D7]/MTIOC6A/ TOC1/IRQ7/AN015
72	PE6/D14[A14/D14]/D6[A6/D6](Note 6)/ MTIOC6C/TIC1/MOSIB-B/SDHI_CD/ MMC_CD-B/LCD_DATA10-B(Note 6)/ IRQ6/AN104	PE6/D14[A14/D14]/D6[A6/D6]/MTIOC6C/ TIC1/CTS4#/RTS4#/SS4#/IRQ6/AN014
73	PE5/D13[A13/D13]/D5[A5/D5](Note 6)/ MTIOC4C/MTIOC2B/ET0_RX_CLK/ REF50CK0/RSPCKB-B/ LCD_DATA11-B(Note 6)/IRQ5/AN103	PE5/D13[A13/D13]/D5[A5/D5]/MTIOC4C/ MTIOC2B/IRQ5/AN013/COMP0
74	PE4/D12[A12/D12]/D4[A4/D4](Note 6)/ MTIOC4D/MTIOC1A/PO28/ET0_ERXD2/ SSLB0-B/LCD_DATA12-B(Note 6)/AN102	PE4/D12[A12/D12]/D4[A4/D4]/MTIOC4D/ MTIOC1A/MTIOC4A/MTIOC7D/ IRQ12/AN012
75	PE3/D11[A11/D11]/D3[A3/D3](Note 6)/ MTIOC4B/PO26/TOC3/POE8#/ET0_ERXD3/ CTS12#/RTS12#/SS12#/ MMC_D7-B/LCD_DATA13-B(Note 6)/AN101	PE3/D11[A11/D11]/D3[A3/D3]/MTIOC4B/ POE8#/MTIOC1B/TOC3/CTS12#/RTS12#/ SS12#/IRQ11/AN011
76	PE2/D10[A10/D10]/D2[A2/D2](Note 6)/ MTIOC4A/PO23/TIC3/RXD12/SMISO12/ SSCL12/RXDX12/SSLB3-B/MMC_D6-B/ LCD_DATA14-B(Note 6)/IRQ7-DS/AN100	PE2/D10[A10/D10]/D2[A2/D2]/MTIOC4A/ MTIOC7A/TIC3/RXD12/SMISO12/SSCL12/ RXDX12/IRQ7-DS/AN010/CVREFC0

100 Pin LFQFP	RX65N	RX660
77	PE1/D9[A9/D9]/D1[A1/D1](Note 6)/ MTIOC4C/MTIOC3B/PO18/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLB2-B/MMC_D5-B/ LCD_DATA15-B(Note 6)/ANEX1	PE1/D9[A9/D9]/D1[A1/D1]/MTIOC4C/ MTIOC3B/TXD12/SMOSI12/SSDA12/ TXDX12/SIOX12/IRQ9/AN009/CMPC00
78	PE0/D8[A8/D8]/D0[A0/D0](Note 6)/ MTIOC3D/SCK12/SSLB1-B/MMC_D4-B/ LCD_DATA16-B(Note 6)/ANEX0	PE0/D8[A8/D8]/D0[A0/D0]/MTIOC3D/ SCK12/IRQ8/AN008
79	PD7/D7[A7/D7]/MTIC5U/POE0#/ SSLC3-A/QMI-B/QIO1-B/SDHI_D1B/ MMC_D1-B/LCD_DATA17-B(Note 6)/ IRQ7/AN107	PD7/D7[A7/D7]/MTIC5U/POE0#/ IRQ7/AN023
80	PD6/D6[A6/D6]/MTIC5V/MTIOC8A/POE4#/ SSLC2-A/QMO-B/QIO0-B/SDHI_D0-B/ MMC_D0-B/LCD_DATA18-B(Note 6)/ IRQ6/AN106	PD6/D6[A6/D6]/MTIC5V/POE4#/MTIOC8A/ IRQ6/AN022
81	PD5/D5[A5/D5]/MTIC5W/MTIOC8C/ POE10#/SSLC1-A/QSPCLK-B/SDHI_CLK-B/ MMC_CLK-B/LCD_DATA19-B(Note 6)/ IRQ5/AN113	PD5/D5[A5/D5]/MTIC5W/POE10#/ MTIOC8C/IRQ5/AN021
82	PD4/D4[A4/D4]/MTIOC8B/POE11#/ SSLC0-A/QSSL-B/SDHI_CMD-B/ MMC_CMD-B/LCD_DATA20-B(Note 6)/ IRQ4/AN112	PD4/D4[A4/D4]/POE11#/MTIOC8B/IRQ4/ AN020
83	PD3/D3[A3/D3]/MTIOC8D/TOC2/POE8#/ RSPCKC-A/QIO3-B/SDHI_D3-B/ MMC_D3-B/LCD_DATA21-B(Note 6)/ IRQ3/AN111	PD3/D3[A3/D3]/POE8#/MTIOC8D/TOC2/ IRQ3/AN019
84	PD2/D2[A2/D2]/MTIOC4D/TIC2/ MISOC-A/CRX0/QIO2-B/ SDHI_D2-B/MMC_D2-B/ LCD_DATA22-B(Note 6)/IRQ2/AN110	PD2/D2[A2/D2]/MTIOC4D/TIC2/ CRX0-B/IRQ2/AN018
85	PD1/D1[A1/D1]/MTIOC4B/POE0#/ MOSIC-A/CTX0/ LCD_DATA23-B(Note 6)/IRQ1/AN109	PD1/D1[A1/D1]/MTIOC4B/POE0#/ CTX0-B/IRQ1/AN017
86	PD0/D0[A0/D0]/POE4#/ LCD_EXTCLK-B(Note 6)/IRQ0/AN108	PD0/D0[A0/D0]/POE4#/IRQ0/AN016
87	P47/IRQ15-DS/AN007	P47/IRQ15-DS/AN007
88	P46/IRQ14-DS/AN006	P46/IRQ14-DS/AN006
89	P45/IRQ13-DS/AN005	P45/IRQ13-DS/AN005
90	P44/IRQ12-DS/AN004	P44/IRQ12-DS/AN004
91	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
92	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
93	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
94	VREFL0	VREFL0/PJ7
95	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
96	VREFH0	VREFH0/PJ6
97	AVCC0	AVCC0
98	P07/IRQ15/ADTRG0#	P07/IRQ15/ADTRG0#

100 Pin LFQFP	RX65N	RX660
99	AVSS0	AVSS0
100	P05/IRQ13/DA1	P05/IRQ13/DA1

Note 1. Not present on products without a JTAG.
Note 2. Not present on products provided with a JTAG.
Note 3. Not present on products without a sub-clock oscillator.
Note 4. Not present on products provided with a sub-clock oscillator.
Note 5. Not available on products without a sub-clock oscillator.
Note 6. Only available for products with code flash memory capacity of 2 MB or 1.5 MB.
Note 7. The BCLK function is multiplexed with the I/O port function for pin P53, so the port function is not available if the external bus is enabled.

3.3 64-Pin Package

Table 3.3 is a Comparative Listing of 64-Pin Package Pin Functions.

Table 3.3 Comparative Listing of 64-Pin Package Pin Functions

64-Pin LFQFP/ LQFP	RX65N	RX660
1	AVCC1	P03/IRQ11/DA0
2	EMLE	VCL
3	AVSS1	MD/FINED/PN6
4	VCL	XCIN(Note 1)/PH7(Note 2)
5	VBATT	XCOUT(Note 1)/PH6(Note 2)
6	MD/FINED	RES#
7	XCIN	XTAL/P37/IRQ4
8	XCOUT	VSS
9	RES#	EXTAL/P36/IRQ5
10	XTAL/P37	VCC
11	VSS	P35/NMI
12	EXTAL/P36	P32/MTIOC0C/TMO3/RTCIC2(Note 3)/ RTCOUT(Note 3)/POE0#/POE10#/TXD6/ SMOSI6/SSDA6/CTX0-A/IRQ2-DS
13	VCC	P31/MTIOC4D/TMCI2/RTCIC1(Note 3)/CTS1#/ RTS1#/SS1#/IRQ1-DS
14	UPSEL/P35/NMI	P30/MTIOC4B/TMRI3/RTCIC0(Note 3)/POE8#/ RXD1/SMISO1/SSCL1/IRQ0-DS/COMP3
15	TRST#/P34/MTIOC0A/TMCI3/POE10#/IRQ4	P27/MTIOC2B/TMCI3/SCK1/IRQ7/ CVREFC3
16	TDI/P30/MTIOC4B/TMRI3/RTCIC0/POE8#/ RXD1/SMISO1/SSCL1/MISOB-A/IRQ0-DS	P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/SS3#/IRQ6/CMPC30
17	TMS/P31/MTIOC4D/TMCI2/RTCIC1/CTS1#/ RTS1#/SS1#/SSLB0-A/IRQ1-DS	P17/MTIOC3A/MTIOC3B/TMO1/POE8#/ MTIOC4B/SCK1/TXD3/SMOSI3/SSDA3/ MISOA-C/SDA2/IRQ7/COMP2
18	TDO/P26/MTIOC2A/TMO1/TXD1/SMOSI1/ SSDA1/CTS3#/RTS3#/MOSIB-A	P16/MTIOC3C/MTIOC3D/TMO2/ RTCOUT(Note 3)/TXD1/SMOSI1/SSDA1/RXD3/ SMISO3/SSCL3/MOSIA-C/SCL2/ IRQ6/ADTRG0#
19	TCK/P27/MTIOC2B/TMCI3/SCK1/ RSPCKB-A	P15/MTIOC0B/MTCLKB/TMCI2/RXD1/ SMISO1/SSCL1/SCK3/ CRX0-C/IRQ5/CMPC20
20	P17/MTIOC3A/ MTIOC3B/MTIOC4B/TIOCB0/ TCLKD/TMO1/POE8#/SCK1/TXD3/SSDA3/ SDA2-DS/IRQ7/ADTRG1#	P14/MTIOC3A/MTCLKA/TMRI2/CTS1#/ RTS1#/SS1#/CTX0-C/IRQ4/CVREFC2
21	P16/MTIOC3C/MTIOC3D/TIOCB1/TCLKC/ TMO2/RTCOUT/TXD1/SMOSI1/SSDA1/ RXD3/SSCL3/SCL2-DS/USB0_VBUS/ IRQ6/ADTRG0#	PH3/MTIOC4D/TMCI0
22	P13/MTIOC0B/TIOCA5/TMO3/TXD2/ SSDA2/SDA0[FM+]/IRQ3/ADTRG1#	PH2/MTIOC4C/TMRI0/TOC1/IRQ1
23	P12/TMCI1/RXD2/SSCL2/SCL0[FM+]/IRQ2	PH1/MTIOC3D/TMO0/TIC1/IRQ0/ADST0
24	VCC_USB	PH0/MTIOC3B/CACREF/ADTRG0#

64-Pin LFQFP/ LQFP	RX65N	RX660
25	USB0_DM	P55/MTIOC4D/MTIOC4A/TMO3/ CRX0-D/IRQ10
26	USB0_DP	P54/MTIOC4B/TMCI1/CTX0-D/IRQ4
27	VSS_USB	UB/PC7/MTIOC3A/MTCLKB/TMO2/ CACREF/TOC0/TXD8/SMOSI8/ SSDA8/SMOSI10/SSDA10/TXD10/ TXD010-C/SMOSI010-C/ SSDA010-C/MISOA-A/IRQ14
28	P53	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ RXD010-C/SMISO010-C/SSCL010-C/ MOSIA-A/IRQ13
29	UB/PC7/MTIOC3A/MTCLKB/TMO2/TOC0/ CACREF/TXD8/SMOSI8/SSDA8/SMOSI10/ SSDA10/TXD10/MISOA-A/IRQ14	PC5/MTIOC3B/MTCLKD/TMRI2/MTIOC0C/ SCK8/SCK10/SCK010-C/RSPCKA-A/ PMC0/IRQ5
30	PC6/MTIOC3C/MTCLKA/TMCI2/TIC0/RXD8/ SMISO8/SSCL8/SMISO10/SSCL10/RXD10/ MOSIA-A/IRQ13	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ MTIOC0A/SCK5/CTS8#/RTS8#/SS8#/ SS10#/CTS10#/RTS10#/ CTS010#-B/RTS010#-B/SS010#-B/ DE010-B/SSLA0-A/PMC0/IRQ12
31	PC5/MTIOC3B/MTCLKD/TMRI2/SCK8/ SCK10/RSPCKA-A	PC3/MTIOC4D/TXD5/SMOSI5/SSDA5/ PMC0/IRQ11
32	PC4/MTIOC3D/MTCLKC/TMCI1/POE0#/ CTS8#/RTS8#/SS8#/SS10#/CTS10#/ RTS10#/SSLA0-A	PC2/MTIOC4B/RXD5/SMISO5/SSCL5/ TXDB011-A/SSLA3-A/IRQ10
33	PC1/MTIOC3A/TCLKD/SSLA2-A/IRQ12	PB7/MTIOC3B/TXD9/SMOSI9/SSDA9/ SMOSI11/SSDA11/TXD11/TXD011-B/ SMOSI011-B/SSDA011-B/IRQ15
34	PC0/MTIOC3C/TCLKC/SSLA1-A/IRQ14	PB6/MTIOC3D/RXD9/SMISO9/SSCL9/ SMISO11/SSCL11/RXD11/RXD011-B/ SMISO011-B/SSCL011-B/IRQ6
35	PB7/MTIOC3B/TIOCB5/TXD9/SSDA9/ SSDA11/TXD11	PB5/MTIOC2A/MTIOC1B/TMRI1/POE4#/ TOC2/SCK9/SCK11/SCK011-B/IRQ13
36	PB6/MTIOC3D/TIOCA5/RXD9/SSCL9/ SSCL11/RXD11	PB3/MTIOC0A/MTIOC4A/TMO0/ POE11#/TIC2/SCK4/SCK6/PMC0/IRQ3
37	PB5/MTIOC2A/MTIOC1B/TIOCB4/TMRI1/ POE4#/SCK9/SCK11	PB1/MTIOC0C/MTIOC4C/TMCI0/TXD4/ SMOSI4/SSDA4/TXD6/SMOSI6/SSDA6/ IRQ4-DS/COMP1
38	VCC	VCC
39	VSS	PB0/MTIC5W/MTIOC3D/RXD4/SMISO4/ SSCL4/RXD6/SMISO6/SSCL6/RSPCKA-C/ IRQ12
40	PA7/TIOCB2	VSS
41	PA6/MTIC5V/MTCLKB/TIOCA2/TMCI3/ POE10#/CTS5#/RTS5#/SS5#	PA6/MTIC5V/MTCLKB/TMCI3/POE10#/ MTIOC3D/MTIOC6B/CTS5#/RTS5#/SS5#/ CTS12#/RTS12#/SS12#/MOSIA-B/IRQ14
42	PA4/MTIC5U/MTCLKA/TIOCA1/TMRI0/ TXD5/SMOSI5/SSDA5/IRQ5-DS	PA4/MTIC5U/MTCLKA/TMRI0/MTIOC4C/ MTIOC7C/TXD5/SMOSI5/SSDA5/TXD12/ SMOSI12/SSDA12/TXDX12/SIOX12/ SSLA0-B/IRQ5-DS/CVREFC1/ADST0

64-Pin LFQFP/ LQFP	RX65N	RX660
43	PA2/MTIOC7A/RXD5/SMISO5/SSCL5	PA3/MTIOC0D/MTCLKD/MTIC5V/MTIOC4D/ RXD5/SMISO5/SSCL5/IRQ6-DS/CMPC10
44	PA1/MTIOC0B/ MTCLKC/MTIOC7B/TIOCB0/ SCK5/IRQ11	PA1/MTIOC0B/MTCLKC/MTIOC7B/ MTIOC3B/SCK5/SCK12/SSLA2-B/IRQ11/ ADTRG0#
45	PE7/MTIOC6A/TOC1/SDHI_WP/IRQ7	PA0/MTIOC4A/CACREF/MTIOC6D/ SSLA1-B/IRQ0
46	PE6/MTIOC6C/TIC1/SDHI_CD/IRQ6	PE5/MTIOC4C/MTIOC2B/IRQ5/AN013/ COMP0
47	PE2/MTIOC4A/TIC3/RXD12/SSCL12/ RXDX12/IRQ7-DS	PE4/MTIOC4D/MTIOC1A/MTIOC4A/ MTIOC7D/IRQ12/AN012
48	PE1/MTIOC4C/MTIOC3B/TXD12/SSDA12/ TXDX12/SIOX12/ANEX1	PE3/MTIOC4B/POE8#/MTIOC1B/TOC3/ CTS12#/RTS12#/SS12#/IRQ11/AN011
49	PE0/MTIOC3D/SCK12/ANEX0	PE2/MTIOC4A/MTIOC7A/TIC3/RXD12/ SMISO12/SSCL12/RXDX12/IRQ7-DS/ AN010/CVREFC0
50	PD7/MTIC5U/POE0#/QMI-B/ QIO1-B/SDHI_D1-B/IRQ7/AN107	PE1/MTIOC4C/MTIOC3B/TXD12/SMOSI12/ SSDA12/TXDX12/SIOX12/IRQ9/AN009/ CMPC00
51	PD6/MTIC5V/MTIOC8A/POE4#/ QMO-B/QIO0-B/SDHI_D0-B/IRQ6/AN106	PE0/MTIOC3D/SCK12/IRQ8/AN008
52	PD5/MTIC5W/MTIOC8C/POE10#/ QSPCLK-B/SDHI_CLK-B/IRQ5/AN113	P47/IRQ15-DS/AN007
53	PD4/MTIOC8B/POE11#/ QSSL-B/SDHI_CMD-B/IRQ4/AN112	P46/IRQ14-DS/AN006
54	PD3/MTIOC8D/TOC2/POE8#/ QIO3-B/SDHI_D3-B/IRQ3/AN111	P45/IRQ13-DS/AN005
55	PD2/MTIOC4D/TIC2/QIO2-B/ SDHI_D2-B/IRQ2/AN110	P44/IRQ12-DS/AN004
56	P43/IRQ11-DS/AN003	P43/IRQ11-DS/AN003
57	P42/IRQ10-DS/AN002	P42/IRQ10-DS/AN002
58	P41/IRQ9-DS/AN001	P41/IRQ9-DS/AN001
59	VREFL0	VREFL0/PJ7
60	P40/IRQ8-DS/AN000	P40/IRQ8-DS/AN000
61	VREFH0	VREFH0/PJ6
62	AVCC0	AVCC0
63	AVSS0	P07/IRQ15/ADTRG0#
64	P05/IRQ13/DA1	AVSS0

Note 1. Not present on products without a sub-clock oscillator.
Note 2. Not present on products provided with a sub-clock oscillator.
Note 3. Not available on products without a sub-clock oscillator.

4. Important Information when Migrating Between MCUs

This section presents important information on differences between the RX660 Group and the RX65N Group.

4.1 Notes on Functional Design, presents information regarding the software.

4.1 Notes on Functional Design

Some software that runs on the RX65N Group is compatible with the RX660 Group. Nevertheless, appropriate caution must be exercised due to differences in aspects such as operation timing and electrical characteristics.

Software-related considerations regarding function settings that differ between the RX660 Group and RX65N Group are as follows:

For differences between modules and functions, refer to 2, Comparative Overview of Specifications For further information, refer to the User's Manual: Hardware of each MCU group, listed in 5, Reference Documents.

4.1.1 RIIC Operating Voltage Setting

When using the RIIC on the RX660 Group, it is necessary to specify the power supply voltage range to preserve the slope characteristics. VCC is set to a value of 4.5 V or greater by default. If it is set to a value less than 4.5 V, make sure to change the voltage range before activating the RIIC. For details, refer to the description of the VOLSR.RICVLS bit in RX660 Group User's Manual: Hardware.

4.1.2 Performing RAM Self-Diagnostics on Save Register Banks

On the RX660 Group save register banks are configured in the RAM.

The save register banks are provided with a buffer, so when a SAVE instruction is used to write data to a register and then a RSTR instruction is used to read data from the same register, the data is actually read from the buffer and not from the RAM memory cells.

When performing self-diagnostics on the RAM in a save register bank, use the following sequence of steps for checking the written data in order to prevent the data from being read from the buffer:

1. Use the SAVE instruction to write data to the bank that is the target of the diagnostic test.
2. Use the SAVE instruction to write data to a bank other than that written to in step 1.
3. Use the RSTR instruction to read data from the bank written to in step 1.

4.1.3 Restrictions on Compare Function

The compare function of the 12-bit A/D converter on the RX660 Group is subject to the following restrictions.

1. The compare function cannot be used together with the self-diagnosis function or double trigger mode. (The compare function is not available for the ADRD, ADDBLDR, ADDBLDRA, and ADDBLDRB registers.)
2. It is necessary to specify single scan mode when using match or mismatch event outputs.
3. When the temperature sensor or internal reference voltage is selected for window A, window B operations are disabled.
4. When the temperature sensor or internal reference voltage is selected for window B, window A operations are disabled.
5. It is not possible to set the same channel for window A and window B.
6. It is necessary to set the reference voltage values such that the high-side reference voltage value is equal to or larger than the low-side reference voltage value.

4.1.4 Initialization of Port Direction Register (PDR)

The method of initializing the PDR register differs between the RX660 Group and RX65N Group, even on products with the same pin count.

4.1.5 MTIOC Pin Output Level when Counter Stops

To generate PWM waveforms in complementary PWM mode on the RX660 Group, MTU4.TGRA (MTU7.TGRA) compare match detection is performed with not only MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB). Therefore, TRGA4N (TRGA7N) is also generated when a compare match with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB) occurs. When operating MTU3 and MTU4 (MTU6 and MTU7) in complementary PWM mode to generate A/D conversion start requests, use compare match between MTU4.TCNT (MTU7.TCNT) and MTU4.TADCORA or TADCORB (MTU7.TADCORA or TADCORB) as the A/D conversion start request.

4.1.6 A/D Conversion Start Requests in Complementary PWM Mode

To generate PWM waveforms in complementary PWM mode on the RX660 Group, MTU4.TGRA (MTU7.TGRA) compare match detection is performed with not only MTU4.TCNT (MTU7.TCNT) but also with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB). Therefore, TRGA4N (TRGA7N) is also generated when a compare match with MTU3.TCNT (MTU6.TCNT) or TCNTSA (TCNTSB) occurs.

When operating MTU3 and MTU4 (MTU6 and MTU7) in complementary PWM mode to generate A/D conversion start requests, use compare match between MTU4.TCNT

(MTU7.TCNT) and MTU4.TADCORA or TADCORB (MTU7.TADCORA or TADCORB) as the A/D conversion start request.

4.1.7 High-Impedance Control of Unselected MTU Pins

On the RX660 Group, when high-impedance control is enabled for MTU pins in the POECR1 or POECR2 register and the control conditions are met, output on the pins multiplexed with the MTU function enters the high-impedance state regardless of whether or not the MTU function is selected.

To prevent pin output from entering the high-impedance state unexpectedly, make settings such that the MTU pins selected in the PmnPFS register of the MPC and the MTU pins selected in the pin selection register of the POE3 match.

4.1.8 A/D Scan Conversion End Interrupt Generation

On the RX660 Group, when a scan is started by a software trigger and the ADIE bit has been set to 1, an A/D scan conversion end interrupt is generated when the scan ends, even if double trigger mode is selected.

4.1.9 Input Buffer Control by DIRQnE Bits (n = 0 to 15)

On the RX660 Group, setting a DPSIERy.DIRQnE (y = 0 or 1, n = 0 to 15) bit to 1 enables the input buffer of the corresponding pin among IRQ0-DS to IRQ15-DS. Note that once the input buffer is enabled, inputs on these pins are sent to the corresponding DPSIFRy.DIRQnF (y = 0 or 1, n = 0 to 15) bits, but they are not sent to the interrupt controller, peripheral modules, and I/O ports.

4.1.10 Scan Conversion Time of 12-Bit A/D Converter

The scan conversion time differs between the RX65N Group and RX660 Group. The scan conversion time (tSCAN) for each group of a single scan where the number of selected channels is n is expressed by the equations below. For details, refer to the description of the 12-bit A/D converter analog input sampling time and scan conversion time in the User's Manual: Hardware of the RX65N Group and RX660 Group, listed in section 5, Reference Documents.

RX65N: $t_{SCAN} = t_D + t_{SPLSH} + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

RX660: $t_{SCAN} = t_D + (t_{DIS} \times n) + t_{DIAG} + (t_{CONV} \times n) + t_{ED}$

t_{SCAN} (when converting temperature sensor output or internal reference voltage) $= t_D + (t_{ADIS} \times m) + (t_{CONV} \times m) + t_{ED}$

t_D	Start-of-scanning-delay time
t_{SPLSH}	Channel-dedicated sample and hold circuit processing time
t_{SPL}	Sampling time
t_{DIS}	Disconnection detection assist processing time
t_{DIAG}	Self-diagnosis A/D conversion processing time
t_{CONV}	A/D conversion processing time
t_{ED}	End-of-scanning-delay time
t_{ADIS}	Auto-discharge processing time during A/D conversion of temperature sensor output and internal reference voltage

4.1.11 D/A Converter Settings

When configuring D/A converter settings on the RX660 Group, first set comparator C as the output destination in the D/A destination select register (DADSELR) and wait for the D/A converter output to stabilize before enabling comparator operation. Similarly, stop the comparator temporarily before making changes to the settings of the D/A converter, then wait for the D/A converter output to stabilize before enabling comparator operation.

4.1.12 Comparator C Operation in Module Stop State

On the RX660 Group the analog circuits of comparator C do not stop operating if a transition to the module stop state is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in the module stop state, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.13 Comparator C Operation in Software Standby Mode

On the RX660 Group, the analog circuits of comparator C do not stop operating if a transition to software standby mode is made while comparator C is operating, so the analog power current associated with comparator C remains unchanged. If it is necessary to reduce analog power current consumption in software standby mode, stop operation of comparator C by clearing the CMPCTL.HCMPON bit to 0.

4.1.14 Timer Mode Register Setting for ELC Event Input

To set the MTU to ELC action operation on the RX660 Group, set the timer mode register (TMDR) of the relevant channel to its initial value (00h).

4.1.15 Clock Frequency Settings

On the RX65N Group, the value of the ROMWT register must be changed if the ICLK frequency exceeds 50 MHz.

Note that the following restrictions apply with the RX660 group:

- The system clock (ICLK) and peripheral module clocks A, B, and D (PCLKA, PCLKB, and PCLKD) must be set within the following ranges:
  - PCLKA ≥ PCLKB
  - PCLKB: PCLKD = 1:1 or 2:1 or 4:1 or 1:2

- When CANFD is used:

Clock frequency setting restrictions when using CANFD:

- PCLKA: PCLKB = 2:1
- ICLK ≥ BCLK and PCLKA ≥ PCLKB

5. Reference Documents

User's Manual: Hardware

RX65N Group User's Manual: Hardware Rev2.30 (R01UH0590EJ0230)
(The latest version can be downloaded from the Renesas Electronics website.)

RX660 Group User's Manual: Hardware Rev1.00 (R01UH0937EJ0100)
(The latest version can be downloaded from the Renesas Electronics website.)

Technical Update/Technical News
(The latest information can be downloaded from the Renesas Electronics website.)

Related Technical Updates

This module reflects the content of the following technical updates:

- TN-RX*-A0215A/E
- TN-RX*-A0217A/E
- TN-RX*-A0223A/E
- TN-RX*-A0224B/E
- TN-RX*-A0226A/E
- TN-RX*-A0227A/E
- TN-RX*-A0233A/E
- TN-RX*-A0235B/E
- TN-RX*-A0236B/E
- TN-RX*-A0248A/E
- TN-RX*-A0250A/E
- TN-RX*-A0257A/E

Revision History

Rev.	Date	Description	
		Page	Summary
1.00	May.31.22	—	First edition issued

General Precautions in the Handling of Microprocessing Unit and Microcontroller Unit Products

The following usage notes are applicable to all Microprocessing unit and Microcontroller unit products from Renesas. For detailed usage notes on the products covered by this document, refer to the relevant sections of the document as well as any technical updates that have been issued for the products.

1. Precaution against Electrostatic Discharge (ESD)

   A strong electrical field, when exposed to a CMOS device, can cause destruction of the gate oxide and ultimately degrade the device operation. Steps must be taken to stop the generation of static electricity as much as possible, and quickly dissipate it when it occurs. Environmental control must be adequate. When it is dry, a humidifier should be used. This is recommended to avoid using insulators that can easily build up static electricity. Semiconductor devices must be stored and transported in an anti-static container, static shielding bag or conductive material. All test and measurement tools including work benches and floors must be grounded. The operator must also be grounded using a wrist strap. Semiconductor devices must not be touched with bare hands. Similar precautions must be taken for printed circuit boards with mounted semiconductor devices.
2. Processing at power-on

   The state of the product is undefined at the time when power is supplied. The states of internal circuits in the LSI are indeterminate and the states of register settings and pins are undefined at the time when power is supplied. In a finished product where the reset signal is applied to the external reset pin, the states of pins are not guaranteed from the time when power is supplied until the reset process is completed. In a similar way, the states of pins in a product that is reset by an on-chip power-on reset function are not guaranteed from the time when power is supplied until the power reaches the level at which resetting is specified.
3. Input of signal during power-off state

   Do not input signals or an I/O pull-up power supply while the device is powered off. The current injection that results from input of such a signal or I/O pull-up power supply may cause malfunction and the abnormal current that passes in the device at this time may cause degradation of internal elements. Follow the guideline for input signal during power-off state as described in your product documentation.
4. Handling of unused pins

   Handle unused pins in accordance with the directions given under handling of unused pins in the manual. The input pins of CMOS products are generally in the high-impedance state. In operation with an unused pin in the open-circuit state, extra electromagnetic noise is induced in the vicinity of the LSI, an associated shoot-through current flows internally, and malfunctions occur due to the false recognition of the pin state as an input signal become possible.
5. Clock signals

   After applying a reset, only release the reset line after the operating clock signal becomes stable. When switching the clock signal during program execution, wait until the target clock signal is stabilized. When the clock signal is generated with an external resonator or from an external oscillator during a reset, ensure that the reset line is only released after full stabilization of the clock signal. Additionally, when switching to a clock signal produced with an external resonator or by an external oscillator while program execution is in progress, wait until the target clock signal is stable.
6. Voltage application waveform at input pin

   Waveform distortion due to input noise or a reflected wave may cause malfunction. If the input of the CMOS device stays in the area between V_{IL} (Max.) and V_{IH} (Min.) due to noise, for example, the device may malfunction. Take care to prevent chattering noise from entering the device when the input level is fixed, and also in the transition period when the input level passes through the area between V_{IL} (Max.) and V_{IH} (Min.).
7. Prohibition of access to reserved addresses

   Access to reserved addresses is prohibited. The reserved addresses are provided for possible future expansion of functions. Do not access these addresses as the correct operation of the LSI is not guaranteed.
8. Differences between products

   Before changing from one product to another, for example to a product with a different part number, confirm that the change will not lead to problems. The characteristics of a microprocessing unit or microcontroller unit products in the same group but having a different part number might differ in terms of internal memory capacity, layout pattern, and other factors, which can affect the ranges of electrical characteristics, such as characteristic values, operating margins, immunity to noise, and amount of radiated noise. When changing to a product with a different part number, implement a system-evaluation test for the given product.

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(Rev.5.0-1 October 2020)

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