

Introduction

The SLG46531 GreenPAK5 has an I2C communication interface for controlling its internal blocks configuration and some connections. It is highly flexible and easy to use. This example shows its use and configuration in the design of a dual window comparator.

Design overview

The design itself is a typical window comparator. 4 ACMPs are used to create 2 full window comparators inside the chip. The I2C interface is used to turn on ACMPs and change their Vref values.

The basic window comparator consists of 2 ACMPs and a 2-bit LUT connected to their outputs. Both ACMPs IN+ are connected to one source, their IN- sources are different Vref values. The LUT truth table is configured to produce a HIGH level when the input analog voltage is between ACMPs references and produce LOW in all other cases. All ACMPs could be dynamically turned on and off via their PWR UP nodes. In this design PWR Ups are connected via I2C virtual OUTs, so they can be controlled through I2C commands. IN- references of ACMP0-ACMP3 are configured as 100, 300, 600, 900 mV respectively. All IN+ inputs source from one pin. All output PINs are configured as Push Pull 1X (please refer to Fig. 1)

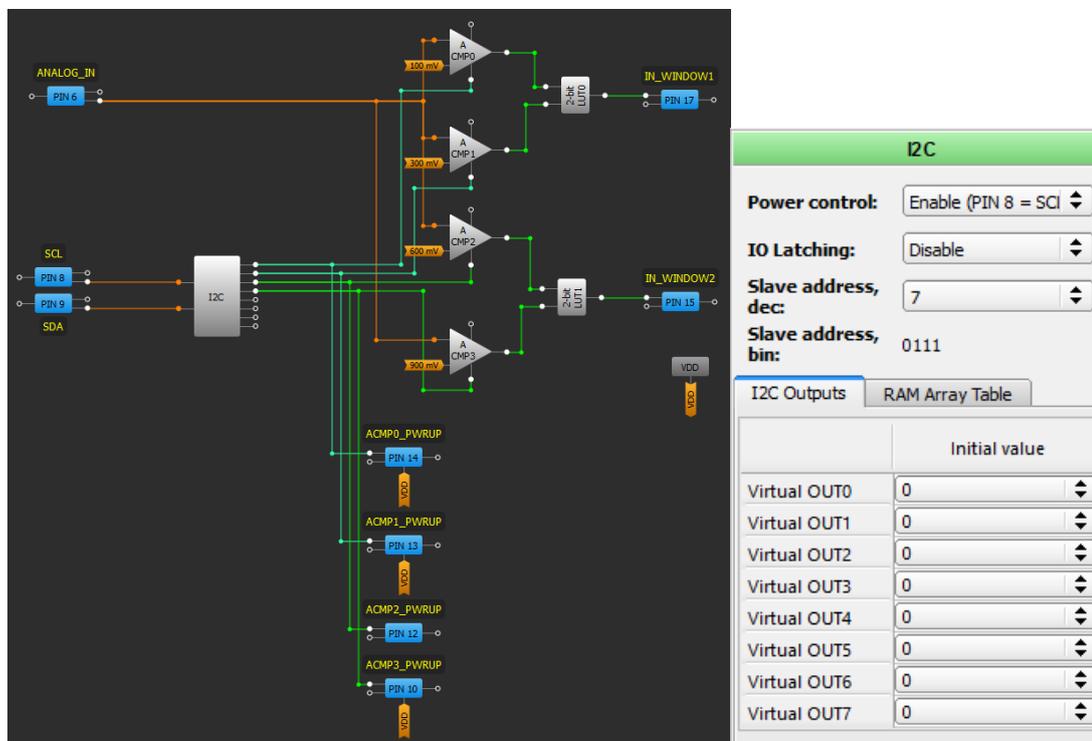


Fig. 1. Dual window comparator design viewed in the GreenPAK Designer and I2C block configuration

I2C operation

ACMP Vrefs and PWR Ups are controlled via I2C protocol. It is a standard serial data transmission protocol. An example of correct chip and internal blocks addressing begins in Fig.2. Certain pin assignments in the SLG46531 are reserved by default: SCL (serial clock) input is assigned to PIN8, while and SDA (serial data) input is assigned to PIN9.

The address of Virtual OUTs is 244 (11110100). To switch a Virtual OUT HIGH, the corresponding bit should be sent into the GreenPAK.

During GreenPAK operation there is the possibility of changing some of the chip's blocks configurations. In this design, a reference voltage of ACMPs is changed by sending to respective ACMP address its configuration byte.

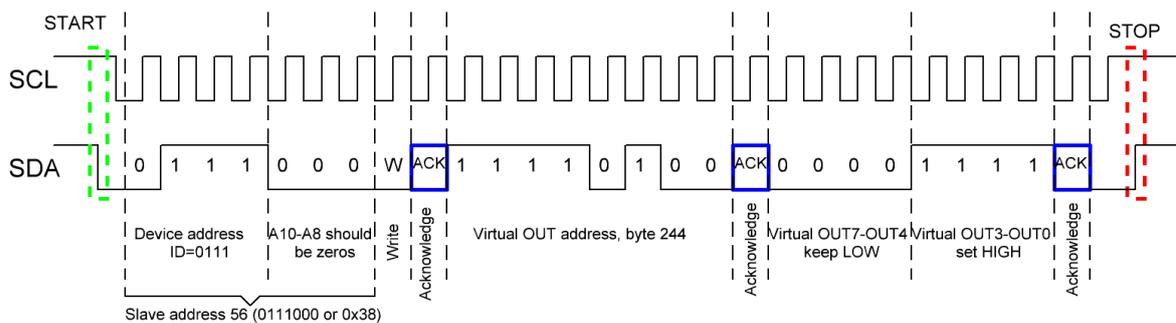


Fig. 2. ACMPs powering up via I2C programming of Virtual OUTs. Timing Diagram

Typically, I2C slave device address consists of 7 bits. GreenPAK5 uses only the 4 MSB to control its device address, so 3 LSB (A10-A8) should be set to '000'. The device address ID is configured in the I2C block properties. In this case it is set to 0111, so the slave address is 56 (0111000 or 0x38). After the device address, the read-write bit follows. If it is LOW the data will be written to the GreenPAK, if it is HIGH the data will be read from the GreenPAK.

Fig. 3 shows the process of sequential configuration byte writing into the GreenPAK. After the device address and read/write bit, ACMP0 is addressed (byte 203 or 11001011). The configuration byte follows next. It consists of Low Bandwidth Filter option bit (MSB), two Gain option bits and 5 Vref option bits (LSB). To have the next ACMP configured there is no need to send separate I2C code. The described code can be continued after ACK signal with 8 configuration bits.

I2C in GreenPAK5. Dynamic access to these

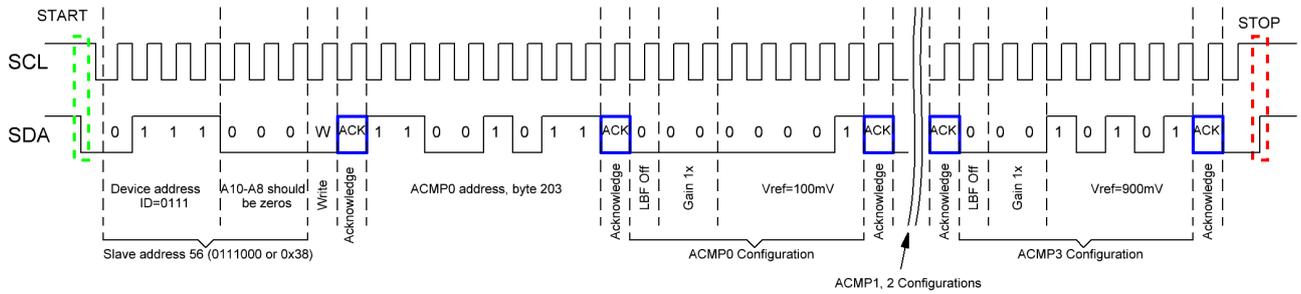


Fig. 3. ACMPs Vref programming via I2C. Timing Diagram

Conclusion

This example describes the implementation of dynamic control and reconfiguration using

and other blocks within the GreenPAK programmable mixed-signal ASIC afford the designer great flexibility.

IMPORTANT NOTICE AND DISCLAIMER

RENESAS ELECTRONICS CORPORATION AND ITS SUBSIDIARIES (“RENESAS”) PROVIDES TECHNICAL SPECIFICATIONS AND RELIABILITY DATA (INCLUDING DATASHEETS), DESIGN RESOURCES (INCLUDING REFERENCE DESIGNS), APPLICATION OR OTHER DESIGN ADVICE, WEB TOOLS, SAFETY INFORMATION, AND OTHER RESOURCES “AS IS” AND WITH ALL FAULTS, AND DISCLAIMS ALL WARRANTIES, EXPRESS OR IMPLIED, INCLUDING, WITHOUT LIMITATION, ANY IMPLIED WARRANTIES OF MERCHANTABILITY, FITNESS FOR A PARTICULAR PURPOSE, OR NON-INFRINGEMENT OF THIRD-PARTY INTELLECTUAL PROPERTY RIGHTS.

These resources are intended for developers who are designing with Renesas products. You are solely responsible for (1) selecting the appropriate products for your application, (2) designing, validating, and testing your application, and (3) ensuring your application meets applicable standards, and any other safety, security, or other requirements. These resources are subject to change without notice. Renesas grants you permission to use these resources only to develop an application that uses Renesas products. Other reproduction or use of these resources is strictly prohibited. No license is granted to any other Renesas intellectual property or to any third-party intellectual property. Renesas disclaims responsibility for, and you will fully indemnify Renesas and its representatives against, any claims, damages, costs, losses, or liabilities arising from your use of these resources. Renesas' products are provided only subject to Renesas' Terms and Conditions of Sale or other applicable terms agreed to in writing. No use of any Renesas resources expands or otherwise alters any applicable warranties or warranty disclaimers for these products.

(Disclaimer Rev.1.01 Jan 2024)

Corporate Headquarters

TOYOSU FORESIA, 3-2-24 Toyosu,
Koto-ku, Tokyo 135-0061, Japan
www.renesas.com

Trademarks

Renesas and the Renesas logo are trademarks of Renesas Electronics Corporation. All trademarks and registered trademarks are the property of their respective owners.

Contact Information

For further information on a product, technology, the most up-to-date version of a document, or your nearest sales office, please visit www.renesas.com/contact-us/.